19-2997; Rev 0; 10/03

MAXIM

8-PIN TDFN 3.0mm x 3.0mm

High-Speed, Wide-Input, Single-Phase MOSFET Driver

MAX8552

General Description

The MAX8552 highly integrated monolithic MOSFET driver is capable of driving a pair of power MOSFETs in single or multiphase synchronous buck-converter applications that provide up to 30A output current per phase. The MAX8552 simplifies PC board layout in multiphase systems, particularly three phases and higher. High input voltages up to 24V allow the MAX8552 to be used in desktop, notebook, and server applications. Each MOSFET driver is capable of driving 3000pF capacitive loads with only 12ns propagation delay and 11ns (typ) rise and fall times, making the MAX8552 ideal for high-frequency applications.

User-programmable break-before-make circuitry prevents shoot-through currents, maximizing converter efficiency. An enable input allows total driver shutdown (<1µA typ) for power-sensitive portable applications. The PWM control input is compatible with TTL and CMOS logic levels. The MAX8552, along with the MAX8524 or the MAX8525 multiphase controllers, provides flexible 2-, 3-, 4-, 6-, or 8-phase CPU core-voltage supplies.

The MAX8552 is available in space-saving 10-pin TDFN and µMAX packages and is specified for -40°C to +85°C operation.

Applications

Multiphase Buck Converters

Voltage Regulator Modules (VRMs)

Processor-Core Voltage Regulators

Desktops, Notebooks, and Servers

Switching Power Supplies

Features

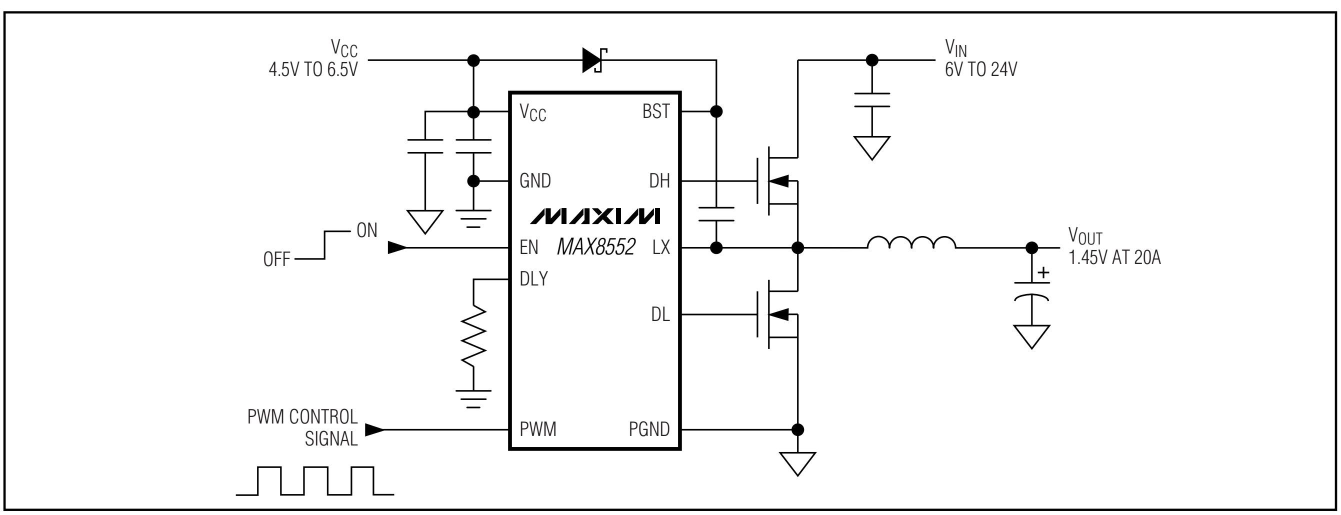
- ♦ Single-Phase Synchronous Drivers
- ♦ Up to 24V (max) Input Voltage
- ♦ 0.1µA (typ) Quiescent Current in Shutdown Over Temperature
- ♦ 0.5Ω/1.0Ω/0.7Ω/1.3Ω R_{OUT} Drivers
- ♦ 12ns (typ) Propagation Delay
- ♦ 11ns (typ) Rise/Fall Times with 3000pF Load
- ♦ Adaptive Dead Time and User-Programmable Delay Mode
- ♦ Up to 2MHz Operation with TDFN Package
- ♦ Up to 1.2MHz Operation with µMAX Package
- ♦ Enable Function
- ♦ TTL- and CMOS-Compatible Logic Inputs
- ♦ Available in a Space-Saving Thin DFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8552EUB	-40°C to +85°C	10 µMAX
MAX8552ETB	-40°C to +85°C	10 TDFN 3mm x 3mm

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +7V
PWM, EN, DL, DLY to GND ....-0.3V to (V_{CC} + 0.3V)
BST to PGND ....-0.3V to +35V
LX to PGND ....-1V to +28V
DH to PGND ....-0.3V to (V_{BST} + 0.3V)
DH, BST to LX....................-0.3V to +7V
DH and DL Continuous Current....................±200mA

Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444.4mW
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{BST} = V_{DLY} = V_{EN} = 5V, V_{GND} = V_{PGND} = V_{LX} = 0V; T_A= -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
UNDERVOLTAGE PROTECTION						
V_{CC} Supply Voltage Range			4.5		6.5	V
Undervoltage Lockout (UVLO)	0.25V hysteresis	V_{CC} rising	3.25		3.80	V
		V_{CC} falling	3.0		3.5	
Shutdown Supply Current	V_{EN} = 0V, V_{CC} = 6.5V	PWM = GND or V_{CC}, T_A= +25°C		0.04	1	µA
		PWM = GND or V_{CC}, T_A = +85°C		0.1		
Idle Supply Current (I_{CC})	No switching	V_{CC} = 6.5V, PWM = GND, R_{DLY} = 47kΩ		330	500	µA
Control Supply Current (I_{GND})	No switching	PWM = GND		25	50	µA
		PWM = V_{CC}		2	3	mA
	Switching	f_{PWM} = 250kHz, 50% duty cycle		1.8	3	mA
Driver Supply Current (I_{PGND})	No switching, I_{CC}	PWM = GND		0.1	10	µA
		PWM = V_{CC}		1.2	2	mA
	No switching, I_{BST}	PWM = GND		0.1	10	µA
		PWM = V_{CC}		1.2	2	mA
	Switching, I_{BST} + I_{CC}	250kHz		2	4	
DRIVER SPECIFICATIONS (See the *Timing Diagram*)						
DH Driver Resistance	PWM = GND, sourcing current	V_{BST} = 4.5V		1.3	2.4	Ω
		V_{BST} = 5V		1.2		
	PWM = V_{CC}, sinking current	V_{BST} = 4.5V		0.7	1.1	
		V_{BST} = 5V		0.6		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{BST} = V_{DLY} = V_{EN} = 5V, V_{GND} = V_{PGND} = V_{LX} = 0V; T_A= -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DL Driver Resistance	PWM = GND, sourcing current	V_{CC} = 4.5V		1.0	1.6	Ω
		V_{CC} = 5V		0.9		
	PWM = V_{CC}, sinking current	V_{CC} = 4.5V		0.5	0.8	
		V_{CC} = 5V		0.45		
DH Rise Time (t_{rDH})	PWM = V_{CC}	V_{BST} = 5V, 3000pF load		14		ns
DH Fall Time (t_{fDH})	PWM = GND	V_{BST} = 5V, 3000pF load		9		ns
DL Rise Time (t_{rDL})	PWM = V_{CC}	V_{CC}= 5V, 3000pF load		11		ns
DL Fall Time (t_{fDL})	PWM = GND	V_{CC}= 5V, 3000pF load		8		ns
DH Propagation Delay	PWM falling (t_{pDHf})	V_{BST} = 5V		12		ns
	PWM = V_{CC}, DL falling (t_{pDHr})	V_{BST} = 5V		14		
DL Propagation Delay	PWM rising (t_{pDLf})			9		ns
	PWM = GND, LX falling (t_{pDLr})	V_{BST} - V_{LX} = 5V		16		
EN						
Leakage Current	V_{PWM} = 0V or 6.5V, V_{EN} = 0V or 6.5V, V_{CC} = 6.5V, T_A = +25°C			0.01	1	µA
	V_{PWM} = 0V or 6.5V, V_{EN} = 0V or 6.5V, V_{CC} = 6.5V, T_A = +85°C			0.1		
Input-Voltage High Threshold	V_{CC} = 6.5V				2.5	V
Input-Voltage Low Threshold	V_{CC} = 4.5V		0.8			V
PWM						
Leakage Current	V_{PWM} = 0V or 6.5V, V_{EN} = 0V or 6.5V, V_{CC} = 6.5V, T_A = +25°C			0.01	1	µA
	V_{PWM} = 0V or 6.5V, V_{EN} = 0V or 6.5V, V_{CC} = 6.5V, T_A = +85°C			0.1		
Input-Voltage High Threshold	V_{CC} = 6.5V				3.5	V
Input-Voltage Low Threshold	V_{CC} = 4.5V		1.2			V
Input Threshold Hysteresis				0.5		V
DLY						
Delay Program Accuracy	R_{DLY} = 47kΩ, DL fall to DH rise		67.5	90.0	112.5	ns
Delay Disable-Detection Threshold			4.0		4.7	V

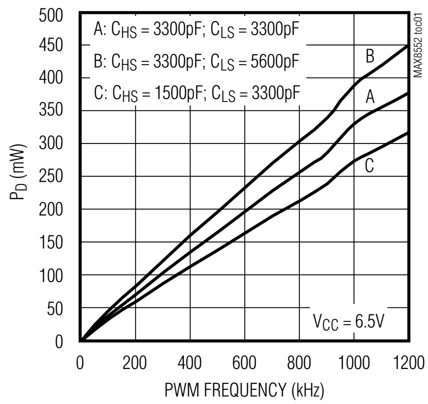
Note 1: Specifications are production tested at T_A = +25°C. Maximum and minimum limits are guaranteed by design and characterization.

High-Speed, Wide-Input, Single-Phase MOSFET Driver

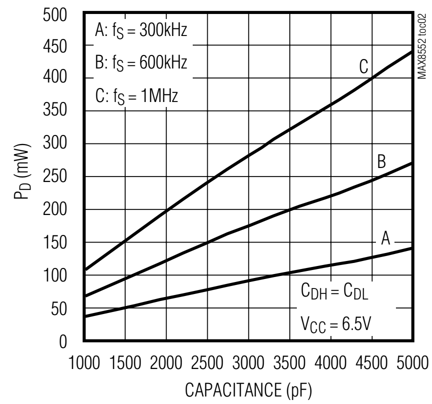
Typical Operating Characteristics

(V_{CC} = V_{DLY} = 5V, C_{HS_LOAD} = C_{LS_LOAD} = 3000pF, 50% duty ratio.)

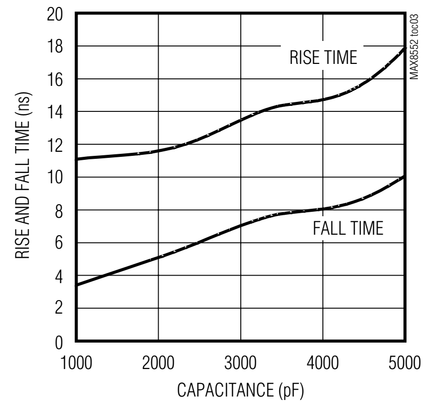
PACKAGE-POWER DISSIPATION vs. PWM FREQUENCY



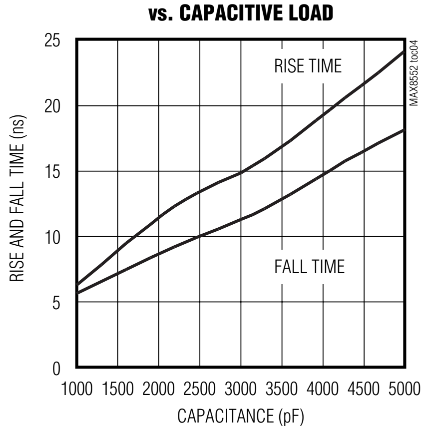
PACKAGE-POWER DISSIPATION vs. CAPACITIVE LOAD ON DH AND DL



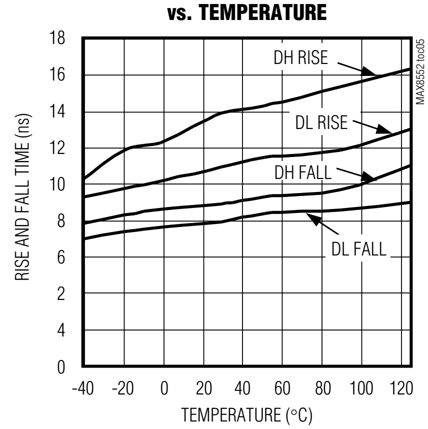
DL RISE AND FALL TIMES vs. CAPACITIVE LOAD



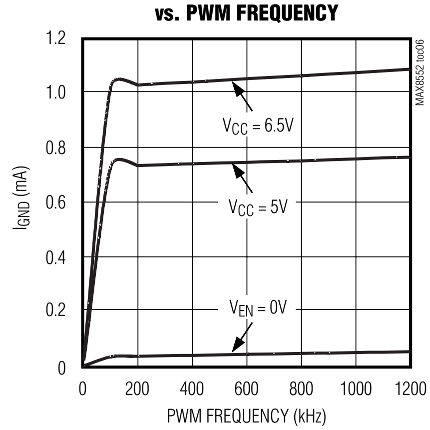
DH RISE AND FALL TIMES vs. CAPACITIVE LOAD



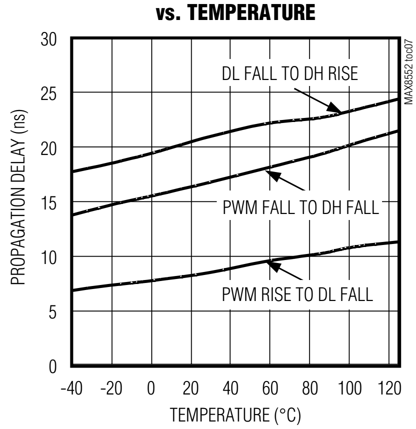
DH AND DL RISE AND FALL TIMES vs. TEMPERATURE



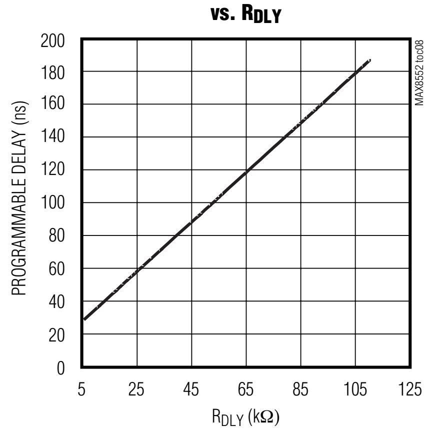
CONTROL-CIRCUITRY CURRENT vs. PWM FREQUENCY



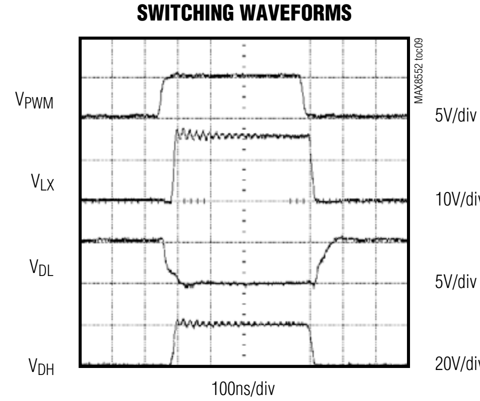
PROPAGATION DELAY vs. TEMPERATURE



PROGRAMMABLE DELAY (t_{DLY}) vs. R_{DLY}



TYPICAL APPLICATION CIRCUIT SWITCHING WAVEFORMS



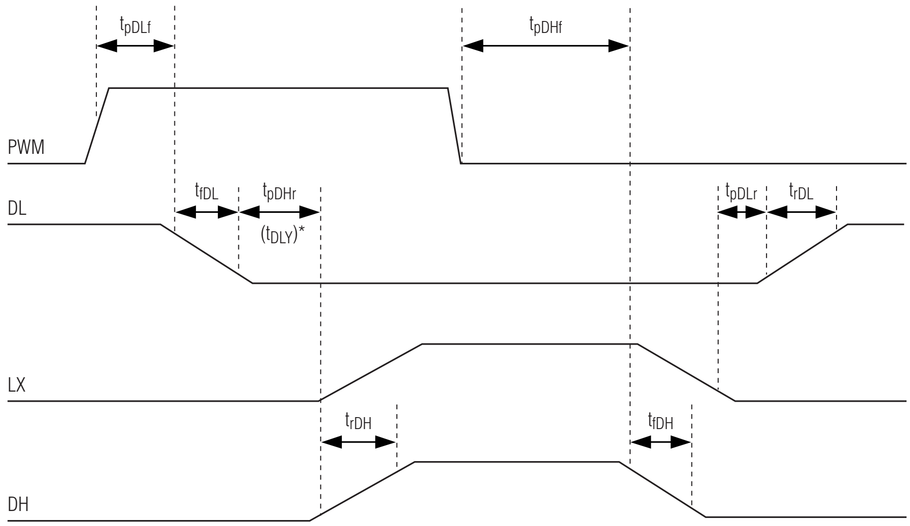
Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Input Supply Voltage. Connect to a supply voltage in the 4.5V to 6.5V range. Bypass to PGND with a 2.2µF or larger capacitor, and bypass to GND with a 0.47µF or larger capacitor.
2	DL	External Synchronous-Rectifier N-MOSFET Gate-Driver Output. Swings between V_{CC} and PGND. Anticrowbar feature prevents DL from turning on until DH is off and (LX - PGND) < 2V. DL is pulled to GND in shutdown.
3	PGND	Power Ground
4	GND	Analog Ground
5	DLY	Dead-Time Delay Programming Input. Connect a resistor from DLY to GND to set the dead-time delay between when DL falls and when DH rises. Connect DLY to V_{CC} to disable the delay function. See the *Typical Operating Characteristics* for R_{DLY} selection.
6	PWM	PWM Input. DH is high when PWM is high; DL is high when PWM is low. Input frequency can be as high as 1.2MHz for the 10-pin µMAX package and as high as 2MHz for the 10-pin TDFN package.
7	EN	Enable Input. Drive high to enable output drivers. Drive low to disable output drivers and place the IC in low-power shutdown mode.
8	LX	Switching Node and Inductor Connection. Low power supply for the DH high-side gate driver. Connect to the source of the high-side N-MOSFET and the drain of the low-side N-MOSFET, as well as the switched side of the inductor.
9	DH	External High-Side N-MOSFET Gate-Driver Output. Swings between LX and BST. Anticrowbar feature delays DH from turning on until DL is off. An additional user-programmable delay can be added. DH is pulled to LX in shutdown.
10	BST	Boost Flying-Capacitor Connection. Gate-drive power supply for DH high-side gate driver. Connect a 0.47µF or larger capacitor between BST and LX.
—	Exposed Paddle*	Exposed Paddle. Connect to GND.

**10-pin TDFN only.*

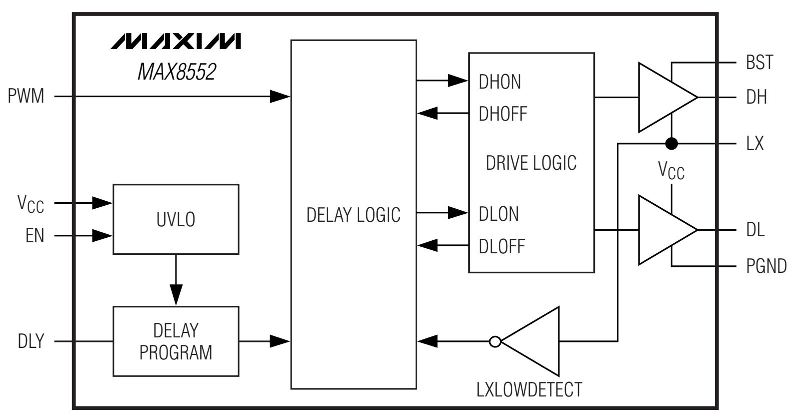
High-Speed, Wide-Input, Single-Phase MOSFET Driver

Timing Diagram



*WHEN R_{DLY} IS USED, t_{pDHr} BECOMES THE LONGER OF THE USER-PROGRAMMABLE TIME DELAY, t_{DLY}, OR THE ADAPTIVE DEAD TIME, t_{pDHr}. DRAWING IS NOT TO SCALE.

Functional Diagram



Detailed Description

The MAX8552 single-phase gate driver, along with the MAX8524/MAX8525 multiphase controllers, provide flexible one- to eight-phase CPU core-voltage supplies. The 1.0Ω/1.3Ω driver resistance allows up to 30A output current per phase. Each MOSFET driver in the MAX8552 is capable of driving 3000pF capacitive loads with only 12ns propagation delay and 11ns (typ) rise and fall times, allowing operation up to 1.2MHz per phase. Adaptive dead time controls MOSFET turn-on, and user-programmable dead time provides additional flexibility for high-side MOSFET turn-on. This maximizes converter efficiency, while allowing operation with a variety of MOSFETs and PWM-controller ICs. An undervoltage-lockout circuit allows proper power-on sequencing. The PWM signal input is both TTL and CMOS compatible. An enable input allows total driver shutdown (<0.1µA typ) for power-sensitive portable applications.

MOSFET Gate Drivers (DH, DL)

The high-side driver (DH) has a 1.3Ω (typ) sourcing resistance and 0.7Ω sinking resistance, resulting in 4A peak sourcing current and 7A peak sinking current with a 5V supply voltage. The low-side driver (DL) has a typical 1.0Ω sourcing resistance and 0.5Ω sinking resistance, yielding 5A peak sourcing current and 10A peak sinking current. This reduces switching losses, making the MAX8552 ideal for both high-frequency and high-output-current applications.

Shoot-Through Protection and Programmable Delay (t_{DLY})

The MAX8552 incorporates adaptive shoot-through protection for the switching transition after the high-side MOSFET turns off and before the low-side MOSFET turns on and vice versa. The low-side driver turns on only when the LX voltage falls below 2.4V. Furthermore, the delay time between the low-side MOSFET turn-off and high-side MOSFET turn-on can be adjusted by selecting the value of R1 (see the *R_{DLY} Selection* section).

Undervoltage Lockout

When V_{CC} is below the UVLO threshold (3.5V typ), DH and DL are held low. Once V_{CC} is above the UVLO threshold and while PWM is low, DL is driven high and DH is driven low. This prevents the output of the converter from rising before a valid PWM signal is applied.

EN

When EN is low, the MAX8552 is in shutdown mode and the total input current is reduced to less than 1µA for power-sensitive applications. In shutdown mode, both DH and DL are held low. When EN goes high, the MAX8552 becomes active.

Applications Information

Decoupling of V_{CC}

V_{CC} provides the supply voltage for the internal logic circuits. Bypass V_{CC} with a 2.2µF or larger capacitor to PGND and a 0.47µF or larger capacitor to GND to limit noise to the internal circuitry. Connect these bypass capacitors as close to the IC as possible.

Boost Flying-Capacitor Selection

The MAX8552 uses a bootstrap circuit to generate the necessary drive voltage (V_{DH}) to fully enhance the high-side N-MOSFET. The selected high-side MOSFET determines appropriate boost capacitance values (C6 in the Typical Application Circuit, Figure 1), according to the following equation:

$$C_{BST} = Q_{GATE} / \Delta V_{BST}$$

where Q_{GATE} is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver. Choose ΔV_{BST} = 0.1V to 0.2V when determining C_{BST}. The boost flying-capacitor should be a low-equivalent series resistance (ESR) ceramic capacitor.

R_{DLY} Selection

Connect DLY to V_{CC} to disable the programmable delay function and default to the adaptive delay time. To program a longer specific delay time between the low-side MOSFET driver turn-off and the high-side MOSFET turn-on, connect a delay resistor, R_{DLY}, between DLY and GND (R1 in the Typical Application Circuit, Figure 1). See the *Typical Operating Characteristics* to select R_{DLY}.

Avoiding dV/dt Turning on the Low-Side MOSFET

At high input voltages, fast turn-on of the high-side MOSFET can momentarily turn on the low-side MOSFET due to the high dV/dt appearing at the drain of the low-side MOSFET. The high dV/dt causes a current flow through the Miller capacitance (C_{RSS}) and the input capacitance (C_{ISS}) of the low-side MOSFET. Improper selection of the low-side MOSFET that results in a high ratio of C_{RSS}/C_{ISS} makes the problem more severe. To avoid this problem, minimize the ratio of C_{RSS}/C_{ISS} when selecting the low-side MOSFET. Adding a 1Ω resistor between BST and C_{BST} can slow the high-side MOSFET turn-on. Similarly, adding a small capacitor from the gate to the source of the high-side MOSFET has the same effect. However, both methods work at the expense of increased switching losses.

High-Speed, Wide-Input, Single-Phase MOSFET Driver

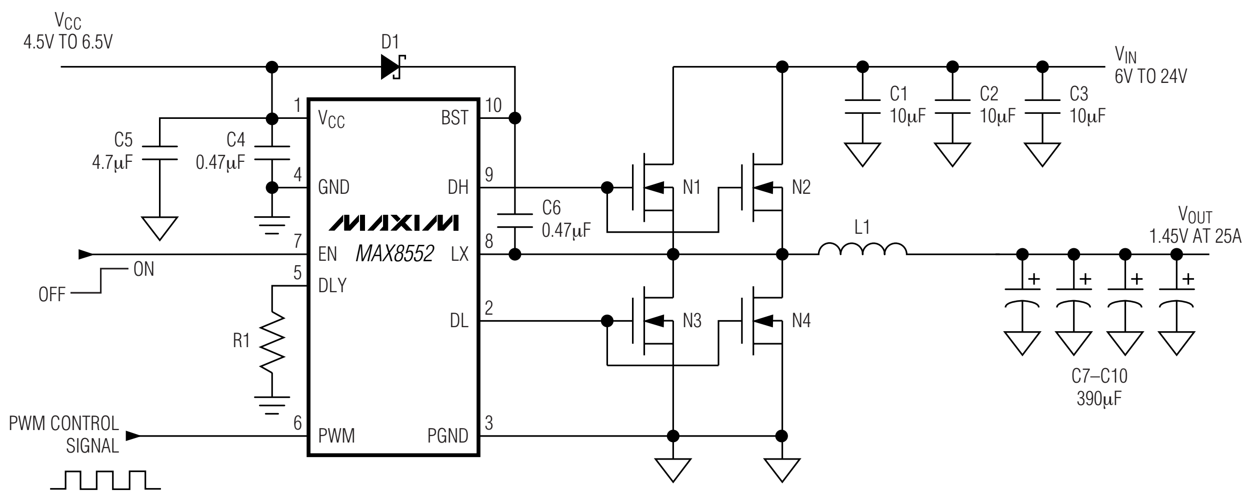


Figure 1. Typical Application Circuit

Table 1. Typical Component Values (500kHz Operation, 25A/Phase Output Current)

DESIGNATION	DESCRIPTION	PART
C1, C2, C3	10µF, 25V ceramic capacitor	Taiyo Yuden TMK432BJ106MM
C4	4.7µF, 10V ceramic capacitor	Taiyo Yuden LMK316 BJ475ML
C5, C6	0.47µF, 10V ceramic capacitor	Taiyo Yuden LMK107BJ474KA
C7–C10	390µF/2V SP capacitor	Panasonic EEFUE0D391XR
D1	30V, 200mA, V_F = 0.5V Schottky diode	Fairchild BAT54S
L1	0.66µH/29A, 0.9mΩ typical R_{DC} resistance	Panasonic PCC-NX3
N1, N2	30V, 14A N-MOSFET	International Rectifier IRF7821
N3, N4	30V, 18A N-MOSFET	International Rectifier IRF7832
R1	6kΩ - 125kΩ = 1%, 1/8W resistor	Panasonic

Layout Guidelines

The MAX8552 MOSFET driver sources and sinks large currents to drive MOSFETs at high switching speeds. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PC board layout guidelines are recommended when designing with the MAX8552:

1) Place all decoupling capacitors as close to their respective IC pins as possible.
2) Minimize the length of the high-current loop from the input capacitor, the upper switching MOSFET, and the low-side MOSFET back to the input-capacitor negative terminal.
3) Provide enough copper area at and around the switching MOSFETs and inductors to aid in thermal dissipation.
4) Connect PGND of the MAX8552 as close as possible to the source of the low-side MOSFETs.
5) Keep LX away from sensitive analog components and nodes. Place the IC and the analog components on the opposite side of the board from the power-switching node if possible.

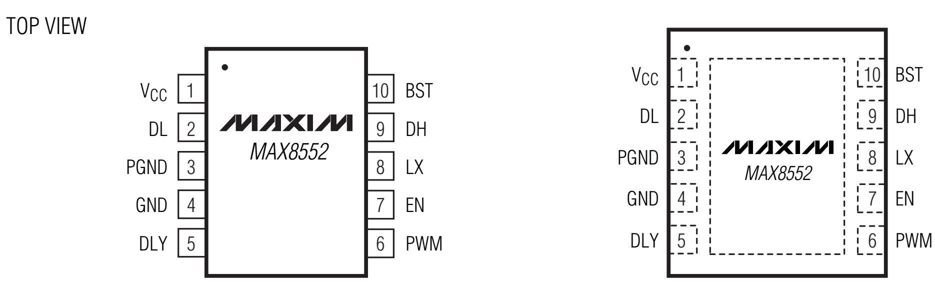
A sample layout is available in the MAX8552 evaluation kit.

Chip Information

TRANSISTOR COUNT: 638

PROCESS: BiCMOS

Pin Configurations

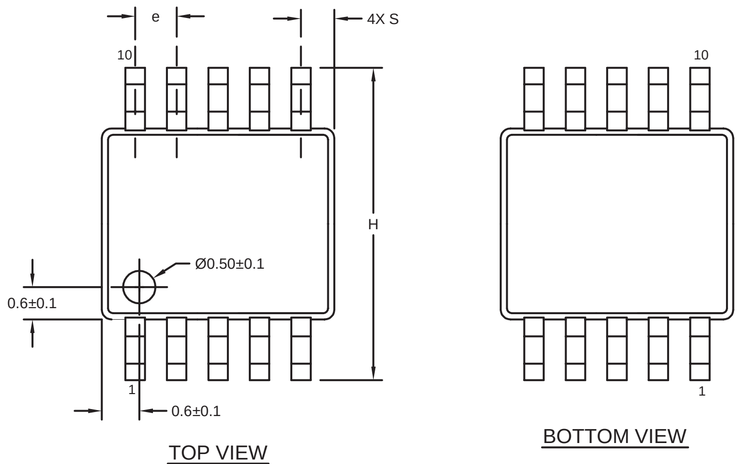


μMAX 3mm x 4.9mm

TDFN 3mm x 3mm

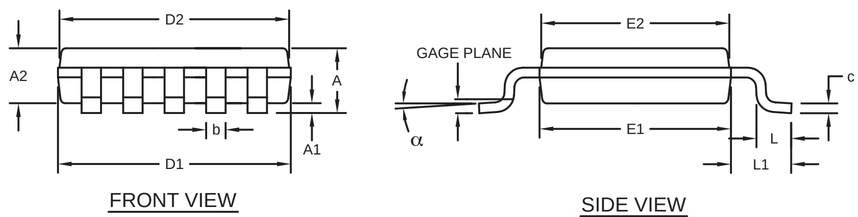
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

10LUMAX.EPS



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

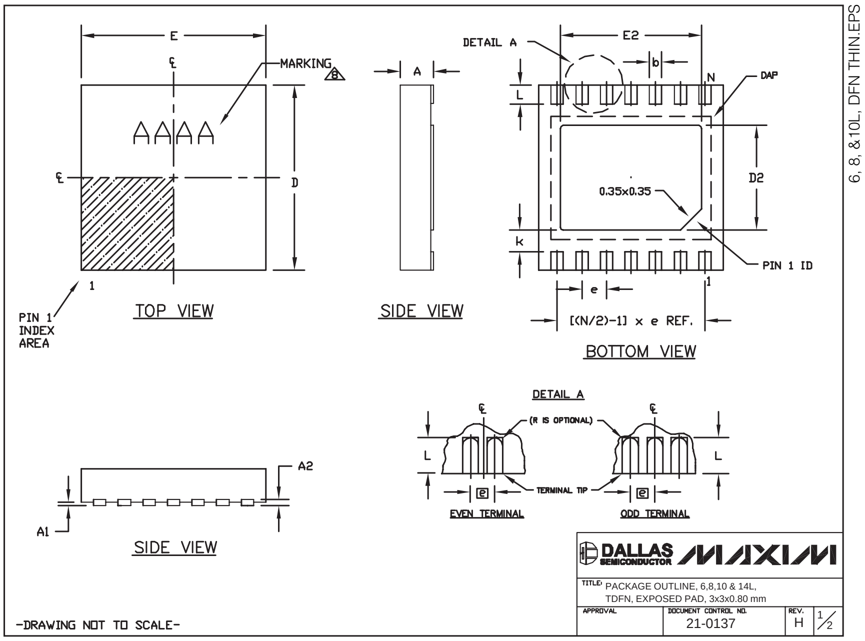
TITLE:

PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

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-DRAWING NOT TO SCALE-

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