PCN Number:	20181005001.0	PCN Date:	October 08, 2018
Title:	Datasheet for DS90UB934-Q1		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:		
☐ Assembly Site	☐ Design	☐ Wafer Bump Site
☐ Assembly Process	☒ Data Sheet	☐ Wafer Bump Material
☐ Assembly Materials	☐ Part number change	☐ Wafer Bump Process
☐ Mechanical Specification	☐ Test Site	☐ Wafer Fab Site
☐ Packing/Shipping/Labeling	☐ Test Process	☐ Wafer Fab Materials
		☐ Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.
The following change history provides further details.

TEXAS INSTRUMENTS

DS90UB934-Q1

SNLS507B – SEPTEMBER 2016 – REVISED OCTOBER 2018

Changes from Revision A (January 2017) to Revision B	Page
• Added that unused GPIOs can be left open or floating	5
• Added that PDB is internal pull down enabled	5
• Added description for selecting pull up resistor for OSS_SEL	5
• Added description for selecting pull up resistor for OEN	5
• Removed S, PD type for RES (pin 44)	6
• Removed S, PD type for RES (pin 43) and added it must be tied to GND.	6
• Added PDB test conditions for the LVCMOS IO voltage parameter in the *Absolute Maximum Ratings* table	7
• Changed typical LVCMOS low-to-high transition time value from: 2.5 ns to: 2 ns	11
• Changed maximum LVCMOS low-to-high transition time value from: 4 ns to: 3 ns	11
• Changed typical LVCMOS high-to-low transition time value from: 2.5 ns to: 2 ns	11
• Changed maximum LVCMOS high-to-low transition time value from: 4 ns to: 3 ns	11
• Changed receiver clock jitter test condition from: SSCG[3:0] = OFF to: SSCG[0] = OFF	11
• Changed deserializer period jitter test condition from: SSCG[3:0] = OFF to: SSCG[0] = OFF	11
• Changed deserializer cycle-to-cycle clock jitter test condition from: SSCG[3:0] = OFF to: SSCG[0] = OFF	11
• Changed input jitter symbol from: TOL_{JIT} to: T_{IJIT}	12
• Added reference to compatibility with DS90UB953-Q1/935-Q1 serializers	17
• Added column for DS90UB953-Q1/935-Q1	20
• Added clarification on input mode selection	20
• Fixed typo in Figure 13 supply rail text	20
• Changed pullup power supply node from VDDIO to V(I2C)	26
• Removed pullup resistor recommendation	26
• Updated description of clock frequency during BIST operation	31
• Fixed typos in register maps	32

The datasheet number will be changing.

Device Family	Change From:	Change To:
DS90UB934-Q1	SNLS507A	SNLS507B

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/DS90UB934-Q1

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

DS90UB934TRGZRQ1	DS90UB934TRGZTQ1		

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
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