

N-channel 30 V, 0.021 Ω typ., 6 A STripFET™ VI DeepGATE™ Power MOSFET in a SOT23-6L package

Datasheet - production data

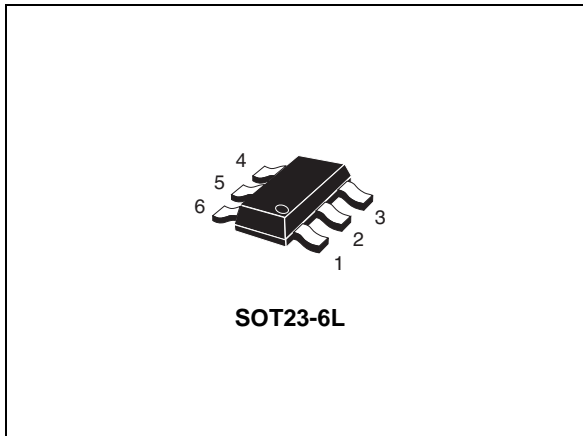
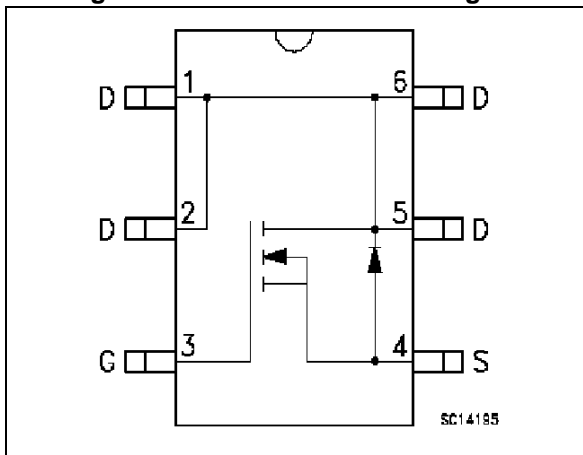


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max	I _D	P _{TOT}
STT6N3LLH6	30 V	0.025 Ω (V _{GS} = 10 V)	6 A	1.6 W
		0.036 Ω (V _{GS} = 4.5 V)		

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STT6N3LLH6	STG1	SOT23-6L	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	6	A
I_D	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	3.75	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	1.6	W
	Derating factor	0.013	W/ $^\circ\text{C}$
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	78	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30\text{ V}$ $V_{DS} = 30\text{ V}$, $T_c = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$		0.021	0.025	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 3\text{ A}$		0.032	0.036	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance		-	283	-	pF
C_{oss}	Output capacitance	$V_{DS} = 24\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	61	-	pF
C_{rss}	Reverse transfer capacitance		-	31	-	pF
Q_g	Total gate charge	$V_{DD} = 10\text{ V}$, $I_D = 6\text{ A}$	-	3.6	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\text{ V}$	-	1.5	-	nC
Q_{gd}	Gate-drain charge	Figure 14	-	1.1	-	nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ Figure 13	-	4.8	-	ns
t_r	Rise time		-	11.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	9.4	-	ns
t_f	Fall time		-	5.4	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 16\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ Figure 15	-	10.6	-	ns
Q_{rr}	Reverse recovery charge		-	2.8	-	nC
I_{RRM}	Reverse recovery current		-	0.5	-	A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

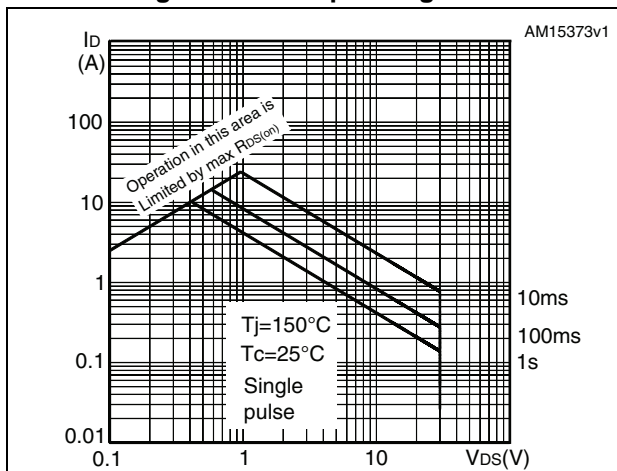


Figure 3. Thermal impedance

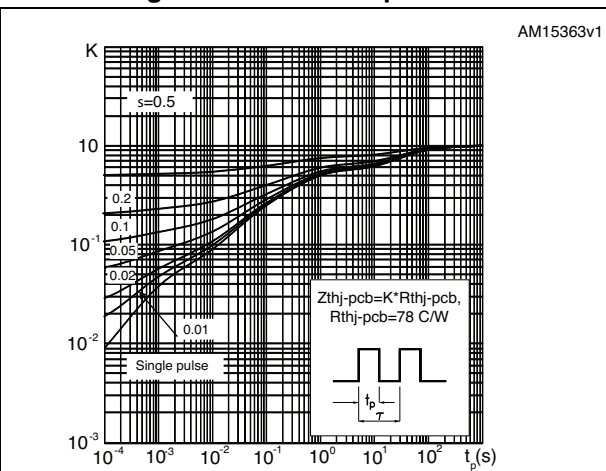


Figure 4. Output characteristics

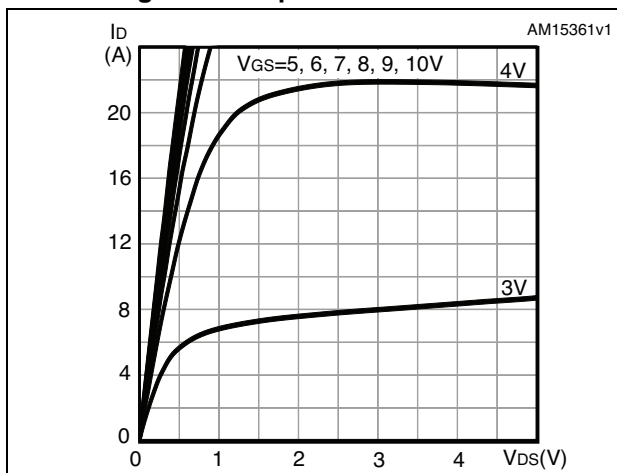


Figure 5. Transfer characteristics

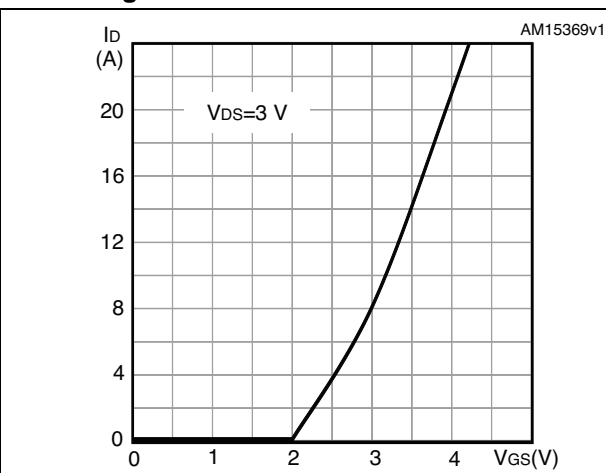


Figure 6. Gate charge vs gate-source voltage

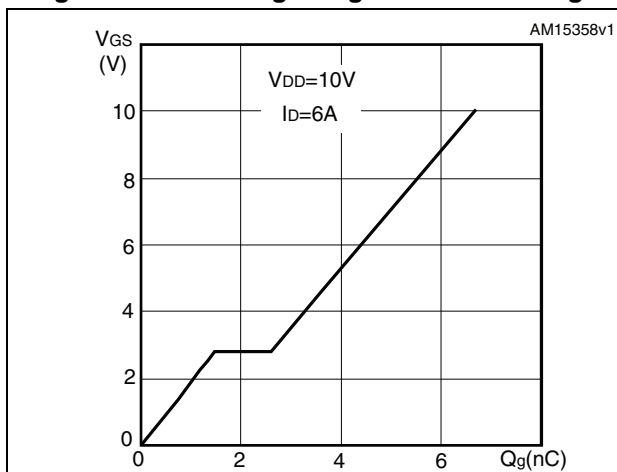


Figure 7. Static drain-source on-resistance

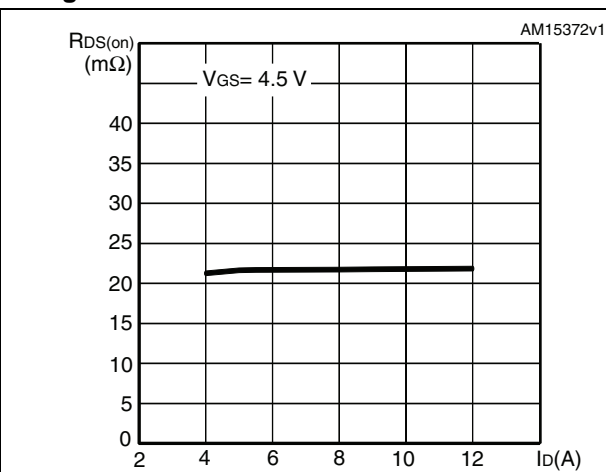


Figure 8. Capacitance variations

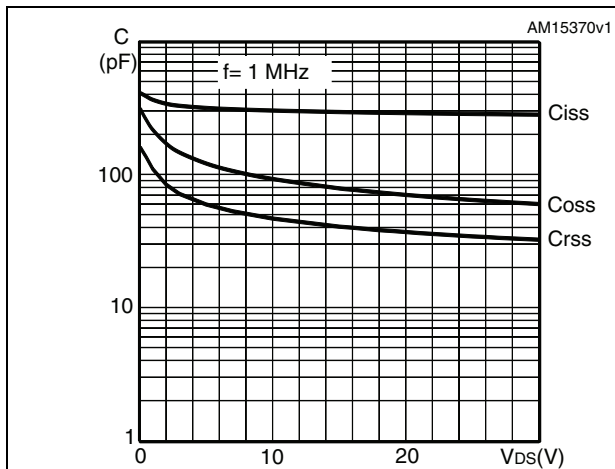


Figure 9. Normalized on-resistance vs temperature

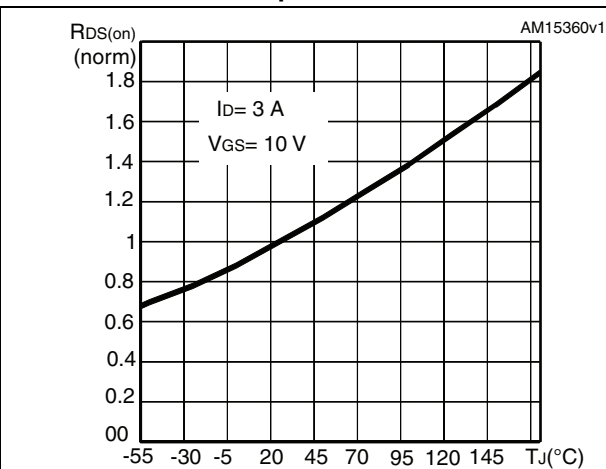


Figure 10. Normalized gate threshold voltage vs temperature

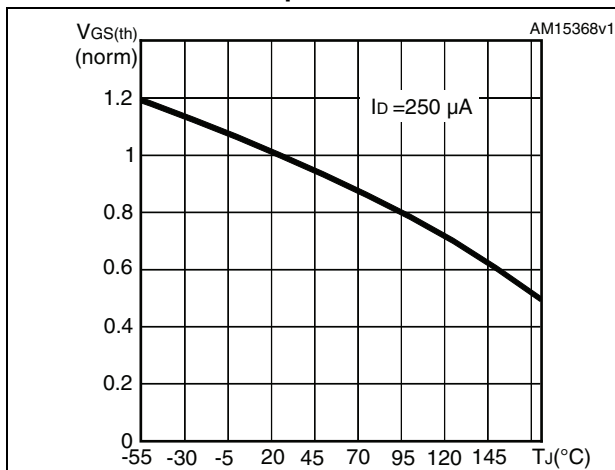


Figure 11. Normalized V(BR)DSS vs temperature

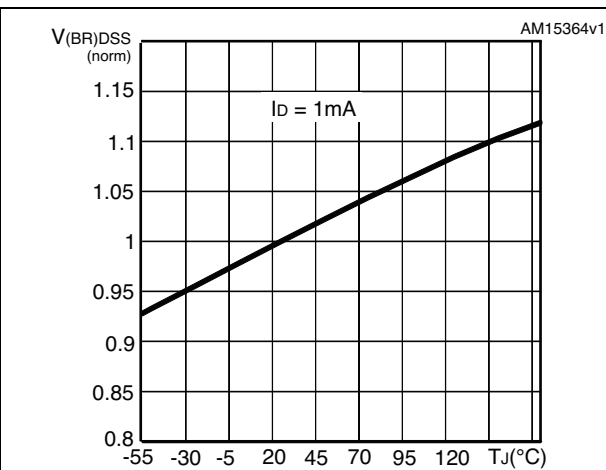
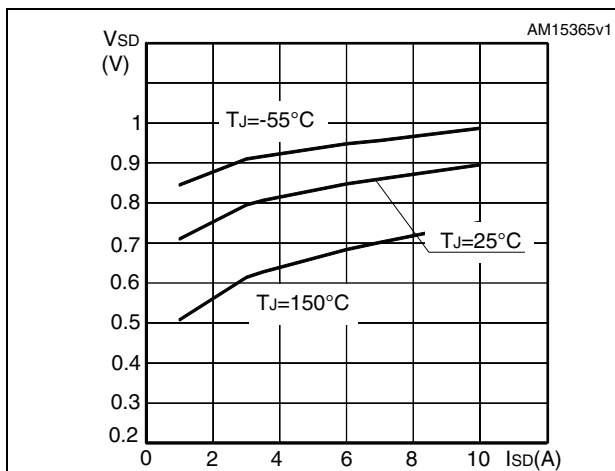
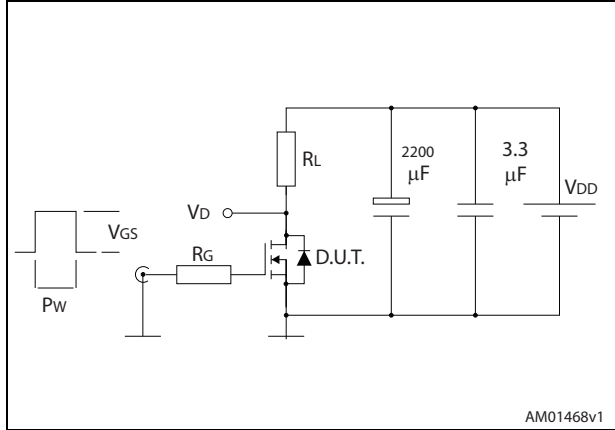


Figure 12. Source-drain diode forward characteristics



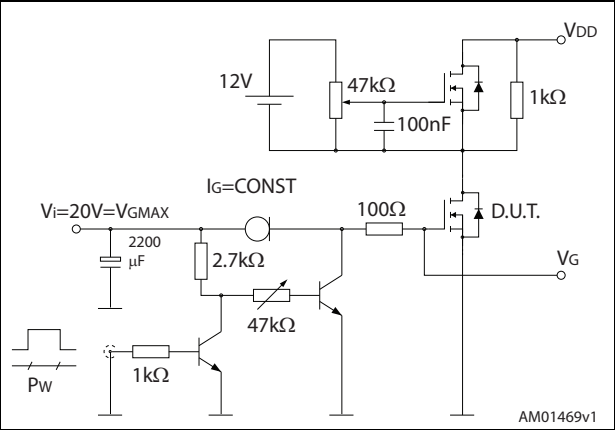
3 Test circuits

Figure 13. Switching times test circuit for resistive load



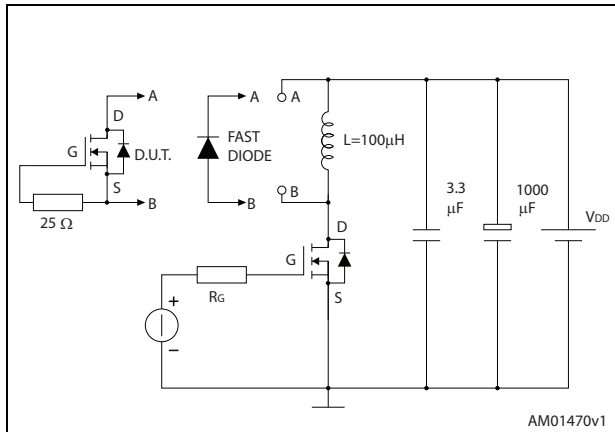
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Figure 14. Gate charge test circuit



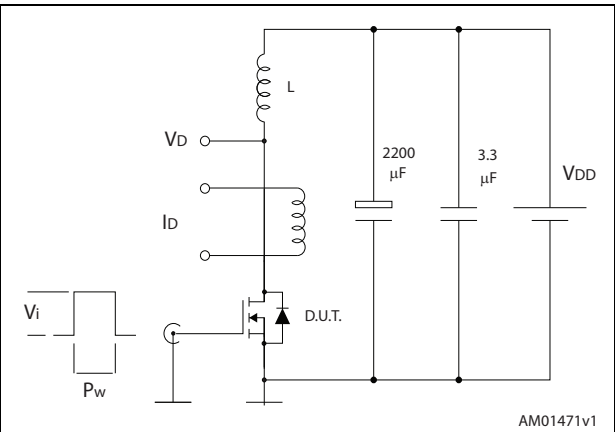
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Figure 15. Test circuit for inductive load switching and diode recovery times



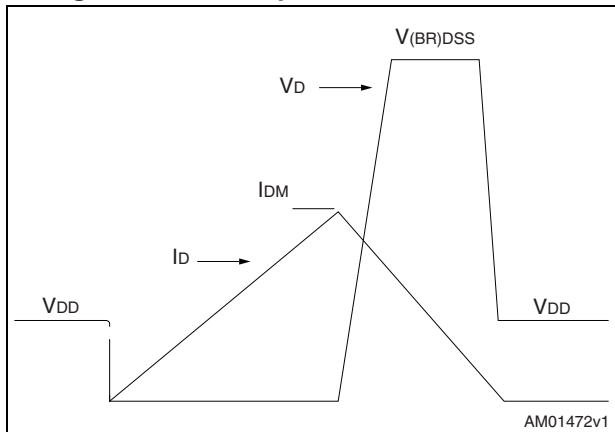
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Figure 16. Unclamped inductive load test circuit



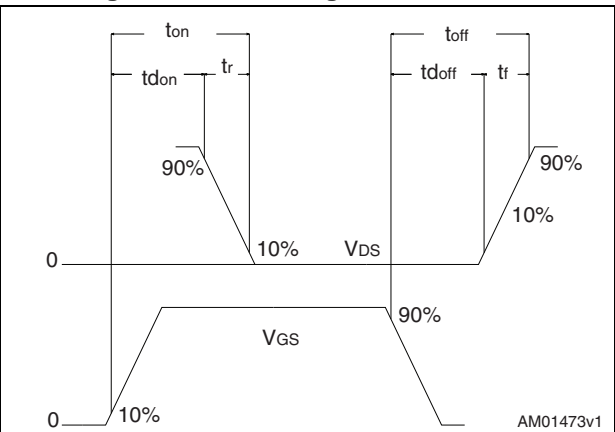
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Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



AM01473v1

4 Package mechanical data

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Figure 19. SOT23-6L package drawing

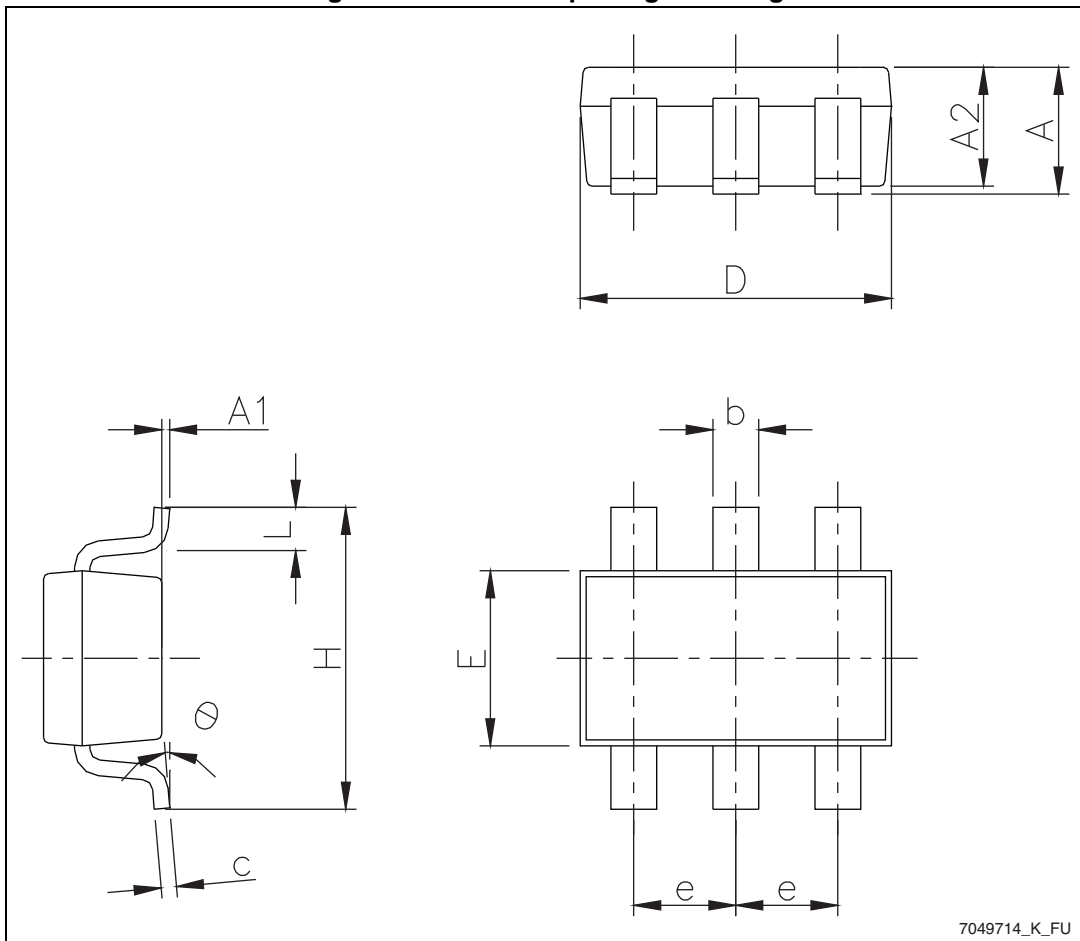
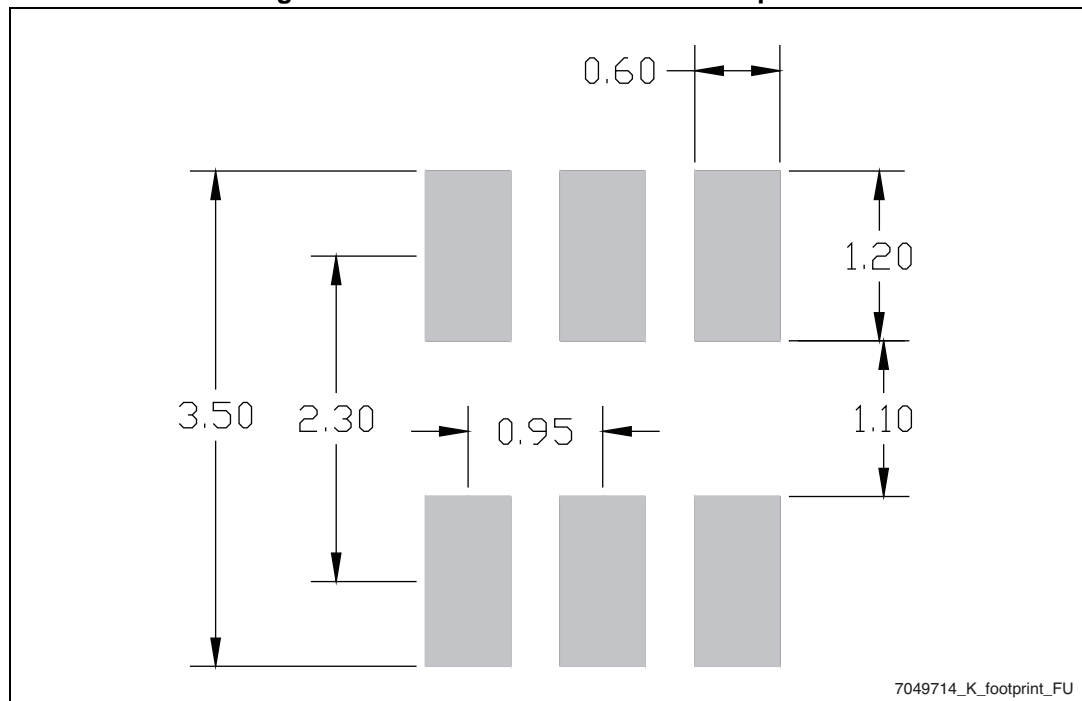


Table 8. SOT23-6L package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.25
A1	0.00		0.15
A2	1.00	1.10	1.20
b	0.36		0.50
C	0.14		0.20
D	2.826	2.926	3.026
E	1.526	1.626	1.726
e	0.90	0.95	1.00
H	2.60	2.80	3.00
L	0.35	0.45	0.60
θ	0°		8°

Figure 20. SOT23-6L recommended footprint^(a)



a. All dimensions are in millimeters

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Oct-2012	1	First release.
24-Oct-2013	2	Modified: $R_{DS(on)}$ value on : Features table and in Table 4 . Document status promoted from preliminary to production data.
11-Mar-2014	3	Updated Section 4: Package mechanical data . Minor text changes

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