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Keywords: hot-swap,five-channel,positive and negative channels,MAX5927,MAX5927A,five-channel hot swap circuit

REFERENCE DESIGN 4228 INCLUDES: ✓Tested Circuit ✓Schematic ✓BOM ✓Description ✓Test Data ✓Layout

A Five-Channel (Three +V and Two -V) Hot-Swap Reference Design

Jun 27, 2008

Abstract: This article presents a five-channel hot-swap circuit that handles both positive and negative input voltages with sequential turn-on. The unique configuration allows two negative-voltage channels not protected by circuit breakers, in addition to three positive-voltage channels, to be controlled by a single MAX5927A positive-voltage hot-swap controller. The included test data verifies that the circuit meets the described load and power-sequencing requirements of the five channels.

Introduction

This five-channel circuit provides hot-swap functions for three positive-voltage circuits and for two negative-voltage circuits, though it employs only a single MAX5927A four-channel hot-swap controller. The **Figure 1** circuit meets the following load and power-sequencing requirements:

- Ch1 = +3.3V at 2A (circuit breaker at $\geq 3A$)
- Ch2 = +5V at 1.6A (circuit breaker at $\geq 2.4A$)
- Ch3 = +12V at 2A (circuit breaker at $\geq 3A$)
- Ch4 = -12V at 150mA (no circuit-breaker action)
- Ch5 = -5V at 50mA (no circuit-breaker action)
- Startup timing is such that channels 2 (+5V) and 3 (+12V) begin to turn on as soon as active-low CARD_PRESENT goes low. STAT2 and STAT3 go active-high 10.8ms after active-low CARD_PRESENT goes low.
- Channel 1 (+3.3V) turn-on is delayed by 11.8ms from channels 2 and 3. STAT1 goes high 10.8ms after channel 1 begins to turn on.
- Turn-on of channels 4 (-12V) and 5 (-5V) is delayed by 27.8ms from channels 2 and 3. STAT4 goes high 10.8ms after channels 4 and 5 begin to turn on.
- Latching fault management. If any of channels 1 through 3 experiences a fault, all channels will shut down until active-low CARD_PRESENT is cycled off and on.

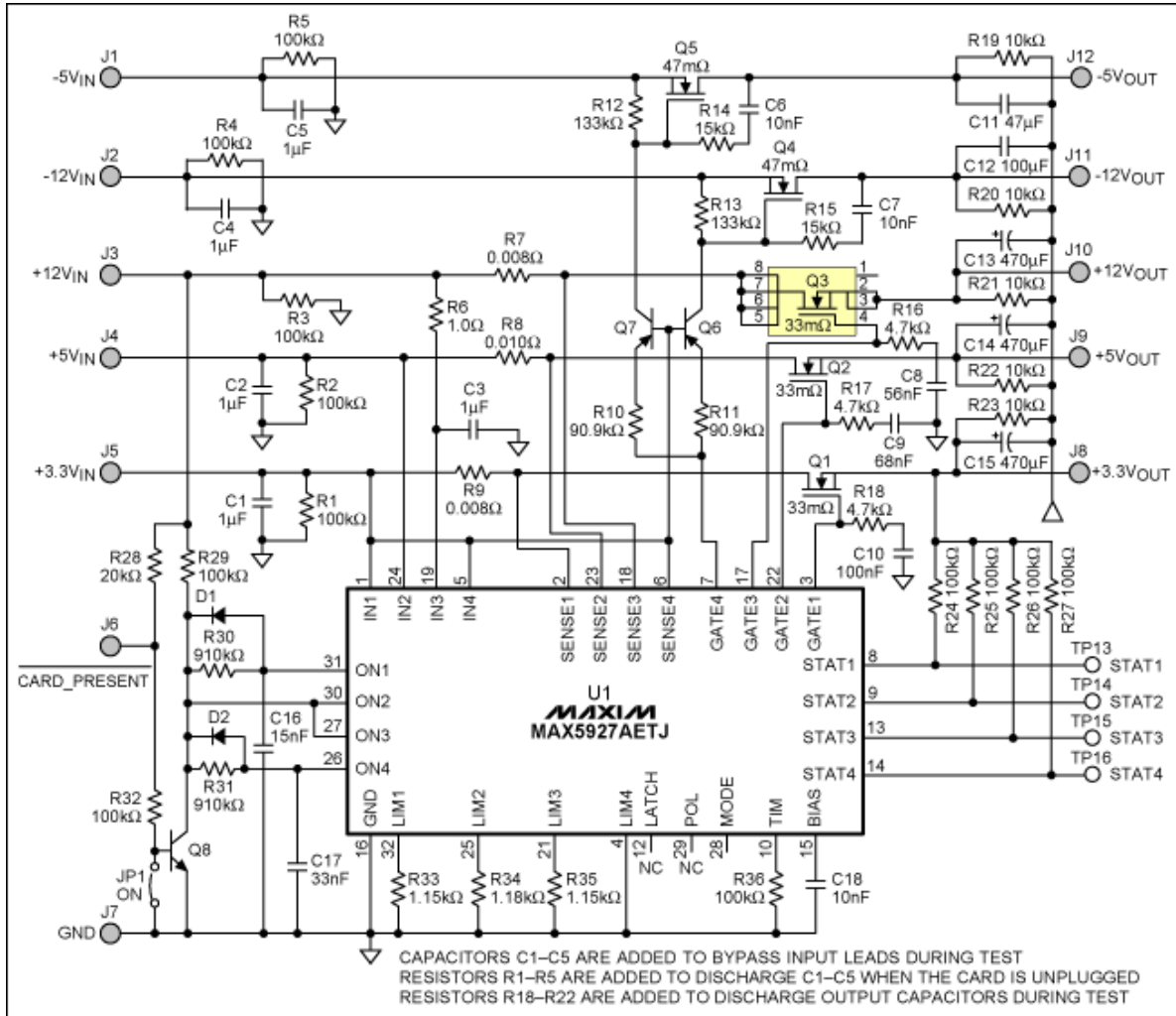


Figure 1. This five-channel hot-swap circuit controls three positive-voltage and two negative-voltage channels.

Although the delay requirements and fault management are specific to this design, the delays may be modified for other timing needs. Fault management may be changed to autoretry mode, if desired.

Hot-Swap Controller Selection

The MAX5927A is chosen for its specified +15V absolute-maximum input voltage, whereas the MAX5927 is specified at 14V. This voltage advantage is considered important if even a minor circuit inductance is present in the 12V power-supply circuit, as a 12V circuit may experience supply-voltage ringing and overshoot when the circuit is opened at circuit-breaker overload.

Turn-On Timing

Resistor R36 (at IC pin 10) sets each channel's turn-on time to 10.8ms ±2.8ms. The MAX5927A's internal slow comparator is disabled during this time, allowing load-capacitor charging current to be twice the preset current-trip values for each of channels 1 to 3, should that be desired. Load capacitors are easily charged to final value during this time without tripping the circuit breakers. This startup delay may be set anywhere from 400µs (min) to 50ms (max) by adjusting the value of R36 between 4kΩ and 500kΩ. The STAT outputs transition from FALSE to TRUE at the end of this startup time. STAT outputs are positive true, but may be set to negative true by grounding POL (pin 29).

Channel 1 turn-on is delayed 11.8ms from channels 2 and 3 by the (R29 + R30) - C16 time constant; C16 may be increased for a longer delay. STAT1 goes high 10.8ms after channel 1 begins to turn on.

Turn-on of channels 4 and 5 is delayed 28ms from channels 2 and 3 by the (R29 + R31) - C17 time constant; C17 may be increased for a longer delay, or R31 may be decreased for a shorter delay. STAT4 goes high 10.8ms after channels 4 and 5 begin to turn on.

MODE is set (open pin 28) to configure the MAX5927A for power-sequencing mode.

Output-Voltage Slew Rate

All channels are set for output-voltage slew rates of ~1V/ms, and the values are independent of load capacitor (C11 to C15) values. The C6 to C10 gate-capacitor values may be modified to change the slew rates. Slew rate may be calculated as $\Delta V/\Delta t = I_{GATE}/C_{GATE}$. This formula is not exact because FET gate capacitance has not been included in the calculation. Gate-charging current for GATE1, GATE2, and GATE3 is ~100 μ A. Gate-charging current for Q4 and Q5 is 30 μ A to 50 μ A because of the current in R10 and R11. Load-capacitor charging current may be calculated as $I_{CHARGE} = C_{LOAD} \times \Delta V/\Delta t$. It follows that $I_{GATE}/C_{GATE} = I_{CHARGE}/C_{LOAD}$. Capacitors C8 to C10 allow the outputs of channels 1 to 3 to slew at ~1V/ms. At no load, C13 to C15 charge at ~0.5A until full outputs are reached. If C8 to C10 are absent, the outputs charge the load capacitors at up to twice the current-trip values calculated above. Capacitors C6 and C7 are 10nF, thus allowing channels 4 and 5 to slew at ~1V/ms.

Circuit-Breaker Set Points

Channels 1 (+3.3V) and 3 (+12V) current limits are set by the slow-comparator threshold of 21mV to 27.5mV, and R7 = R9 = 8.3m Ω . The default value is multiplied by a factor of ~1.13 by R33 = R35 = 1.15k Ω for a final value of ~3.1A to 3.8A. The channel 2 (+5V) current limit is set by the slow-comparator threshold of 21mV to 27.5mV and R8 = 10m Ω . The default value is multiplied by a factor of ~1.15 by R34 = 1.18k Ω , for a final value of ~2.415A to 3.625A. Other current-limit settings may be achieved by adjusting sense resistors R7 to R9 and I_{SET} resistors R33 to R35. The default multiplication factor may be determined from curves in the data sheet. Low-current channels 4 (-12V) and 5 (-5V) are not protected by current-limit circuit breakers.

LATCH is set high by internal pull-up to configure the MAX5927A for latching fault management. If any of channels 1 to 3 experiences a fault, all channels will shut down until active-low CARD_PRESENT is cycled off and on.

Negative-Voltage Channels 4 and 5

The MAX5927A is designed to control positive-voltage circuits. However, ~4.2V of gate drive for the negative-voltage channels Q4 and Q5 is derived from the MAX5927A's GATE4 output, as modified by transistors Q5 and Q6, and resistors R4–R7.

Gate-charging current output at GATE4 is 60 μ A to 100 μ A, but is split to 30 μ A to 50 μ A in the symmetrical circuits R4–Q7 and R5–Q6. The voltage at GATE4 may be 5.3V above $V_{IN4(3.3V)}$ or $\leq +8.6V$ when on, and is ~0V when off. As $V_{Q6(BASE)} = V_{Q7(BASE)} = 3.3V$, $V_{Q6(EMITTER)} = V_{Q7(EMITTER)} \approx 3.9V$ when on, and 0V when off. Equal voltage drop across R4 and R5 creates an equal split in current through Q6 and Q7. Equal currents in R6 and R7 create equal gate drives for Q4 and Q5. Gate drive is 0V when GATE4 = 0V in the off condition. Q4 and Q5 turn off at a rate determined by the gate-discharge current through R6 and R7.

FET Selection

All channels, except the +12V channel, utilize n-channel MOSFET pass transistors in SOT23 packages; a maximum $R_{DS(ON)}$ at $V_{GS} = 4.5V$ and $T_J = +25^\circ C$ is listed on the schematic for each FET. A MOSFET with $V_{GS(max)} = 20V$ (Si9410) is used on the +12V channel.

Summary

The circuit meets all load and power-sequencing design requirements—handling three positive-voltage and two

negative-voltage channels with appropriate sequential turn-on timings, overcurrent trip points above the required minimums, and output slew rates at $\approx 1\text{V/ms}$, as designed.

+3.3V delay from +5V and +12V channels = 11.8ms (see **Figure 2**)

-5V delay from +3.3V channel = 16.2ms (see **Figure 3**)

-5V load turn-off time = 1ms (see **Figures 4 and 5**)

-12V load turn-off time = 4ns (see **Figures 6 and 7**)

-12V output-voltage slew rate $\approx 1\text{V/ms}$ (see **Figure 8**)

-12V load-capacitor charging current $\approx 80\text{mA}$ (see **Figure 9**)

-5V output-voltage slew rate $\approx 1\text{V/ms}$ (see **Figure 10**)

-5V load-capacitor charging current $\approx 55\text{mA}$ (see **Figure 11**)

+3.3V output-voltage slew rate $\approx 1\text{V/ms}$ (see **Figure 12**)

+3.3V load-capacitor charging current $\approx 400\text{mA}$ (see **Figure 12**)

+3.3V turn-on into 3A load without circuit-breaker trip (see **Figure 13**)

+3.3V circuit-breaker shutdown at 3.22A (see **Figure 14**)

+5V load-capacitor charging current $\approx 500\text{mA}$ (see **Figure 15**)

+5V output-voltage slew rate $\approx 1\text{V/ms}$ (see **Figure 15**)

+5V turn-on into 2.4A load without circuit-breaker trip (see **Figure 16**)

+5V circuit-breaker shutdown at 2.87A (see **Figure 17**)

+12V load-capacitor charging current is $\approx 500\text{mA}$ (see **Figure 18**)

+12V turn-on into 3A load without circuit-breaker trip (see **Figure 19**)

+12V circuit-breaker shutdown at 3.1A (see **Figure 20**)

+5V startup into short circuit at $\approx 4\text{A}$ (see **Figure 21**)

+12V startup into short circuit at $\approx 5.7\text{A}$ (see **Figure 22**)

Test Results

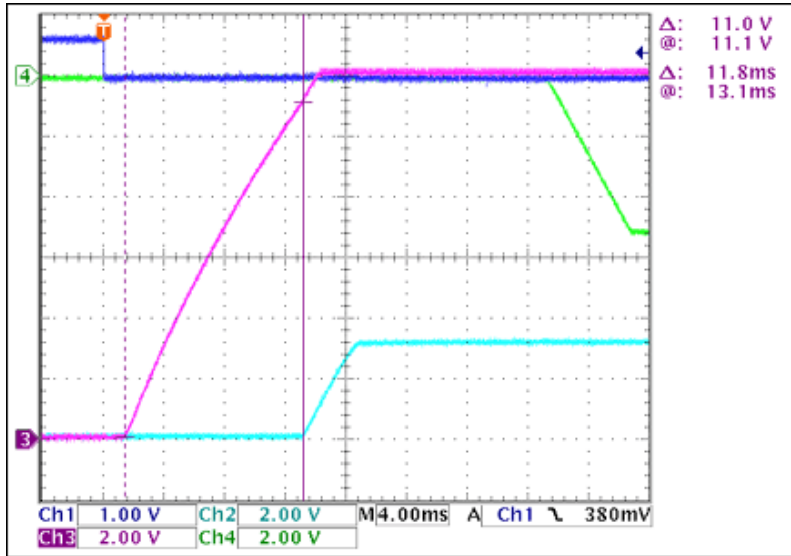


Figure 2. +12V to +3.3V turn-on delay, no load
 Ch1 = Q8BASE(CARD_PRESENT), Ch2 = +3.3V_{OUT}, Ch3 = +12V_{OUT}, Ch4 = -5V_{OUT}
 Note: 11.8ms delay between +12V_{OUT} and +3.3V_{OUT}.

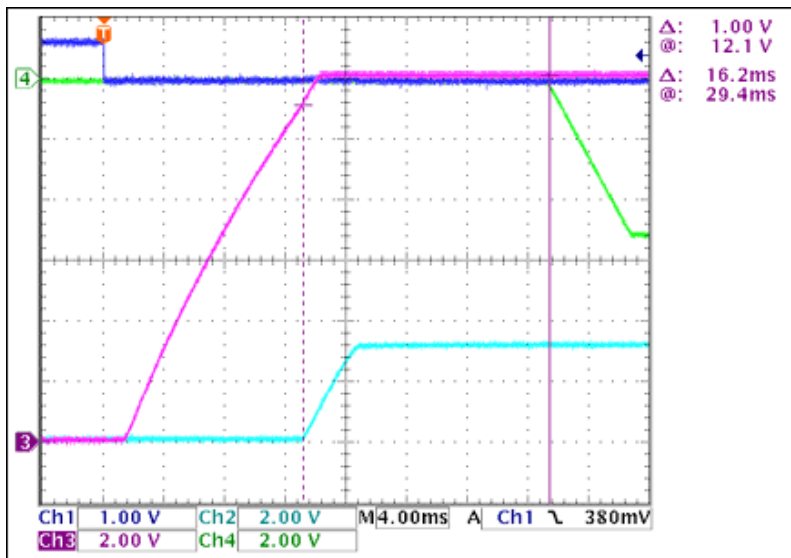


Figure 3. +3.3V to -5V turn-on delay, no load
 Ch1 = Q8BASE, Ch2 = +3.3V_{OUT}, Ch3 = +12V_{OUT}, Ch4 = -5V_{OUT}
 Note: 16.2ms delay between +3.3V_{OUT} and -5V_{OUT}.

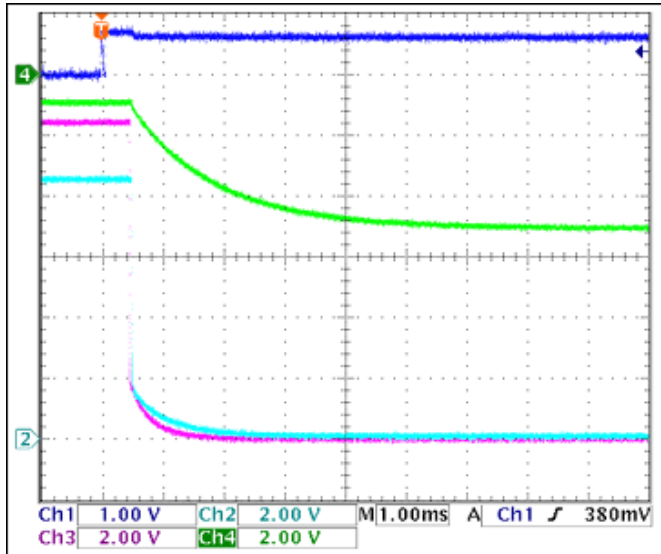


Figure 4. -5V gate turn-off in relation to +3.3V_{GATE}, no load

Ch1 = Q8_{BASE}, Ch2 = +3.3V_{GATE}, Ch3 = +5V_{GATE}, Ch4 = -5V_{GATE}

Note: -5V gate turn-off is slow; the FET is turned off when $1 < V_{GATE} < 3V$ (2.5V, typ). Thus, the -5V gate turn-off is complete about 1.5ms to 4ms after the positive-voltage channels are off.

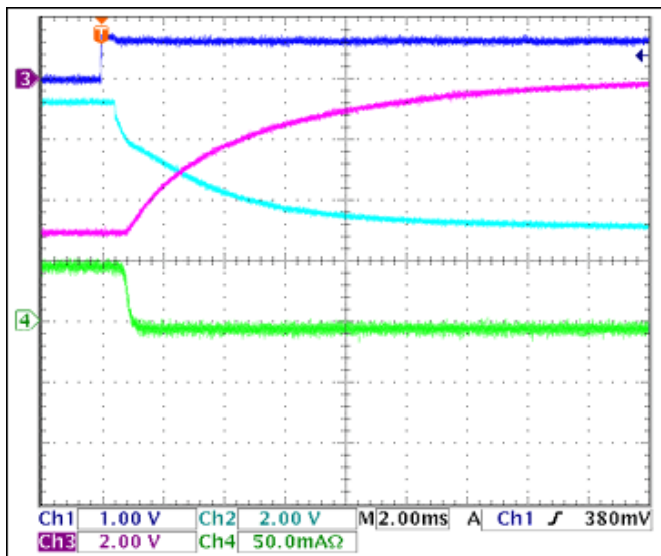


Figure 5. -5V load turn-off, 50mA load

Ch1 = Q8_{BASE}, Ch2 = -5V_{GATE}, Ch3 = -5V_{OUT}, Ch4 = IIN(-5V)

Note: The -5V input current drops to zero within 1ms, though $V_{OUT}(-5V)$ has not reached 0V due to output-capacitor discharge.

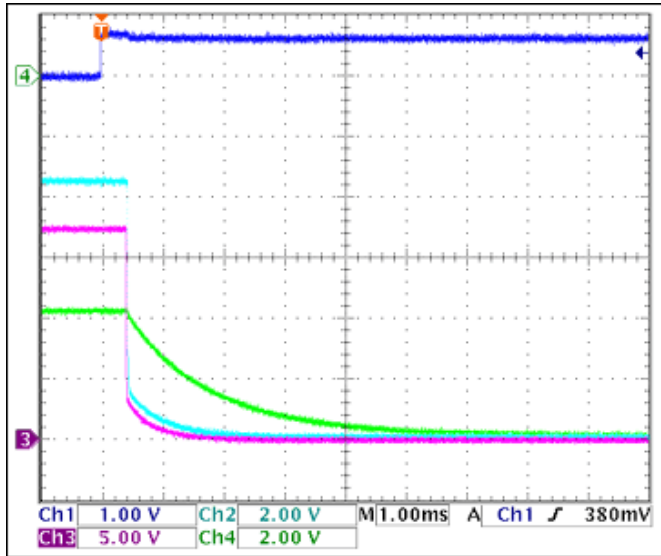


Figure 6. -12V gate turn-off, no load

Ch1 = Q8BASE, Ch2 = +3.3V_{GATE}, Ch3 = +12V_{GATE}, Ch4 = -12V_{GATE}

Note: -12V gate turn-off is slow; the FET is turned off when $1 < V_{GATE} < 3V$ (2.5V, typ). Thus, the -12V gate turn-off is complete about 1ms to 4ms after the positive-voltage channels are off.

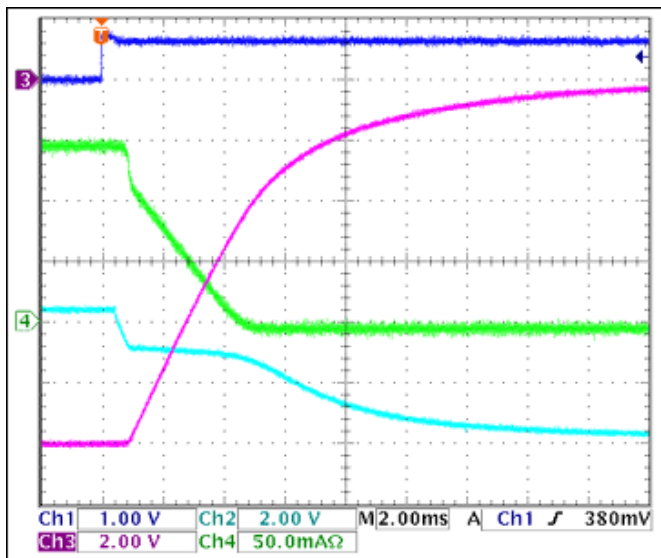


Figure 7. -12V load turn-off, 150mA load

Ch1 = Q8BASE, Ch2 = -12V_{GATE}, Ch3 = -12V_{OUT}, Ch4 = I_{IN(-12V)}

Note: The -12V input current drops to zero within 4ms, though V_{OUT(-12V)} has not reached 0V due to output-capacitor discharge.

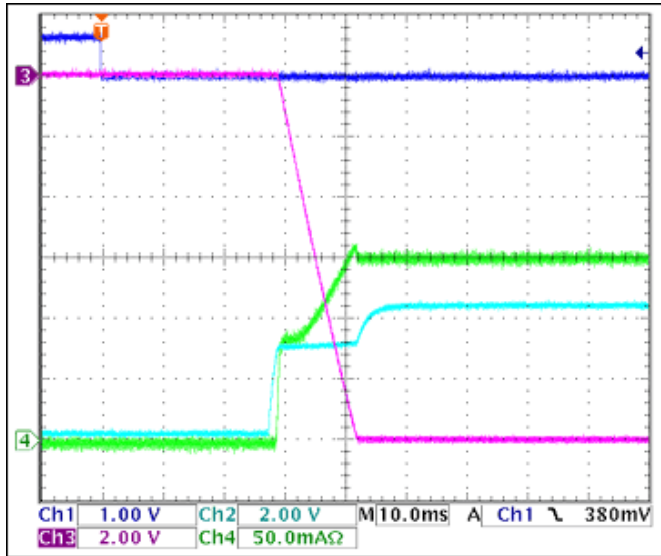


Figure 8. -12V turn-on waveforms
 Ch1 = Q8BASE, Ch2 = -12VGATE, Ch3 = -12VOUT, Ch4 = IIN(-12V)
 Note: Turn-on sequence, 80Ω resistive load = 150mA.

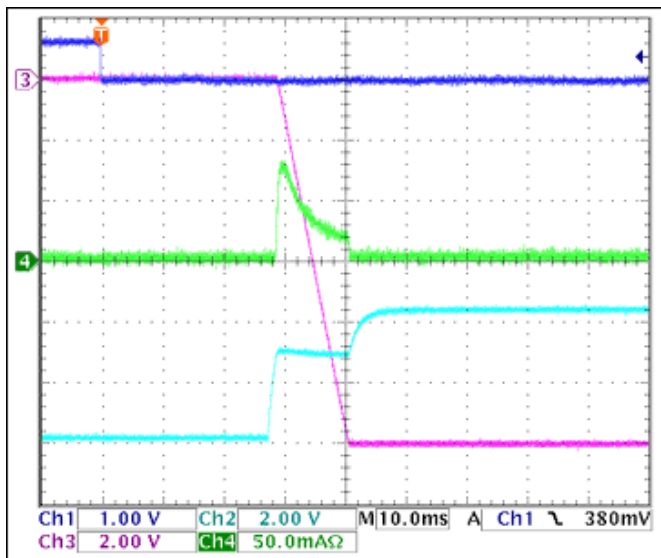


Figure 9. -12V turn-on waveforms, no load
 Ch1 = Q8BASE, Ch2 = -12VGATE, Ch3 = -12VOUT, Ch4 = IIN(-12V)
 Note: $I_{IN(PK)} = 80mA$ to charge output capacitor.

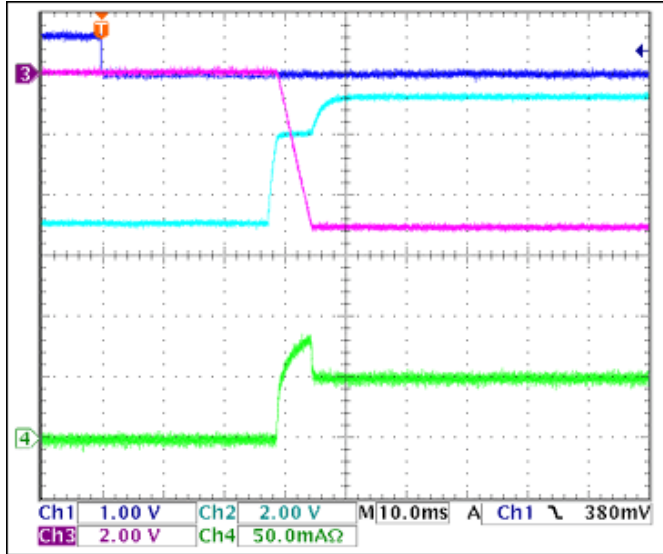


Figure 10. -5V turn-on waveforms, 100Ω resistive load = 50mA
 Ch1 = Q8BASE, Ch2 = -5VGATE, Ch3 = -5VOUT, Ch4 = IIN(-5V)
 Note: -5V slew rate is ~1V/ms.

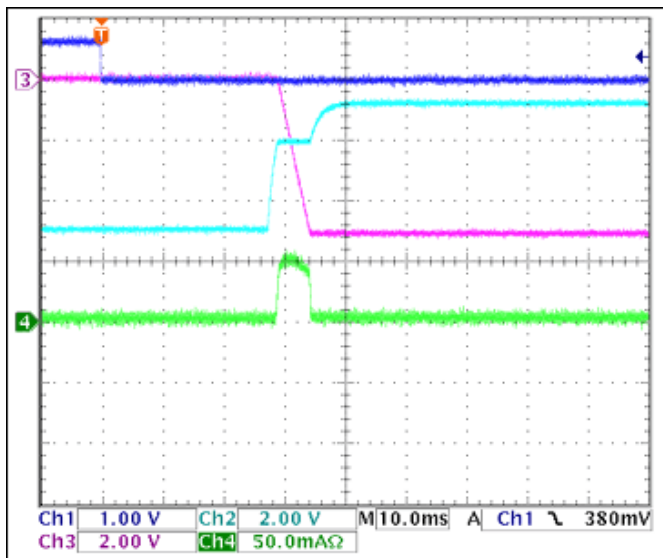


Figure 11. -5V turn-on waveforms, no load
 Ch1 = Q8BASE, Ch2 = -5VGATE, Ch3 = -5VOUT, Ch4 = IIN(-5V)
 Note: IIN(PK) = 55mA to charge output capacitor.

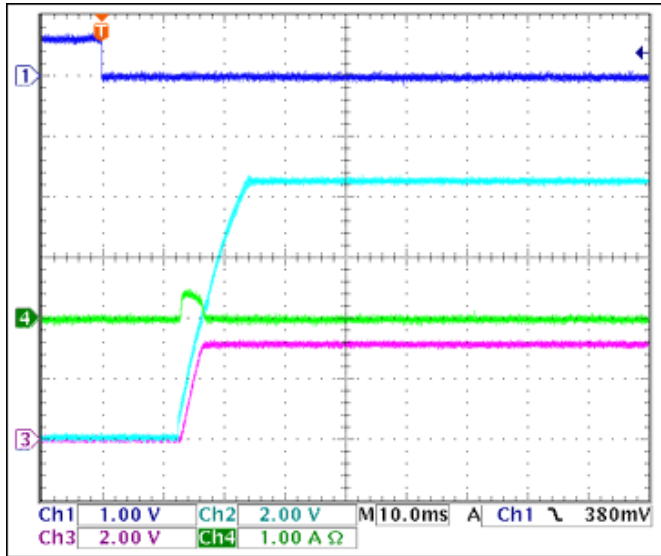


Figure 12. +3.3V turn-on waveforms, no load
 Ch1 = Q8_{BASE}, Ch2 = +3.3V_{GATE}, Ch3 = +3.3V_{OUT}, Ch4 = I_{IN(+3.3V)}
 Notes: I_{IN(PK)} = 400mA to charge output capacitor; +3.3V slew rate is ~1V/ms.

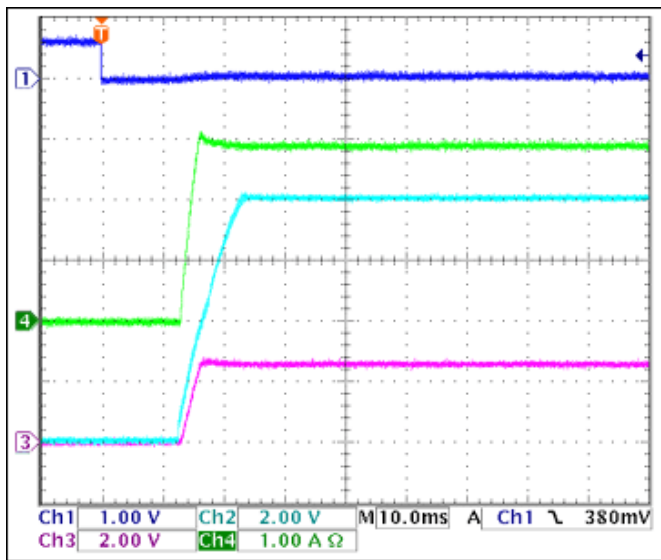


Figure 13. +3.3V turn-on waveforms, 1.1Ω load = 3A
 Ch1 = Q8_{BASE}, Ch2 = +3.3V_{GATE}, Ch3 = +3.3V_{OUT}, Ch4 = I_{IN(+3.3V)}

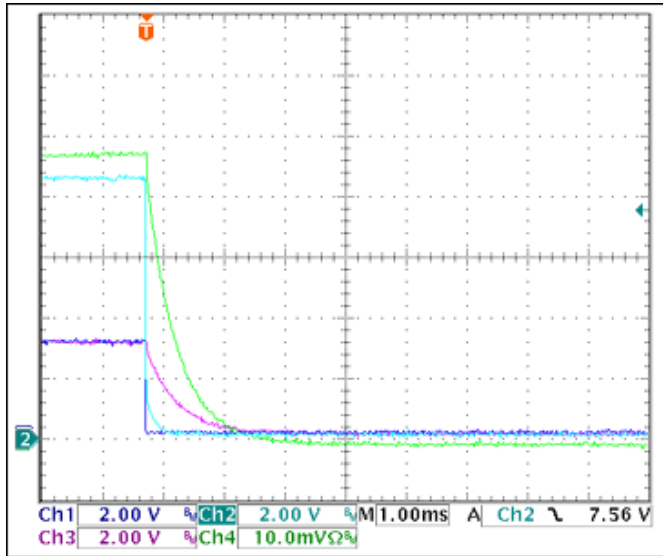


Figure 14. +3.3V overcurrent shutdown

Ch1 = STAT1, Ch2 = $V_{GATE} (+3.3V)$, Ch3 = $+3.3V_{OUT}$, Ch4 = $I_{OUT} (+3.3V)$ 0.5A/div

Notes: Rundown of I_{OUT} and V_{OUT} is due to output-capacitor discharge into a constant-resistance load. Measured trip current was 3.22A.*

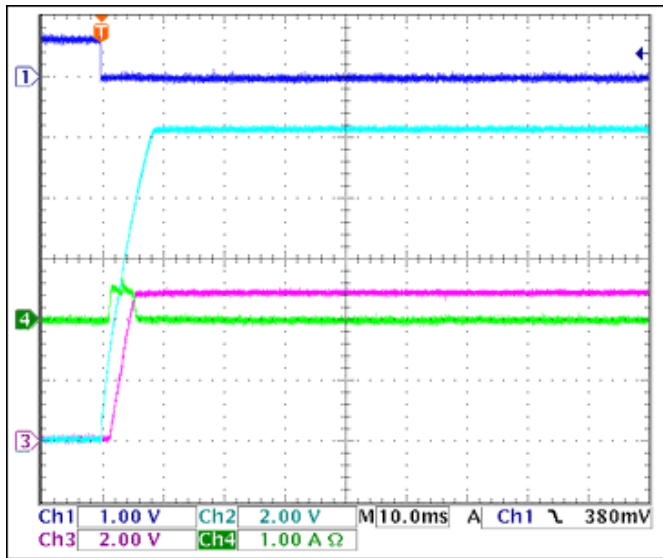


Figure 15. +5V turn-on load-capacitor charging current, no load

Ch1 = Q8BASE, Ch2 = $+5V_{GATE}$, Ch3 = $+5V_{OUT}$, Ch4 = $I_{IN} (+5V)$

Note: $I_{IN(PK)} = 500mA$ to charge output capacitor.

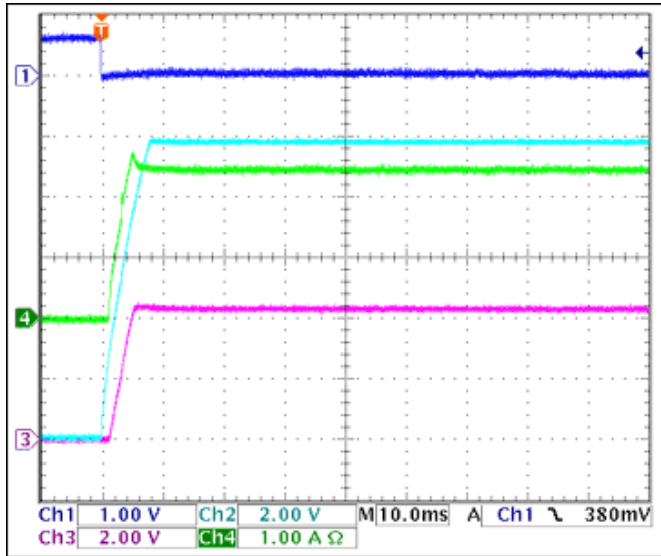


Figure 16. +5V turn-on current, 2.083Ω load = 2.4A
 Ch1 = Q8_{BASE}, Ch2 = +5V_{GATE}, Ch3 = +5V_{OUT}, Ch4 = $I_{IN(+5V)}$

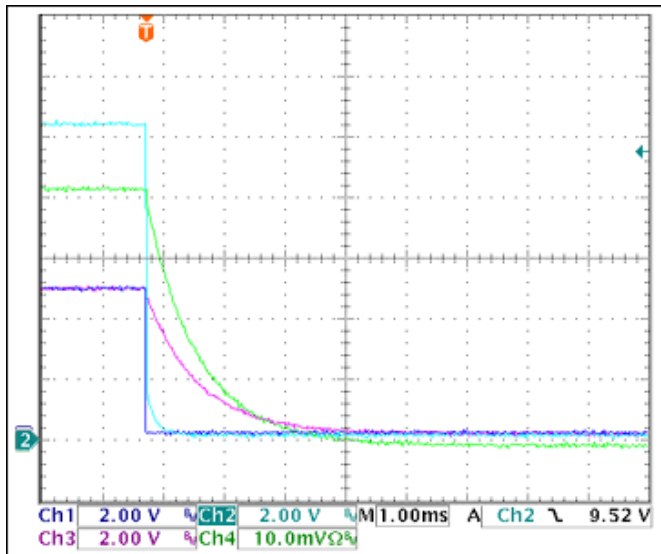


Figure 17. +5V overcurrent shutdown
 Ch1 = STAT2, Ch2 = V_{GATE} (+5V), Ch3 = +5V_{OUT}, Ch4 = $I_{OUT(+5V)}$ 0.5A/div
 Notes: Rundown of I_{OUT} and V_{OUT} is due to output-capacitor discharge into constant-resistance load. Measured current was 2.87A at trip.

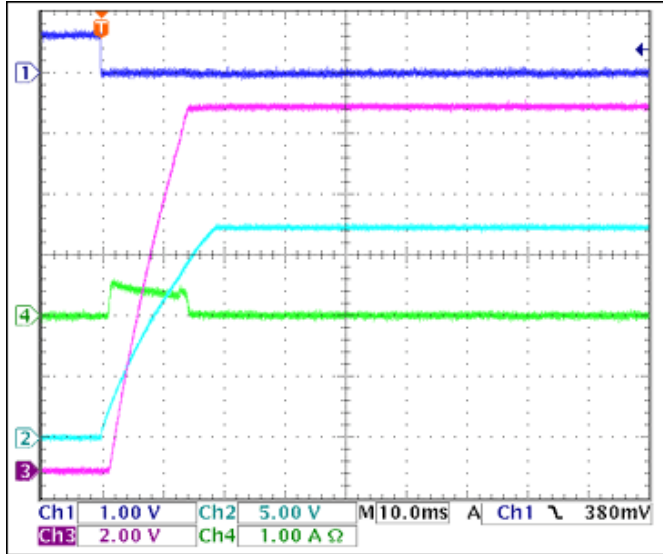


Figure 18. +12V startup current, no load
 Ch1 = Q8_{BASE}, Ch2 = +12V_{GATE}, Ch3 = +12V_{OUT}, Ch4 = $I_{IN(+12V)}$
 Note: $I_{IN(+12Vpk)} = 500mA$ to charge output capacitor.

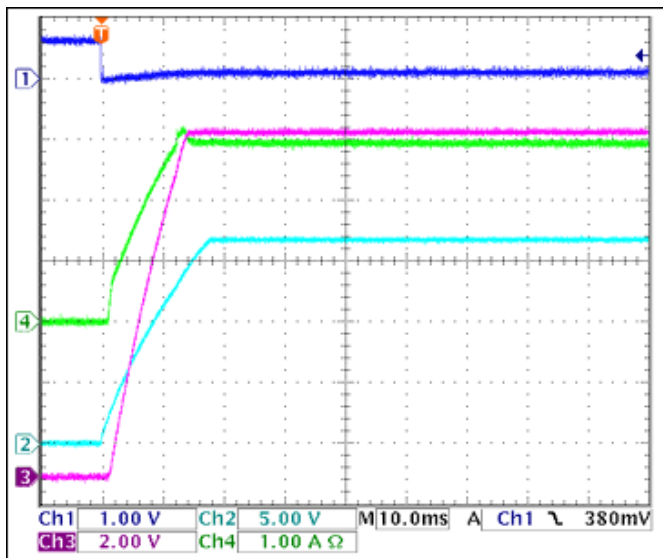


Figure 19. +12V turn-on current, 4Ω load = 3A
 Ch1 = Q8_{BASE}, Ch2 = +12V_{GATE}, Ch3 = +12V_{OUT}, Ch4 = $I_{IN(+12V)}$

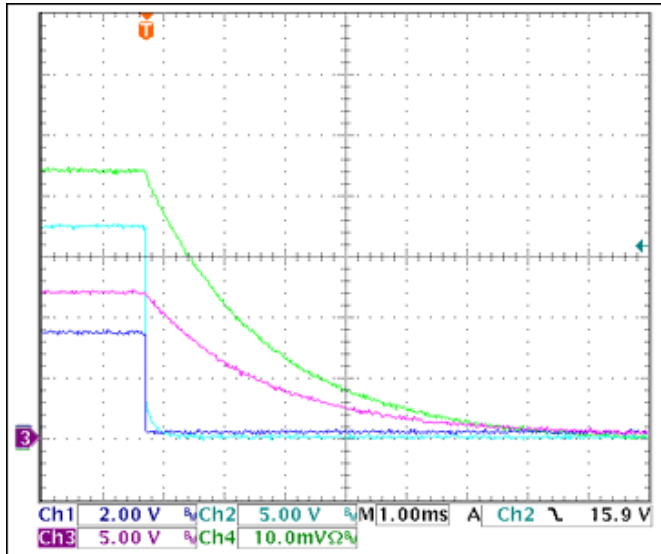


Figure 20. +12V overcurrent shutdown

Ch1 = STAT3, Ch2 = V_{GATE} (+12V), Ch3 = $+12V_{OUT}$, Ch4 = $I_{OUT} (+3.3V)$ 0.5A/div

Notes: Rundown of I_{OUT} and V_{OUT} is due to output-capacitor discharge into constant-resistance load. Measured current was 3.1A at trip.

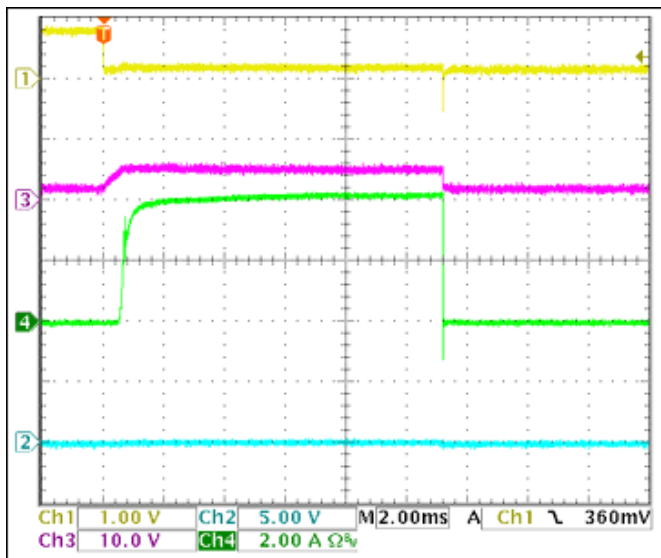


Figure 21. +5V startup current into short circuit

Ch1 = Q8BASE, Ch2 = $+5V_{OUT}$, Ch3 = $+5V_{GATE}$, Ch4 = $I_{IN} (+5V)$

Note: 4A load current at trip.

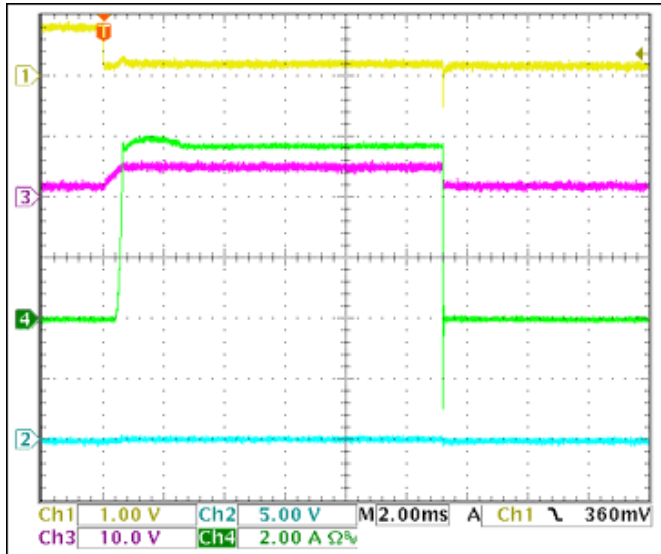
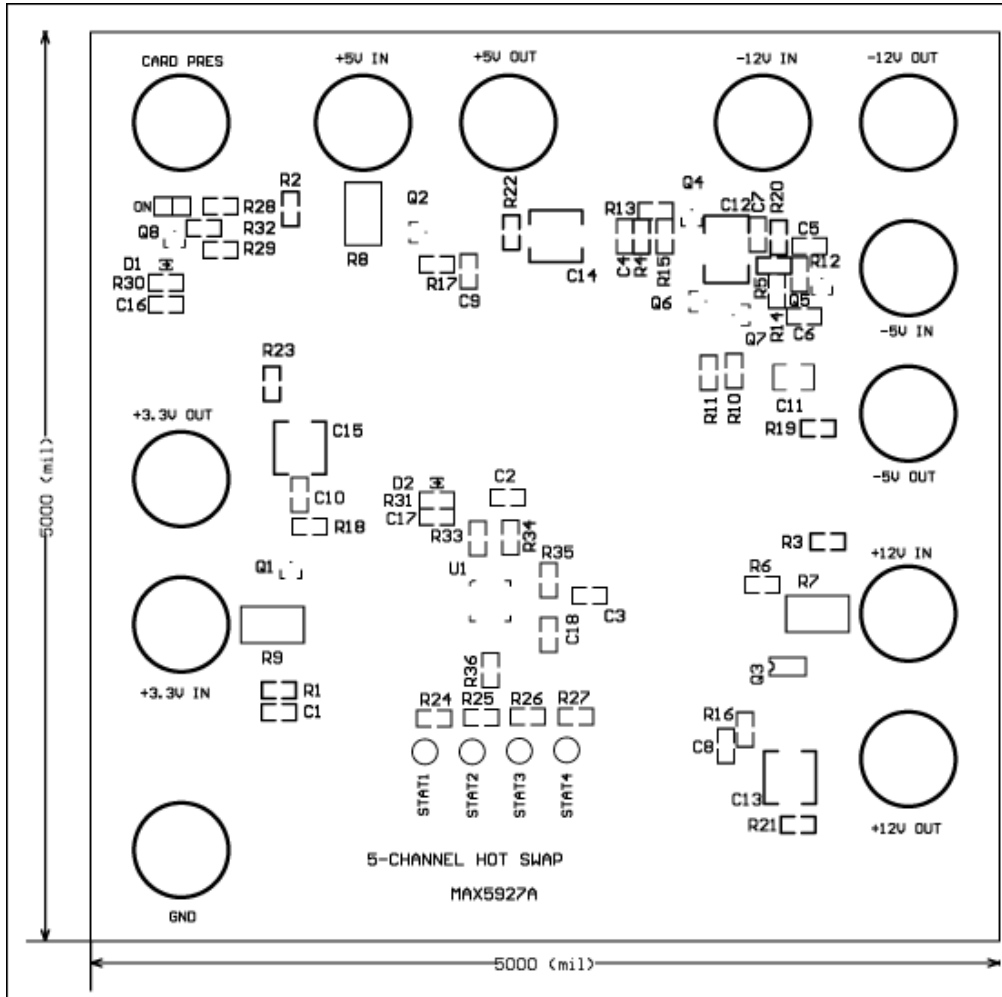


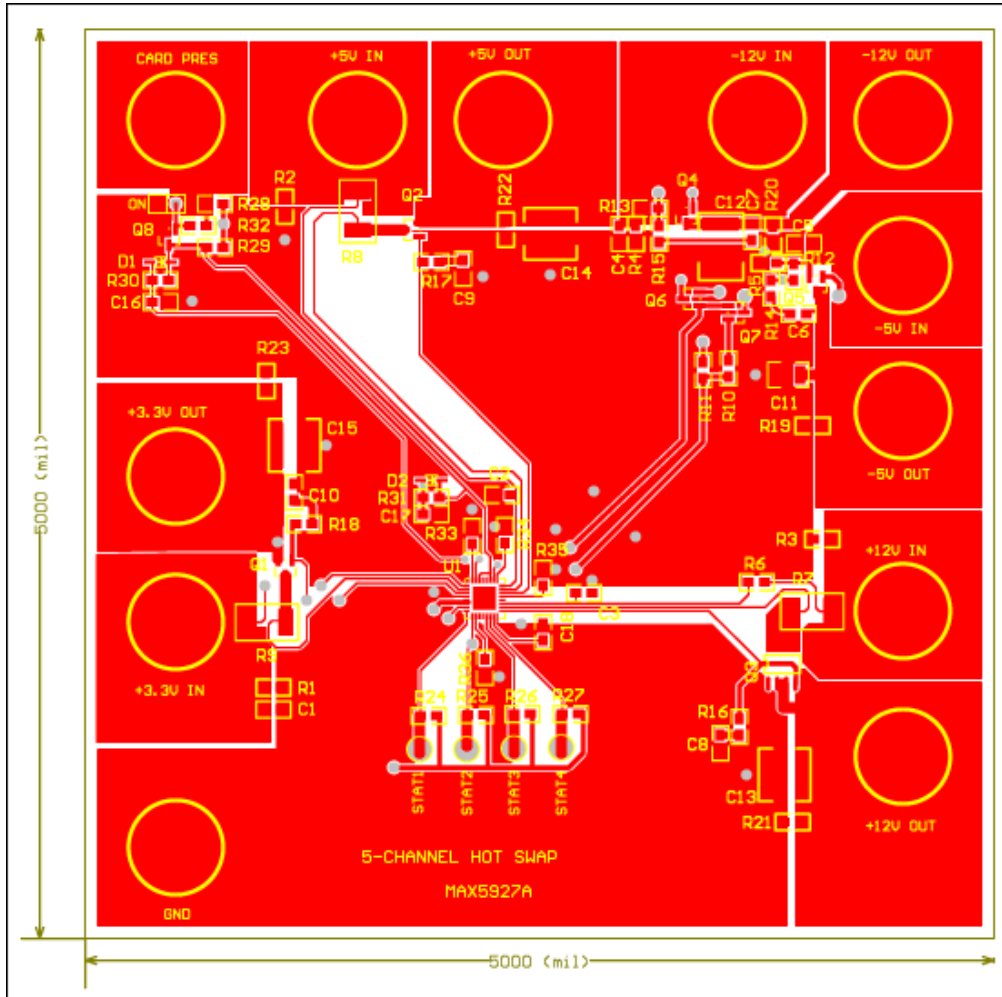
Figure 22. +12V startup current into short circuit
 Ch1 = Q8_{BASE}, Ch2 = V_{OUT}, Ch3 = V_{GATE}, Ch4 = I_{OUT}
 Note: 5.7A load current at trip.

Test PCB Layout



[More detailed image \(PDF, 237kB\)](#)

Figure 23. Parts placement on reference-design PCB.



More detailed image (PDF, 330kB)
 Figure 24. Top layer.

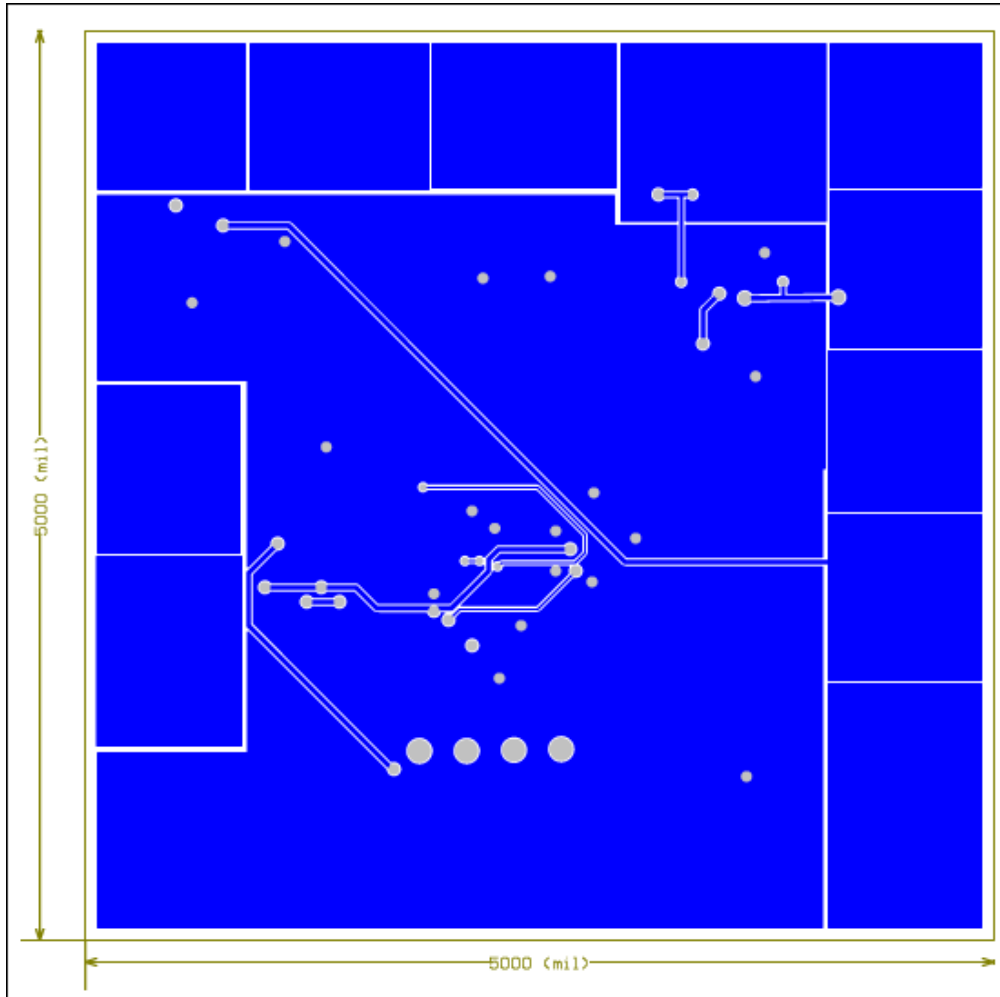


Figure 25. Bottom layer.

Bill of Materials

Qty	Designator	Description	Manufacturer and Part Number
5	C1, C2, C3, C4, C5	1 μ F \pm 10%, 25V X7R ceramic capacitors (0805)	—
3	C6, C7, C18	10nF \pm 10%, 25V X7R ceramic capacitors (0805)	—
1	C8	56nF \pm 10%, 25V X7R ceramic capacitor (0805)	—
1	C9	68nF \pm 10%, 25V X7R ceramic capacitor (0805)	—
1	C10	100nF \pm 10%, 25V X7R ceramic capacitor (0805)	—
1	C11	47 μ F \pm 20%, 6.3V X5R electrolytic capacitor (1210)	TDK C3225X5R0J476M
1	C12	100 μ F +80%, -20%; 16V Y5V ceramic capacitor (2220)	TDK C5750Y5V1C107Z

3	C13, C14, C15	470 μ F \pm 20%, 16V electrolytic capacitors	—
1	C16	15nF \pm 10%, 25V X7R ceramic capacitor (0805)	—
1	C17	33nF \pm 10%, 25V X7R ceramic capacitor (0805)	—
2	D1, D2	75V, 200mW silicon diodes (SOD-323)	Diodes Inc. MMBD4148WS
2	Q1, Q2	20V, 4.9A, 33m Ω n-channel MOSFETs (SOT23)	Vishay Si2314BDS
1	Q3	30V, 6.9A, 33m Ω n-channel MOSFET (8-SO)	Vishay Si9410BDY
2	Q4, Q5	30V, 4A, 47m Ω n-channel MOSFETs (SOT23)	Vishay Si2306BDS
2	Q6, Q7	60V, 800mA bipolar PNP transistors (SOT23)	Fairchild MMBT2907
1	Q8	40V, 1A bipolar NPN transistor (SOT23)	Fairchild MMBT2222A
10	R1, R2, R3, R4, R5, R24, R25, R26, R27, R32	100k Ω \pm 5%, 1/16W thick-film resistors (0805)	—
1	R6	1 Ω \pm 5%, 1/16W thick-film resistor (0805)	—
2	R7, R9	0.008 Ω \pm 1%, 1/4W thick-film resistors (2512)	—
1	R8	0.010 Ω \pm 1%, 1/4W thick-film resistor (2512)	—
2	R10, R11	90.9k Ω \pm 1%, 1/16W thick-film resistors (0805)	—
2	R12, R13	133k Ω \pm 1%, 1/16W thick-film resistors (0805)	—
2	R14, R15	15k Ω \pm 1%, 1/16W thick-film resistors (0805)	—
3	R16, R17, R18	4.7k Ω \pm 1%, 1/16W thick-film resistors (0603)	—
5	R19, R20, R21, R22, R23	10k Ω \pm 5%, 1/16W thick-film resistors (0805)	—
1	R28	20k Ω \pm 5%, 1/16W thick-film resistor (0805)	—
2	R29, R36	100k Ω \pm 1%, 1/16W thick-film resistors (0805)	—
2	R30, R31	910k Ω \pm 1%, 1/16W thick-film resistors (0805)	—
2	R33, R35	1.15k Ω \pm 1%, 1/16W thick-film resistors (0805)	—
1	R34	1.18k Ω \pm 1%, 1/16W thick-film resistor (0805)	—
1	U1	Quad hot-swap controller IC, 32-TQFN-EP	Maxim MAX5927AETJ

*Note that the particular current probe used in Figures 14, 17, and 20 shows only about 72% of true value. Circuit-breaker currents were measured using an adjustable constant-current load and noting the point where shutdown occurred.

Related Parts

[MAX5927](#)

Low-Voltage, Quad, Hot-Swap Controllers/Power Sequencers

[Free Samples](#)

More Information

For Technical Support: <http://www.maximintegrated.com/support>

For Samples: <http://www.maximintegrated.com/samples>

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Application Note 4228: <http://www.maximintegrated.com/an4228>

REFERENCE DESIGN 4228, AN4228, AN 4228, APP4228, Appnote4228, Appnote 4228

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