

MLX92255LSE

Dual Hall Effect Latch with two Speed Outputs

1. Features and Benefits

- Operating Voltage from 2.7V to 5.5V
- Two Integrated Hall plates for Direction Detection
- Latching Magnetic Characteristics
- Feedback loop during power-on

2. Application Examples

- Windows lifter with Anti-Pinch feature
- Rotation speed & direction detection
- Linear speed & direction detection
- Angular position detection
- Power closures with Anti-Pinch features

3. Description

The Melexis MLX92255 is a second generation Hall-effect dual latch designed in mixed signal CMOS technology. The device integrates a voltage regulator, two Hall sensors with advanced offset cancellation system and two open-drain output drivers, all in a single package.

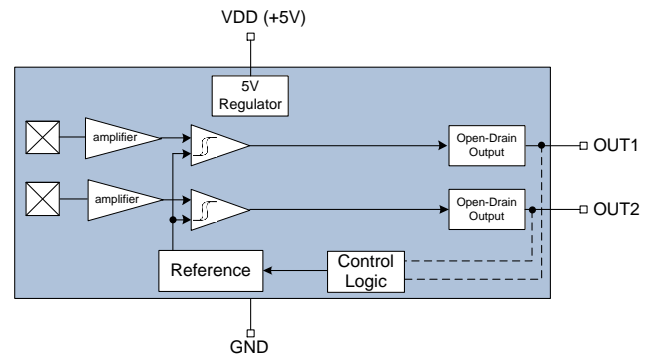
Two Hall plates are integrated on the same piece of silicon, thus using the high precision of the wafer fabrication process to ensure a fixed spacing of 1.45mm between the sensing elements.

With latching magnetic characteristics, both speed outputs (OUT1, OUT2) are turned low or high respectively with a sufficiently strong South or North pole facing the package top side. When removing the magnetic field, the device keeps its previous state.

During Startup communication with the IC is possible to load the previous state into the registers of our IC. This will then be used as a starting point.

The MLX92255 is delivered in a Green compliant 5-pin Thin Small Outline Transistor (TSOT) for surface-mount process.

The block diagram is shown on Figure 1.



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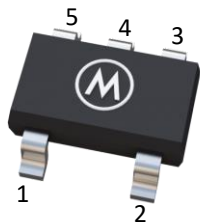
4. Ordering Information

Product	Temperature	Package	Option Code	Packing Form	Definition
MLX92255LSE	L	SE	AAA-001	RE	Sensitivity ±3mT

5. Glossary of Terms

Abbreviation	Description
TC	Temperature Coefficient [ppm/°C]
Gauss (G), Tesla (T)	Units for the magnetic flux density – 1 mT = 10 G
RoHS	Restriction of Hazardous Substances
TSOT	Thin Small Outline Transistor (TSOT package) – also referred with the Melexis package code “SE”
ESD	Electro-Static Discharge

6. Pin Definitions and Descriptions



Pin #	Name	Description
1	OUT1	Open-Drain Output 1
2	OUT2	Open-Drain Output 2
3	VDD	Power Supply
4	GND	Ground pin
5	GND	Ground pin

7. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{DD}	-0.5		6	V
Supply Current ⁽¹⁾	I _{DD}	-20		20	mA
Output Voltage	V _{OUT}	-0.5		6	V
Output Current ⁽¹⁾	I _{OUT}	-20		20	mA
Operating Temperature Range	T _A	-40		150	°C
Maximum Junction Temperature	T _J			165	°C
ESD Sensitivity – HBM ⁽²⁾	-			8	kV
ESD Sensitivity – CDM ⁽³⁾	-			1000	V
Magnetic Flux Density	B			Unlimited	mT

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

¹ Including current through the protection structure. Max Power dissipation should be also considered

² Human Body Model according AEC-Q100-002 standard

³ Charged Device Model according AEC-Q100-011 standard

8. General Electrical Specifications

DC Operating Parameters $T_A = -40^{\circ}\text{C}$ to 150°C , $V_{DD} = 2.7\text{V}$ to 5.5V (unless otherwise specified)

Electrical Parameter	Symbol	Min.	Typ. ⁽¹⁾	Max.	Unit	Condition
Supply Voltage	V_{DD}	2.7	-	5.5	V	Operating
Supply Current	I_{DD}	3	5	7	mA	
Output Leakage Current	I_{OFF}		0.001	5	μA	$V_{OUT} = 5.5\text{V}$, $B < B_{RP}$
Output Saturation Voltage	V_{OUTS}		0.15	0.4	V	$B > B_{OP}$, $I_{OUT} = 5\text{mA}$
Output Rise/Fall Time ^(2,3)	t_R / t_F		0.3		μs	$V_{DD} = 5\text{V}$, $V_{PU}^{(4)} = 5\text{V}$, $R_{PU} = 1\text{k}\Omega$, $C_L = 50\text{pF}$
Chopping Frequency	f_{CHOP}		500		kHz	
Output Refresh Period	t_{PER}		4	6	μs	
Output Jitter (p-p value) ⁽²⁾	t_{JITTER}		4.8		μs	Over 1000 successive output switching events @10kHz triangle wave, $B_{PEAK}=30\text{mT}$
Maximum Switching Frequency ^(2,5)	f_{SW}	40	66		kHz	$\geq 10\text{mT}$ triangle wave magnetic field
Power-On Reset Voltage ⁽⁶⁾	V_{POR}		2.5	2.6	V	
Power-On Time ⁽⁷⁾	t_{PON}		20	40	μs	$V_{DD} = 5\text{V}$, $dV_{DD}/dt > 2\text{V}/\mu\text{s}$
Input High Voltage ⁽⁸⁾	V_{IH}	2.0	-	5.5	V	
Input Low Voltage ⁽⁸⁾	V_{IL}	-	-	0.8	V	
SE Package Thermal Resistance	R_{THJA}		300		$^{\circ}\text{C}/\text{W}$	Single layer (1S) JEDEC board

1 Typical values are defined at $T_A = +25^{\circ}\text{C}$ and $V_{DD} = 5\text{V}$

2 Guaranteed by design and verified by characterization, not production tested

3 Measured between $0.1 \cdot V_{PU}$ and $0.9 \cdot V_{PU}$

4 R_{PU} and V_{PU} are respectively the external pull-up resistor and pull-up power supply

5 Maximum switching frequency corresponds to the maximum frequency of the applied magnetic field which is detected without loss of pulses

6 If V_{DD} drops below V_{POR} the output is reset to High state

7 The Power-On Time represents the time from reaching $V_{DD} = 2.7\text{V}$ to the first refresh of the outputs

8 Applicable for OUT1 and OUT2 during start-up

9. Magnetic Specifications

9.1. MLX92255LSE-AAA-001

DC Operating Parameters $T_A = -40^{\circ}\text{C}$ to 150°C , $V_{DD} = 2.7\text{V}$ to 5.5V (unless otherwise specified)

Parameter	Symbol	Min.	Typ. ⁽¹⁾	Max.	Unit	Condition
Operating Point	B_{OP}	0.5	3.0	5.5	mT	
Release Point	B_{RP}	-5.5	-3.0	-0.5	mT	
Hysteresis ⁽²⁾	B_{HYST}	3	6	10	mT	$T_A = -40^{\circ}\text{C}$ to 150°C
		4	6	10	mT	$T_A = -40^{\circ}\text{C}$ to 55°C
Magnetic Matching	B_{MATCH}	-2		2	mT	$B_{OP1} - B_{OP2}$ or $B_{RP1} - B_{RP2}$, $T_A = 25^{\circ}\text{C}$
		-3		3	mT	$B_{OP1} - B_{OP2}$ or $B_{RP1} - B_{RP2}$
Magnetic Offset	B_{OFF}	-2		2	mT	$(B_{OP1} + B_{RP1}) / 2$, $(B_{OP2} + B_{RP2}) / 2$
Temperature Coefficient ⁽³⁾	TC		-1800		ppm/ $^{\circ}\text{C}$	
Hall Sensors Spacing	-		1.45		mm	

10. Output Behavior versus Magnetic Pole

DC Operating Parameters $T_A = -40^{\circ}\text{C}$ to 150°C , $V_{DD} = 2.7\text{V}$ to 5.5V (unless otherwise specified)

Parameter	Output State	Condition
South pole	Low	$B > B_{OP}$
North pole	High ⁽⁴⁾	$B < B_{RP}$

Output behavior versus magnetic pole⁽⁵⁾

¹ Typical values are defined at $T_A = +25^{\circ}\text{C}$ and $V_{DD} = 5\text{V}$

² Guaranteed by design and verified by characterization, not production tested

³ Temperature coefficient value is guaranteed by design and verified by characterization and is calculated using the following formula:

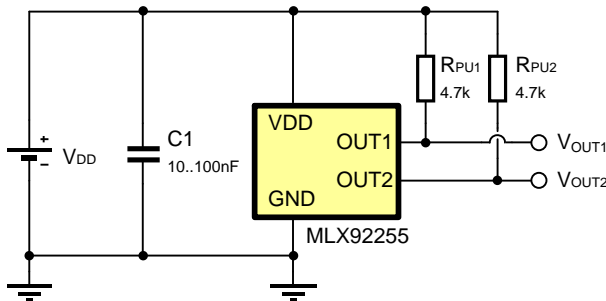
$$\frac{B_{T_2} - B_{T_1}}{B_{25^{\circ}\text{C}} \times (T_2 - T_1)} \times 10^6, \left[\frac{\text{ppm}}{^{\circ}\text{C}} \right]; T_1 = -40^{\circ}\text{C}; T_2 = 150^{\circ}\text{C}$$

⁴ Default output state during power-up

⁵ Magnetic pole applied perpendicularly to Hall plate, facing the branded/top side of the package

11. Application Information

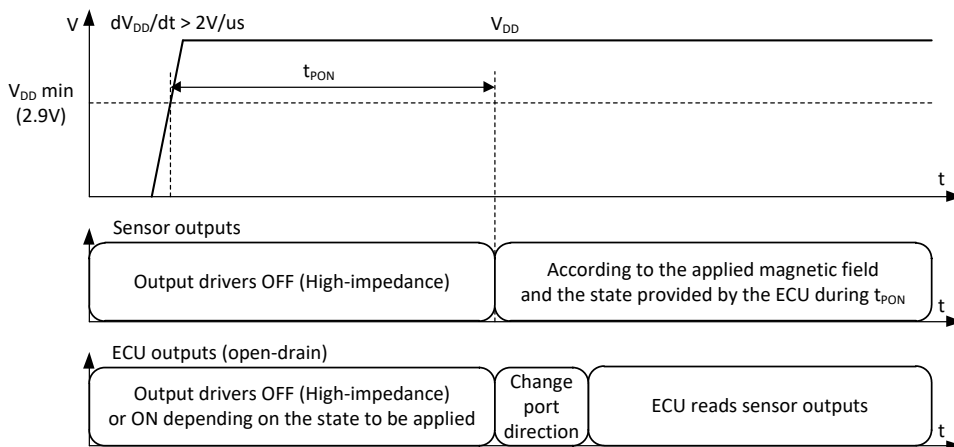
11.1. Default Application Schematic



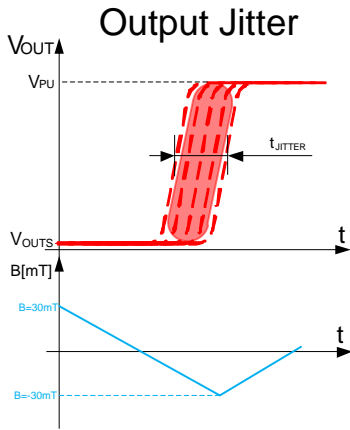
Note:

1. For proper operation, a 10nF to 100nF bypass capacitor should be placed as close as possible to the V_{DD} and ground pin.

11.2. Start-up procedure



11.3. Output Jitter



12. Standard Information

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Developments)

- IPC/JEDEC J-STD-020
Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Developments) and THD's (Through Hole Developments)

- EN60749-20
Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Developments)

- EN60749-15
Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Developments) and THD's (Through Hole Developments)

- EIA/JEDEC JESD22-B102 and EN60749-21
Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: <http://www.melexis.com/quality.aspx>

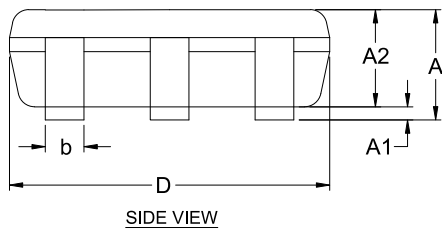
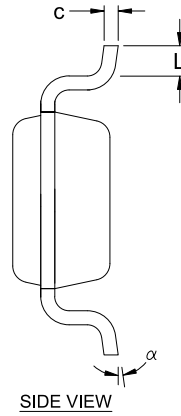
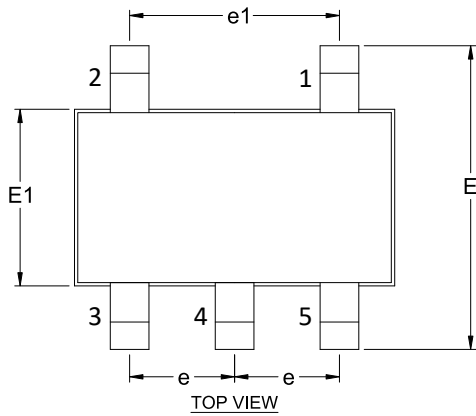
13. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).

Always observe Electro Static Discharge control procedures whenever handling semiconductor products

14. TSOT-5L (SE) Package Information

14.1. TSOT-5L – Package dimensions

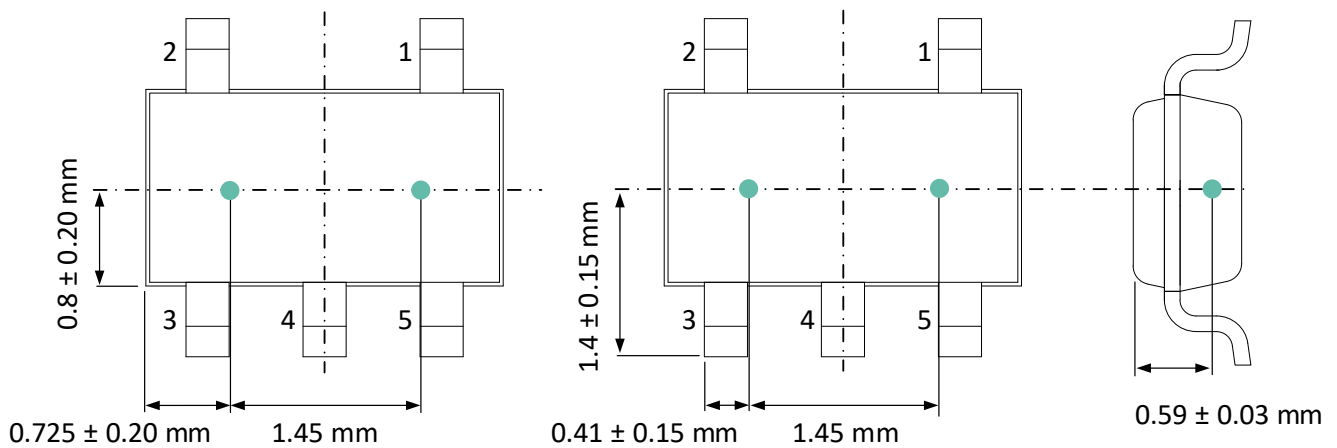


SYMBOL	MINIMUM	MAXIMUM
A	---	1.00
A1	0.025	0.10
A2	0.85	0.90
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
L	0.30	0.50
b	0.30	0.45
c	0.10	0.20
e	0.95 BSC	
e1	1.90 BSC	
α	0°	8°

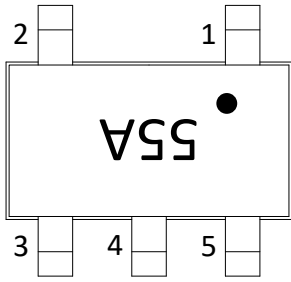
NOTE :

1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.07 mm.
5. DIMENSION L IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.076 mm SEATING PLANE.

14.2. TSOT-5L – Sensitive spots

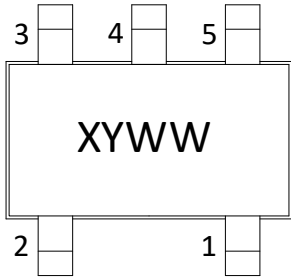


14.3. TSOT-5L – Package marking

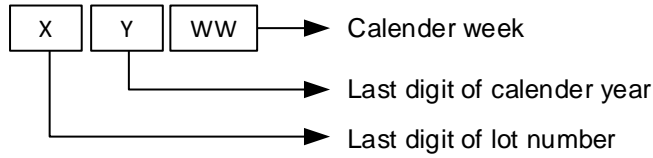


Top

55A → MLX92255LSE-AAA-001



Bottom



15. Contact

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