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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

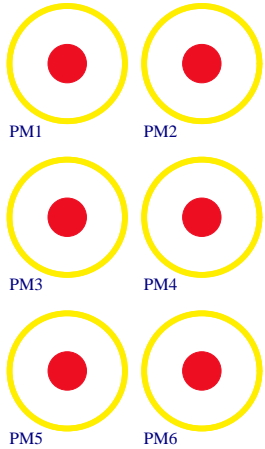
U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

LOGO1
TE Logo PRINT Layer
LOGO PRINT



Serial
Serialnumber 6,3 x 6.3mm



Title: TE0782 - Overview		
A4	Number: TE0782 82133FA	Rev. 02
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Filename: TE0782.SchDoc		

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U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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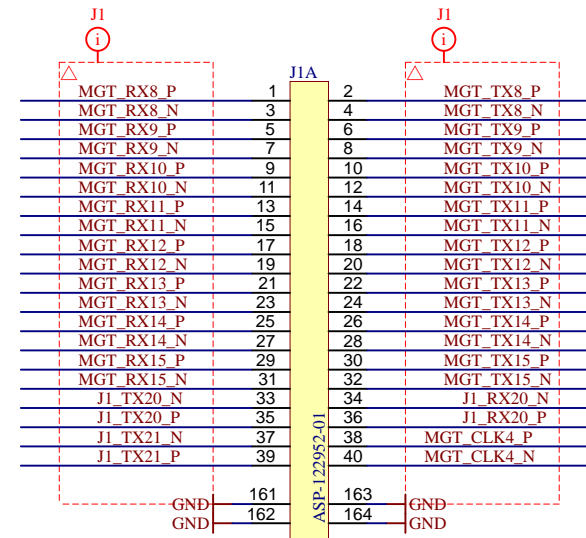
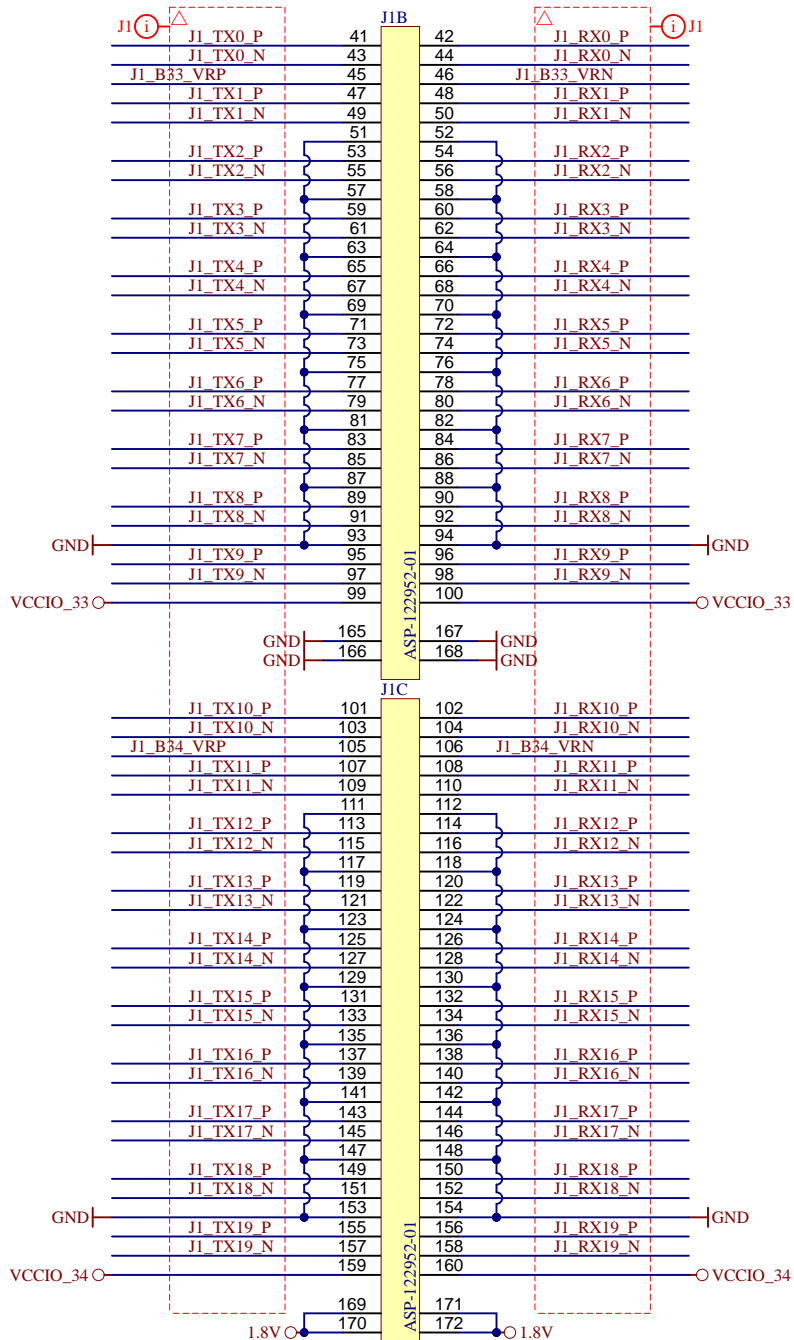

		Title: TE0782 - Connectors	
		A4	Number: TE0782 82I33FA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: Connectors.SchDoc		Page2 of 31	

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Title: TE0782 - HSMC_Connector_J1		
A4	Number: TE0782 82133FA	Rev. 02
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Filename: HSMC_CONN_J1.SchDoc		

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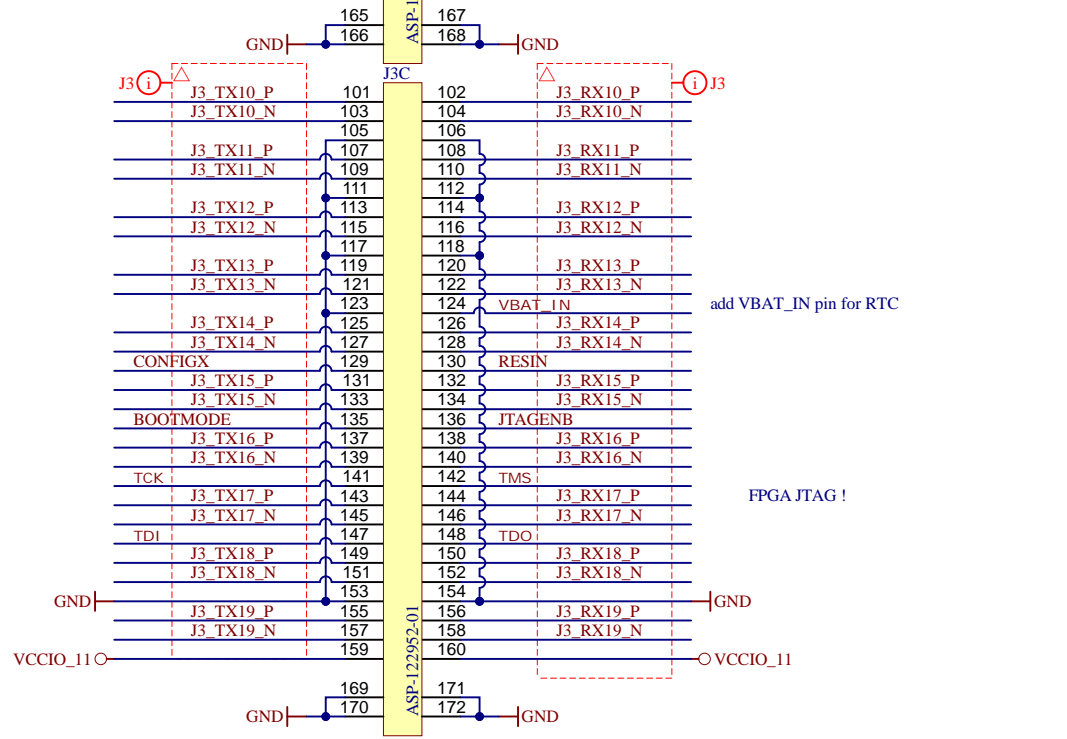
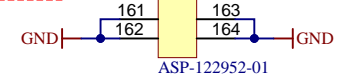
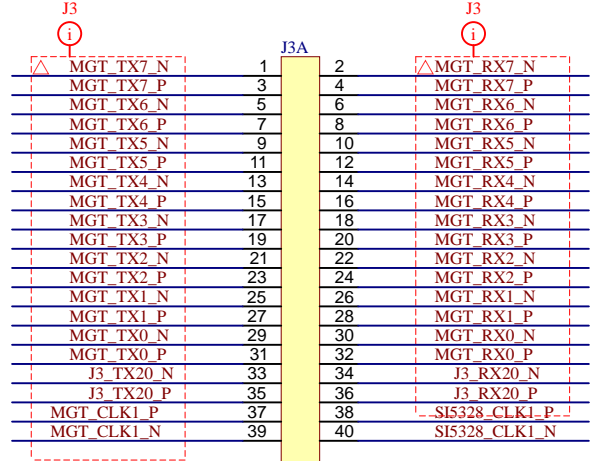
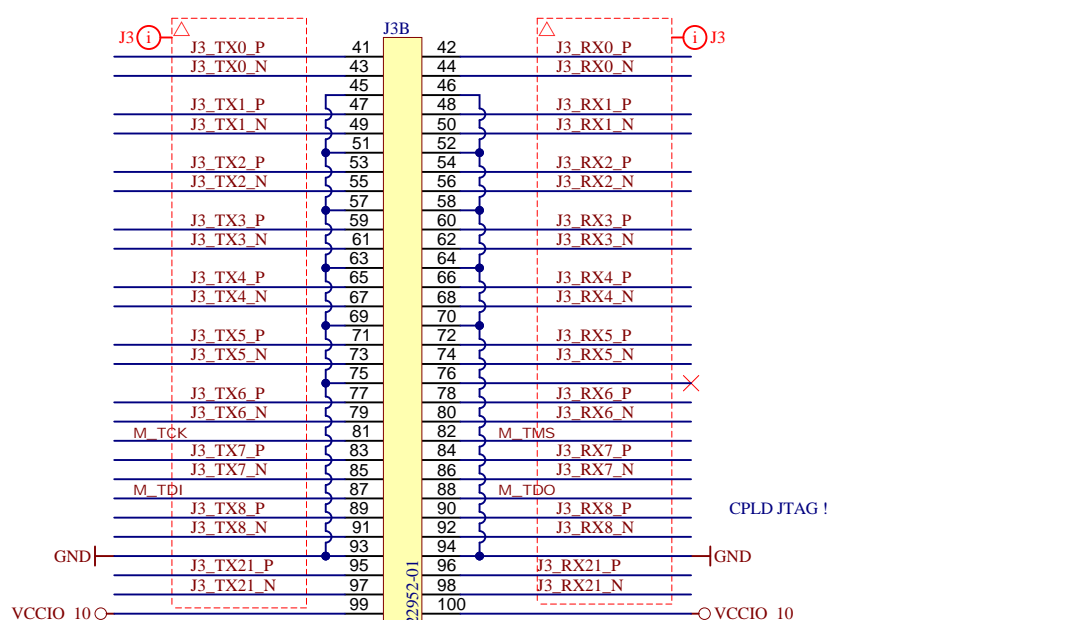
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Title: TE0782 - HSMC_Connector_J3		
A4	Number: TE0782 82I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 4 of 31
Filename: HSMC_CONN_J3.SchDoc		

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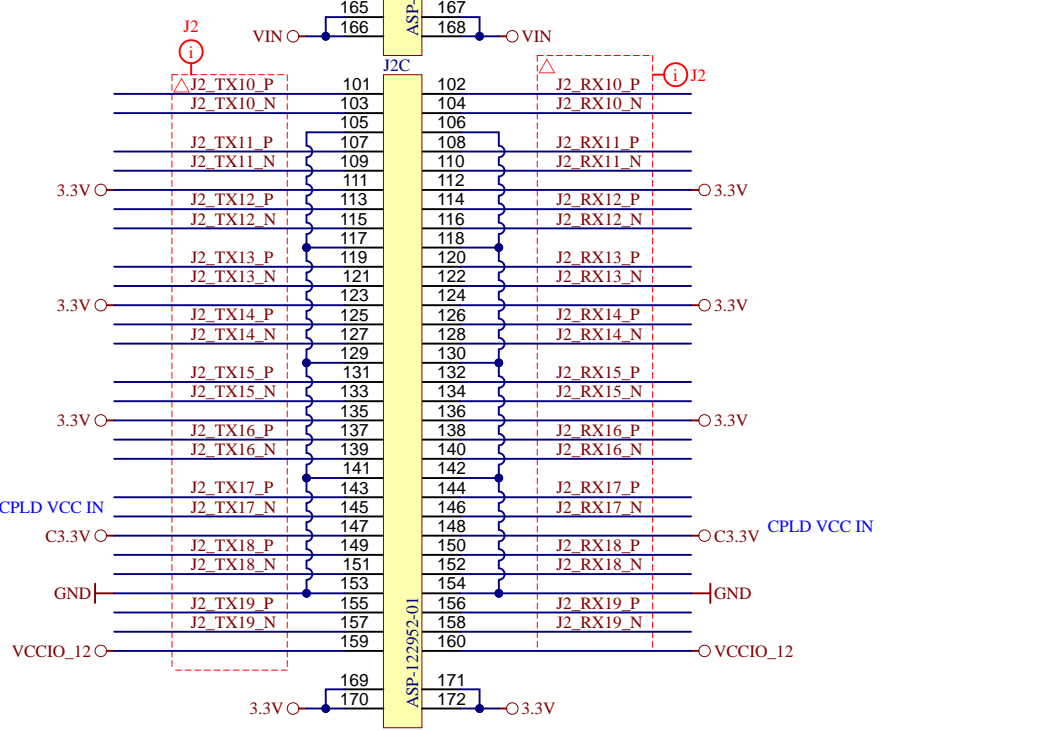
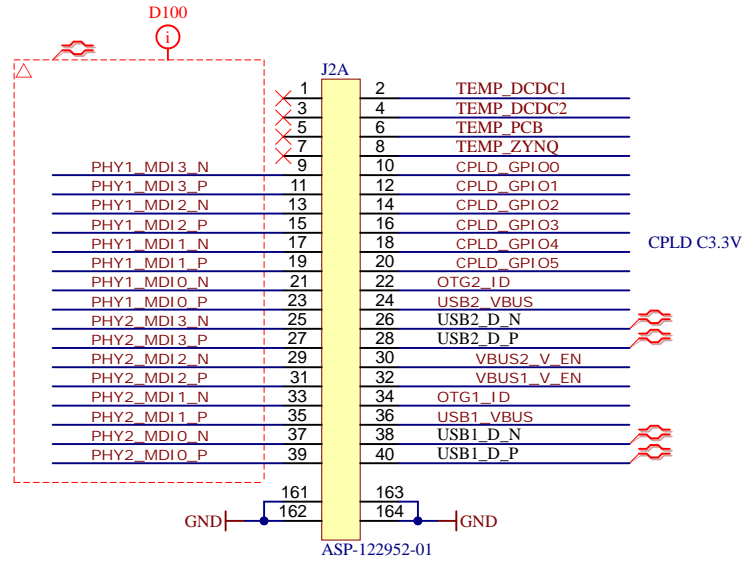
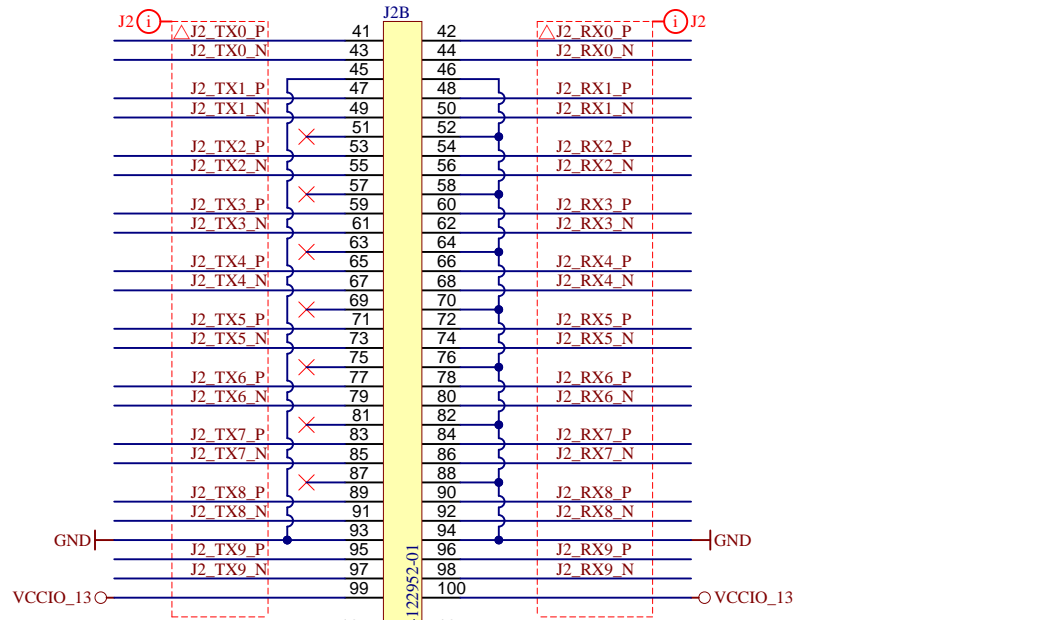
B

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Title: TE0782 - HSMC_Connector_J2		
A4	Number: TE0782 82I33FA	Rev. 02
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U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



U_FPGA-PWR
FPGA-PWR.SchDoc



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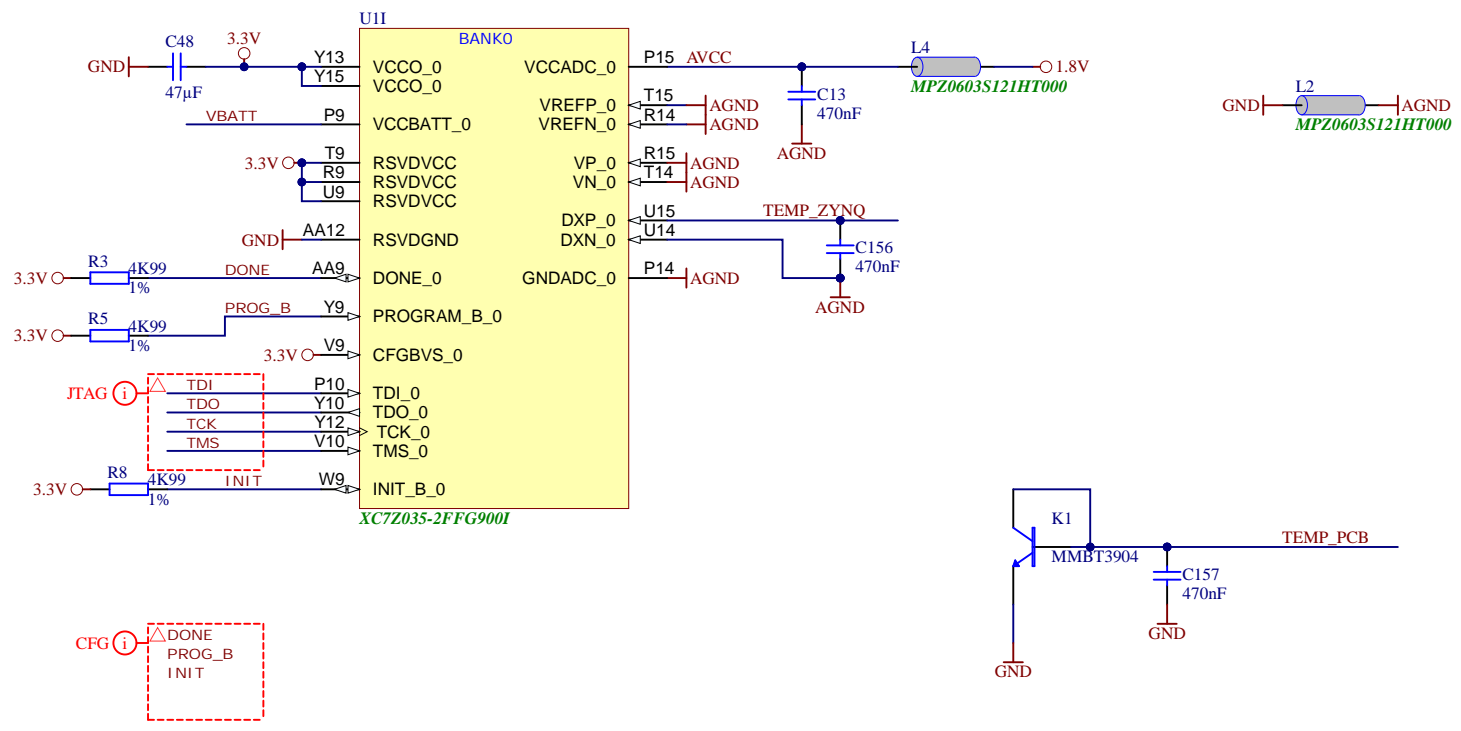
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Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page6 of 31
Filename: SOC.SchDoc				


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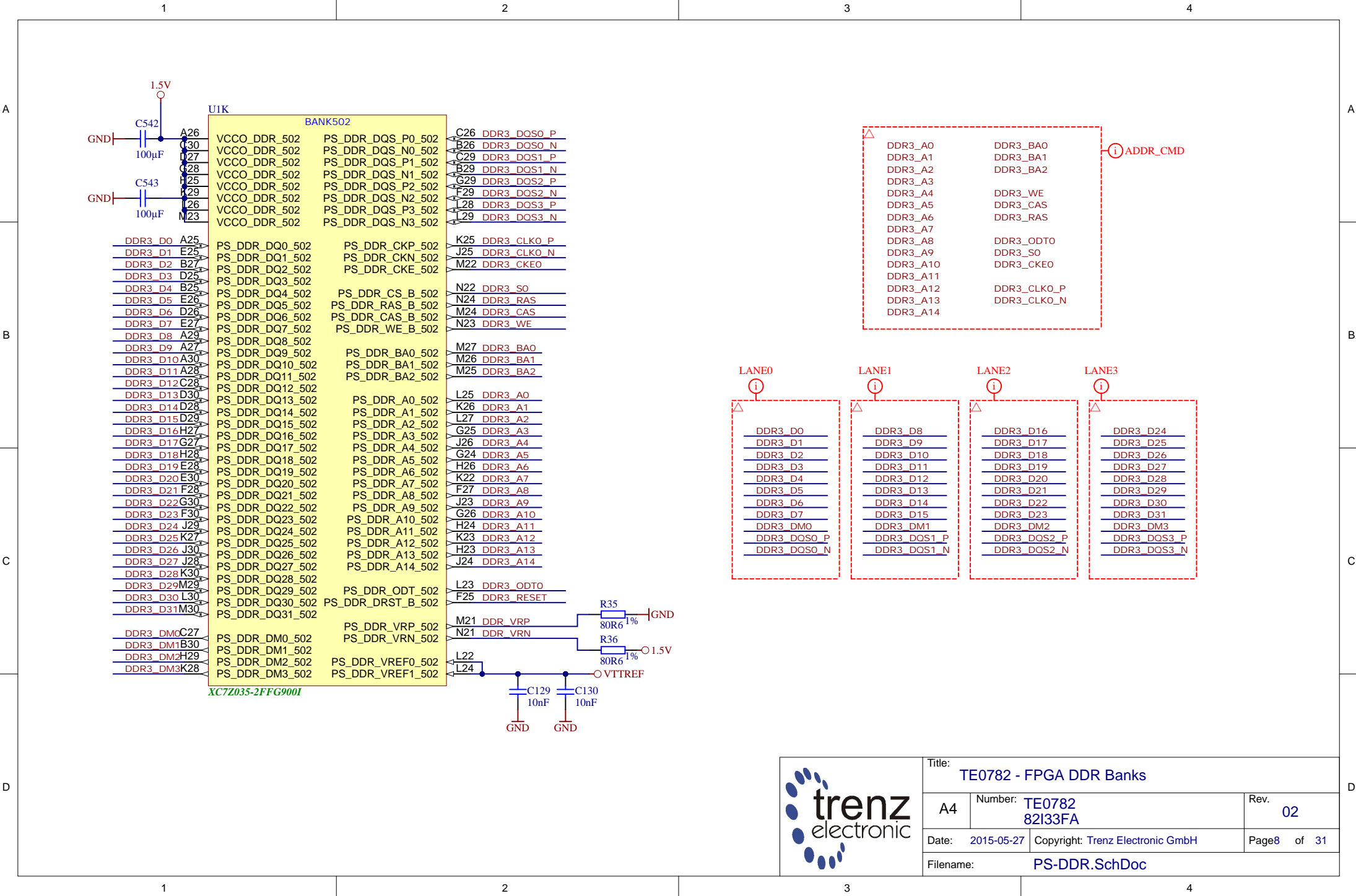
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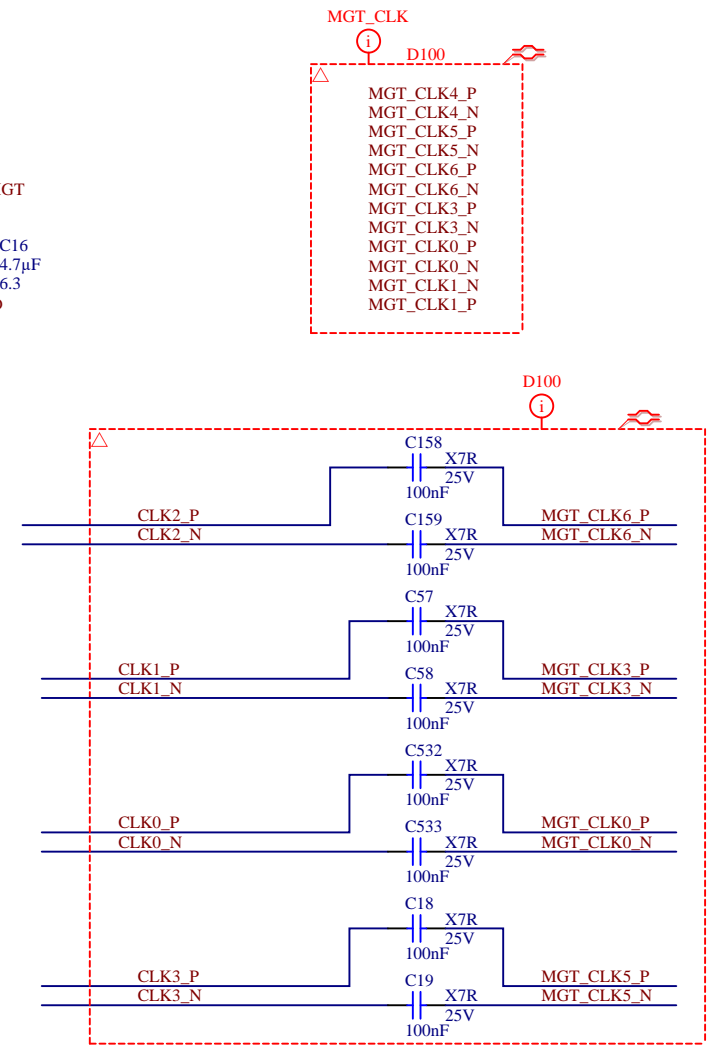
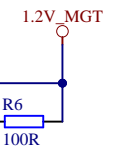
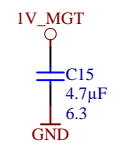
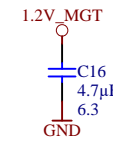
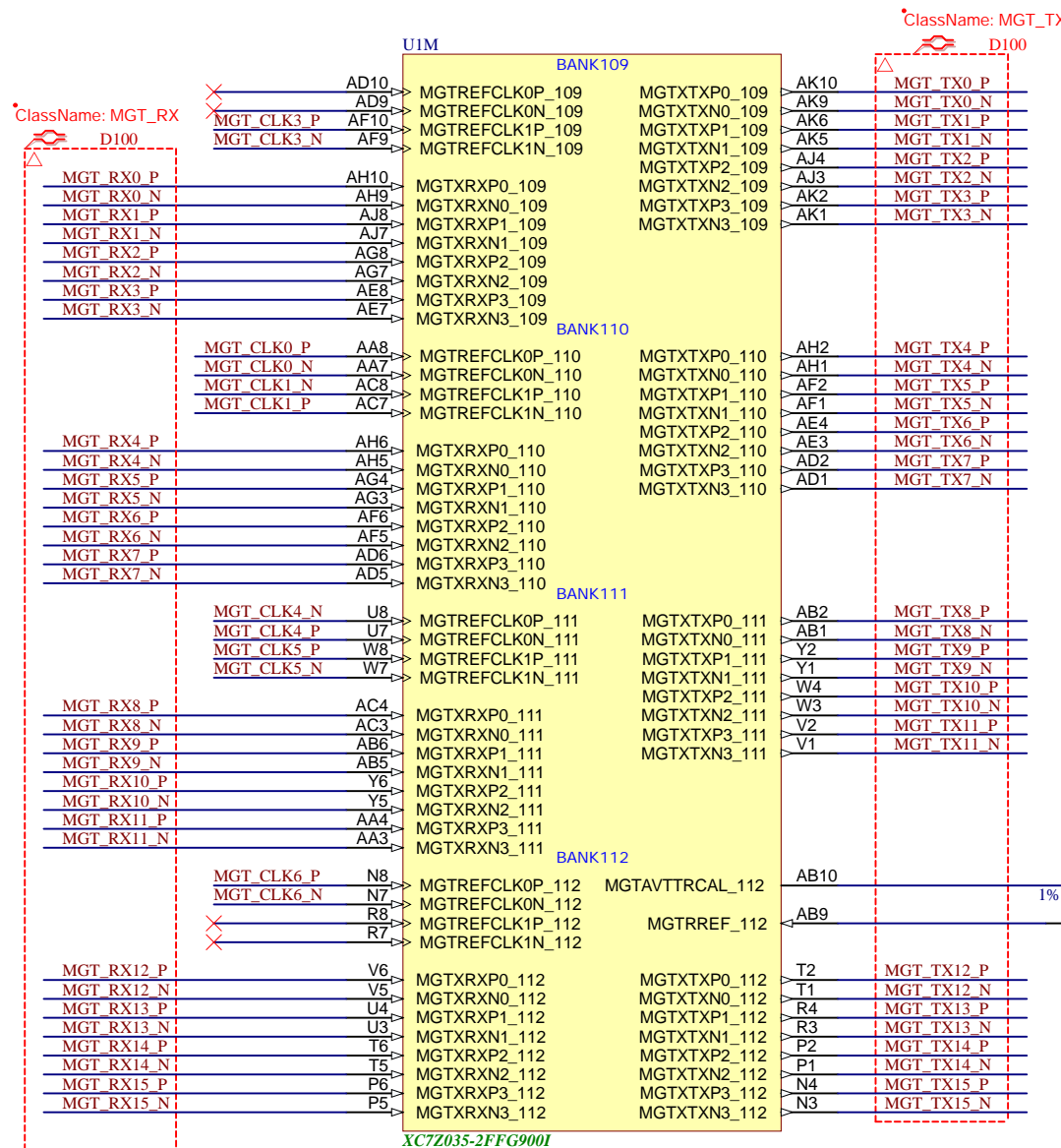
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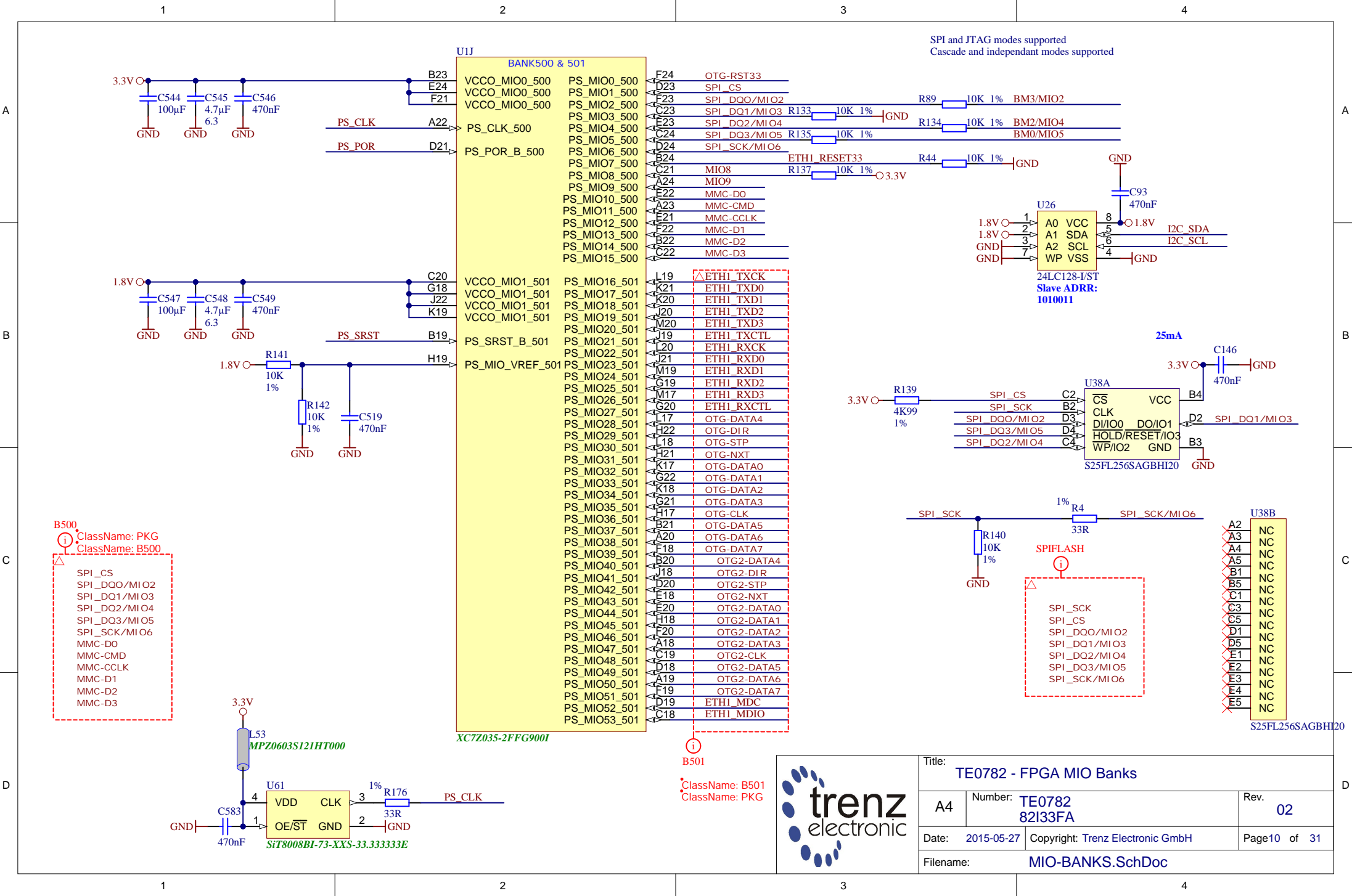
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Datum: 2015-05-27		Zeichner: Trenz Electronic GmbH	
Filename: FPGA-CFG.SchDoc		Blatt 7 von 31	



Title: TE0782 - FPGA DDR Banks		
A4	Number: TE0782 82I33FA	Rev. 02
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Filename: PS-DDR.SchDoc		



Title: TE0782 - FPGA MGT		
A4	Number: TE0782 82133FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page9 of 31
Filename: FPGA-MGT.SchDoc		

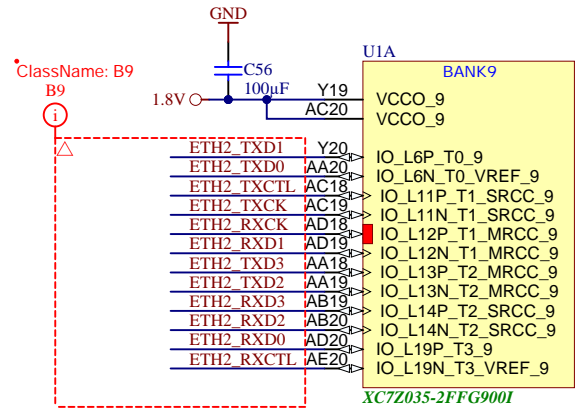


- B500**
- ClassName: PKG
 - ClassName: B500
 - SPI_CS
 - SPI_DQ0/MIO2
 - SPI_DQ1/MIO3
 - SPI_DQ2/MIO4
 - SPI_DQ3/MIO5
 - SPI_SCK/MIO6
 - MMC-D0
 - MMC-CMD
 - MMC-CCLK
 - MMC-D1
 - MMC-D2
 - MMC-D3

- SPIFLASH**
- SPI_SCK
 - SPI_CS
 - SPI_DQ0/MIO2
 - SPI_DQ1/MIO3
 - SPI_DQ2/MIO4
 - SPI_DQ3/MIO5
 - SPI_SCK/MIO6



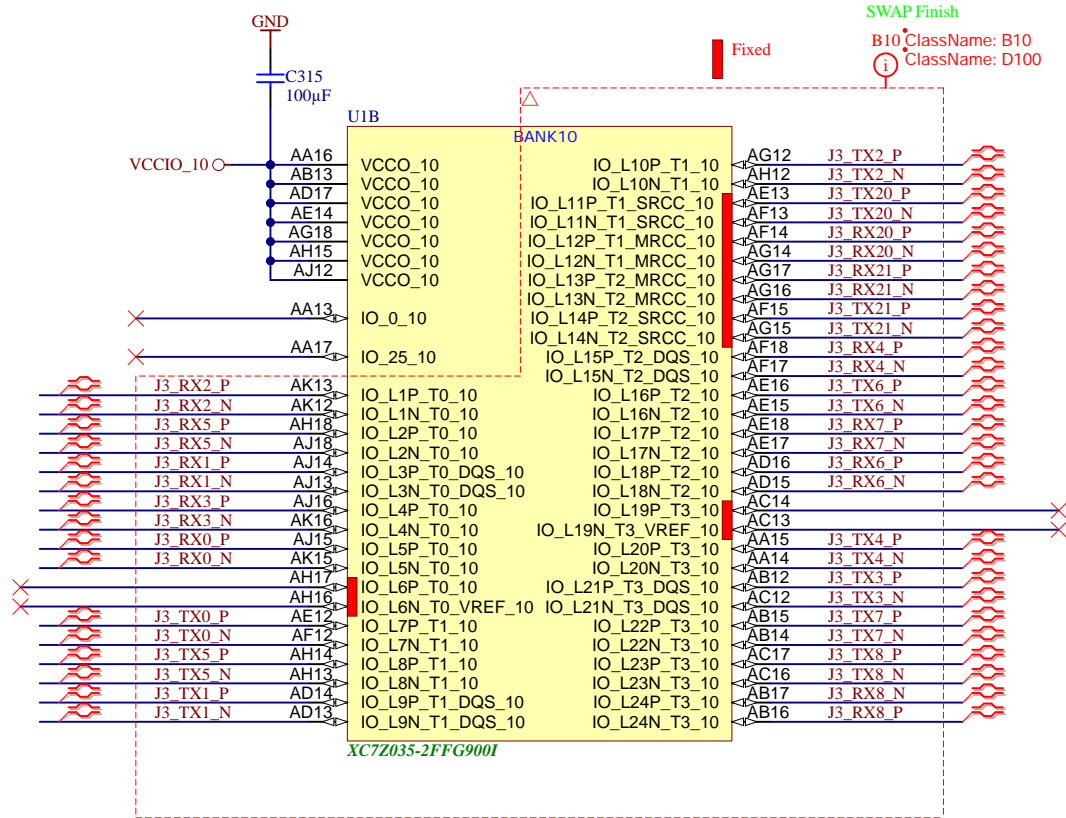
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 10 of 31
Filename: MIO-BANKS.SchDoc		




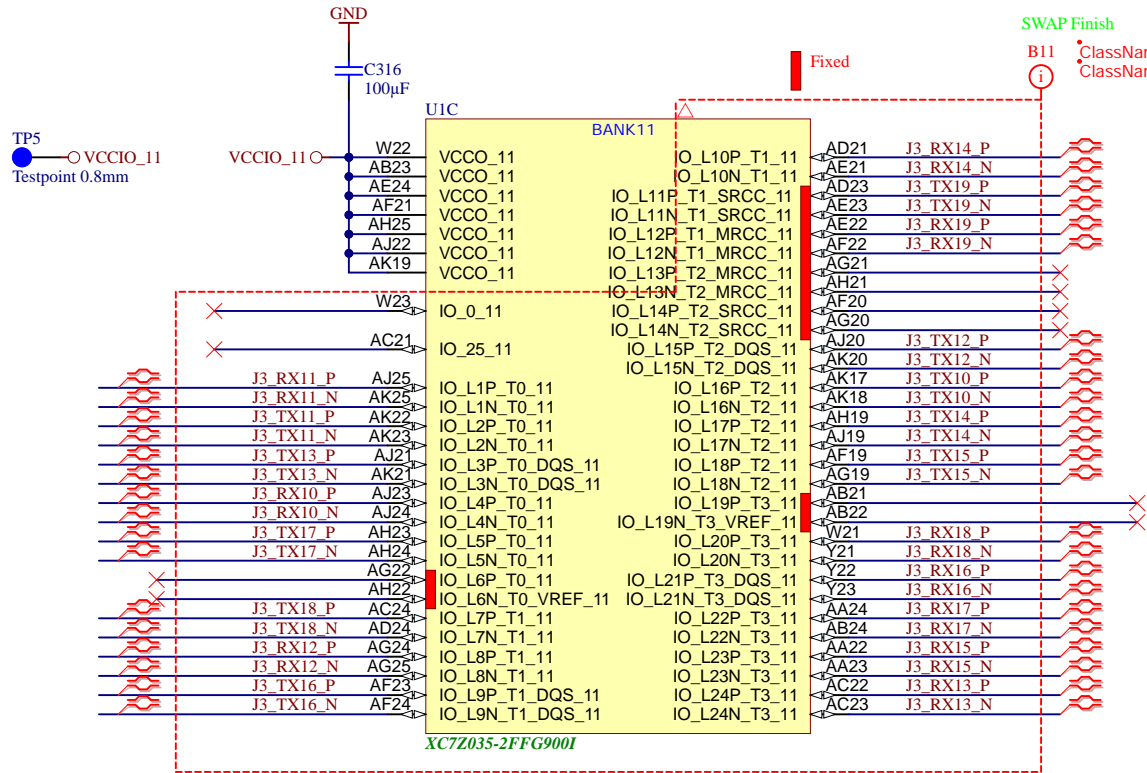
RXCK Fix to MRCCL
Fixed


	Title: TE0782 - FPGA B9		
	A4	Number: TE0782 82I33FA	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 11 of 31
	Filename: B9.SchDoc		


TP4
 ● VCCIO_10
 Testpoint 0.8mm

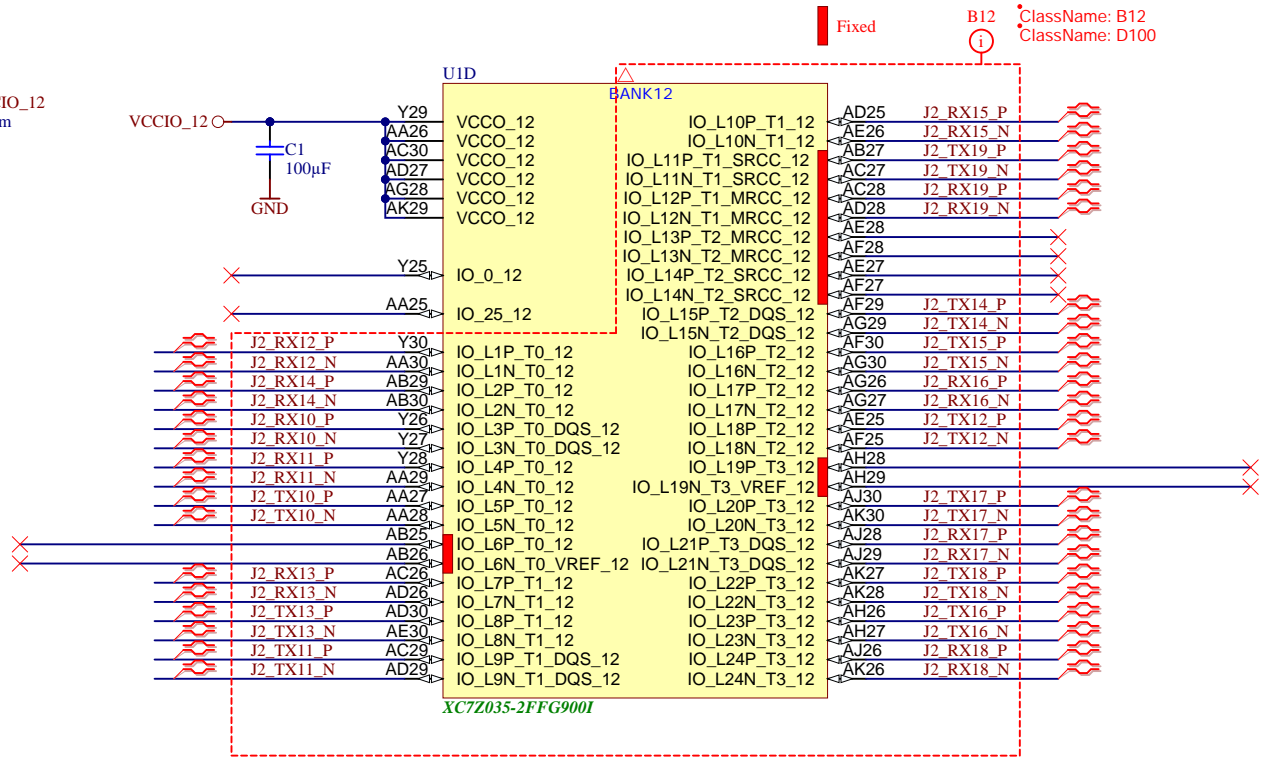


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	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 12 of 31
	Filename: B10.SchDoc		

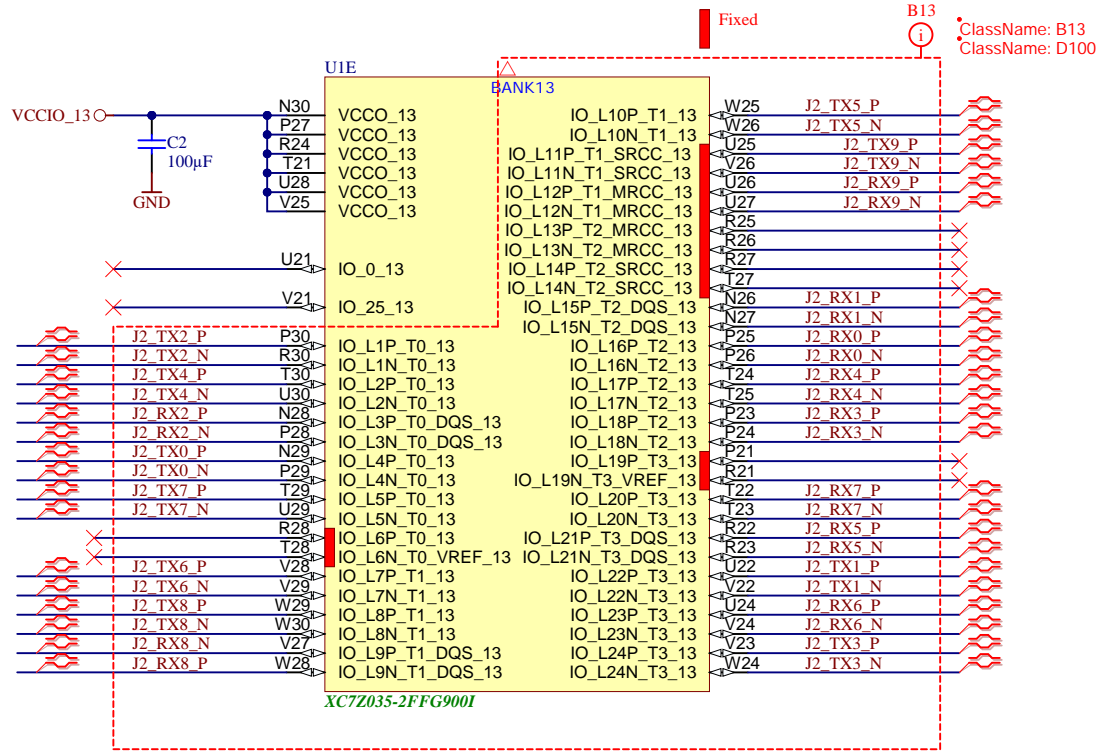
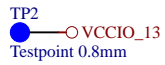


			Title: TE0782 - FPGA B11	
			A4	Number: TE0782 82I33FA
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Filename: B11.SchDoc				

TP1
 VCCIO_12
 Testpoint 0.8mm



Title: TE0782 - FPGA B12		
A4	Number: TE0782 82133FA	Rev. 02
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Filename: B12.SchDoc		



	Title: TE0782 - FPGA B13	
	A4	Number: TE0782 82133FA
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Filename: B13.SchDoc		

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



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		Title: TES0782 - FPGA HP Banks	
		A4	Number: TE0782 82I33FA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: HP-BANKS.SchDoc		Page 16 of 31	

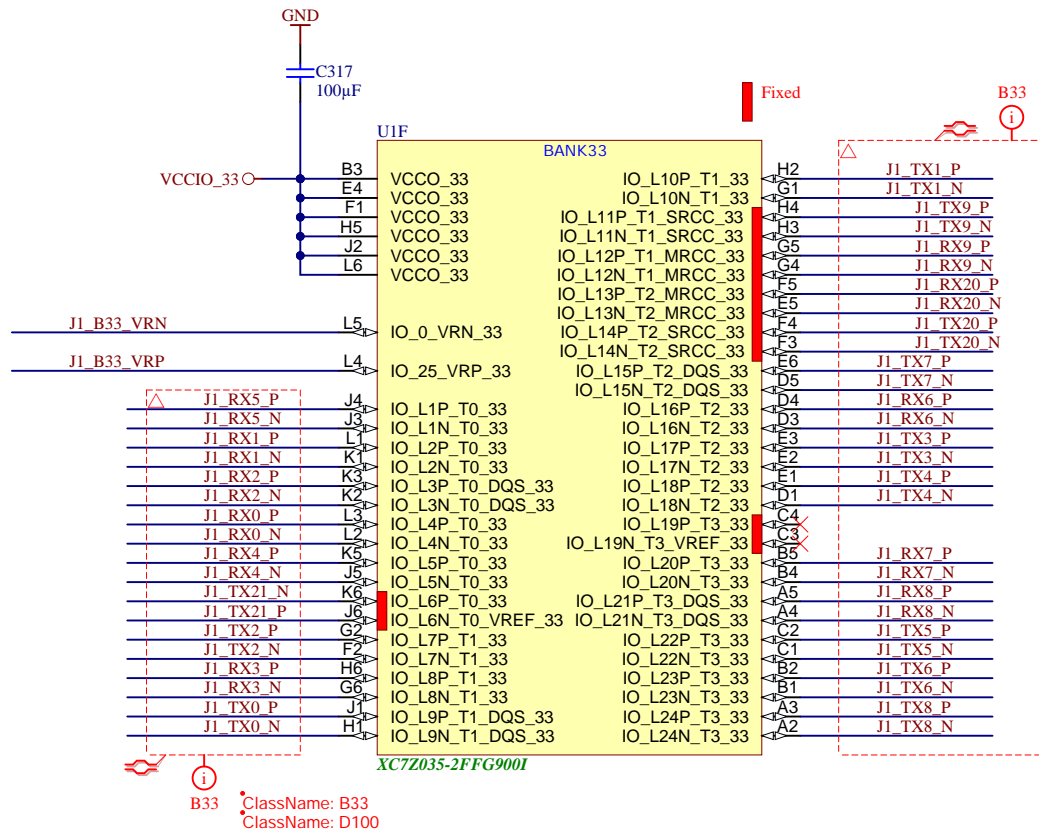

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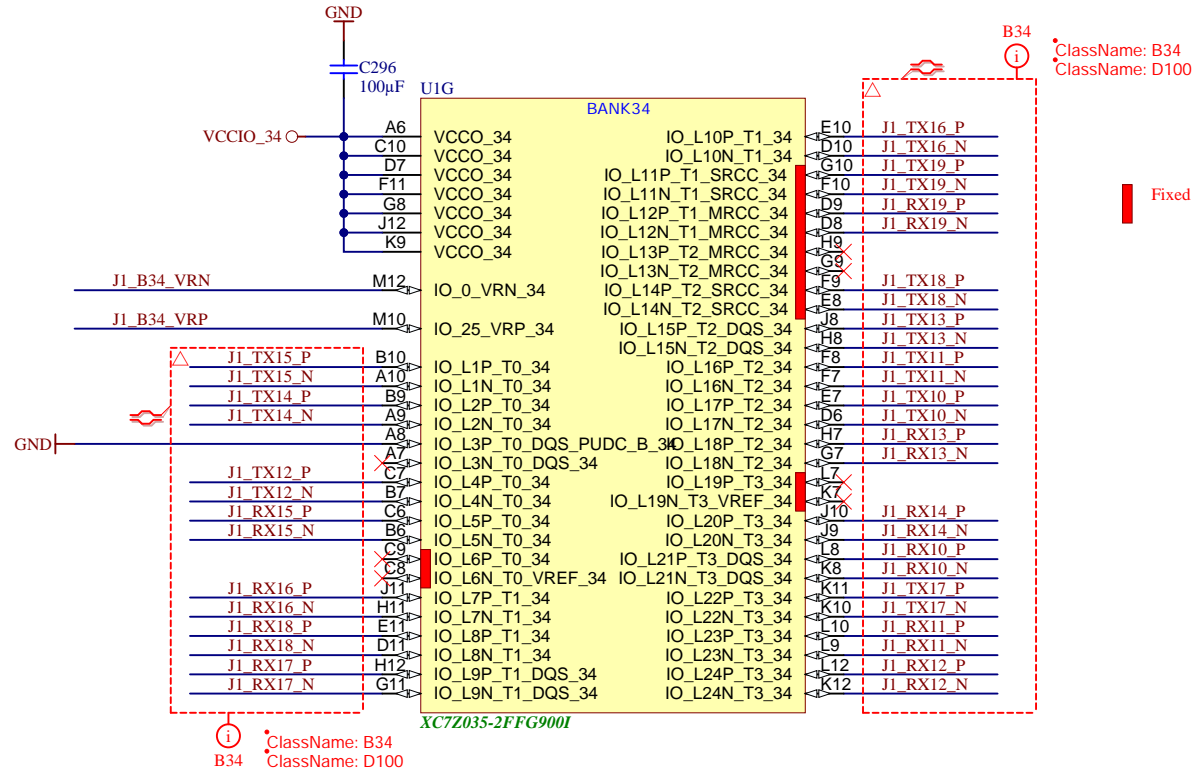
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TP6
 VCCIO_33
 Testpoint 0.8mm

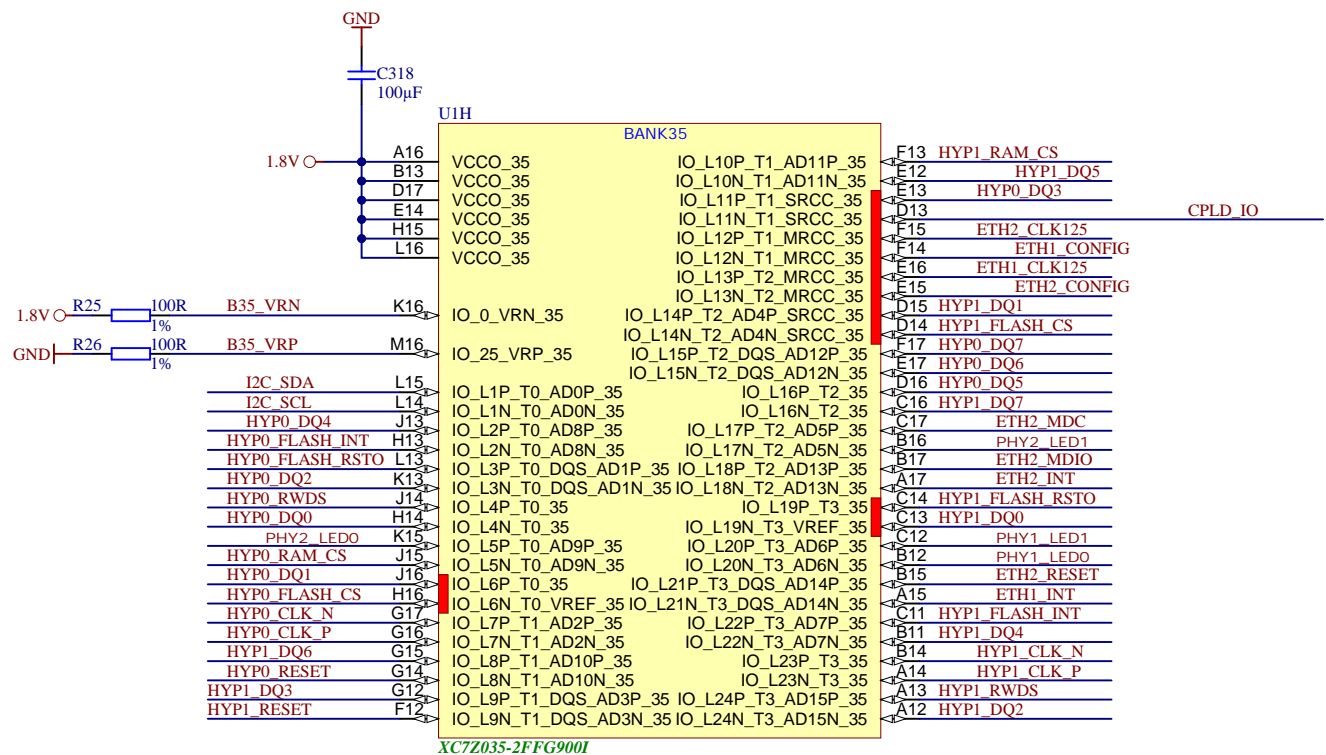



Title: TE0782 - FPGA B33		
A4	Number: TE0782 82I33FA	Rev. 02
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Filename: B33.SchDoc		

TP3
 VCCIO_34
 Testpoint 0.8mm



Title: TE0782 - FPGA B34		
A4	Number: TE0782 82I33FA	Rev. 02
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Filename: B34.SchDoc		

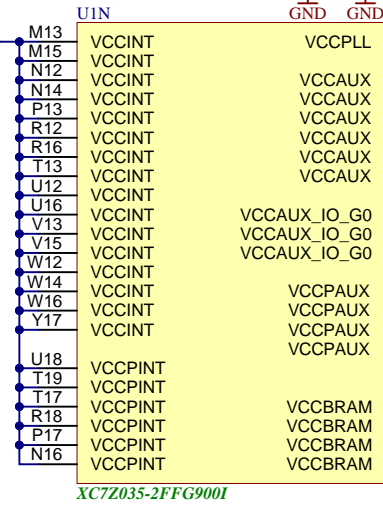
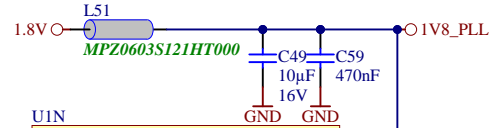
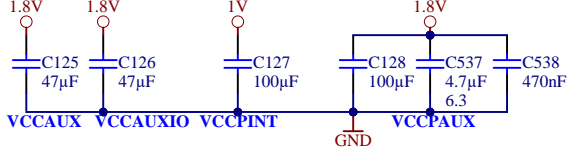
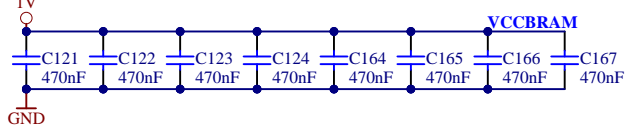
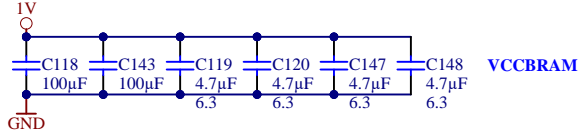
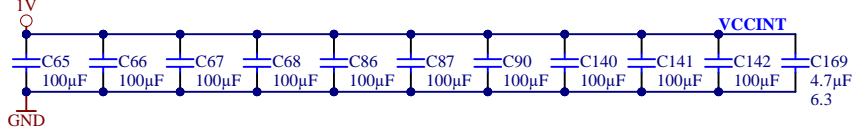
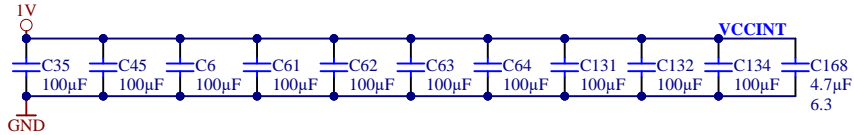


XC7Z035-2FFG9001



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Filename: B35.SchDoc		

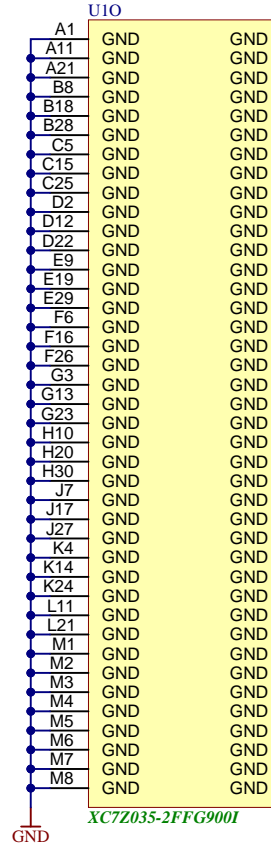
Capacitors suitable for XC7Z100



XC7Z035-2FFG900I

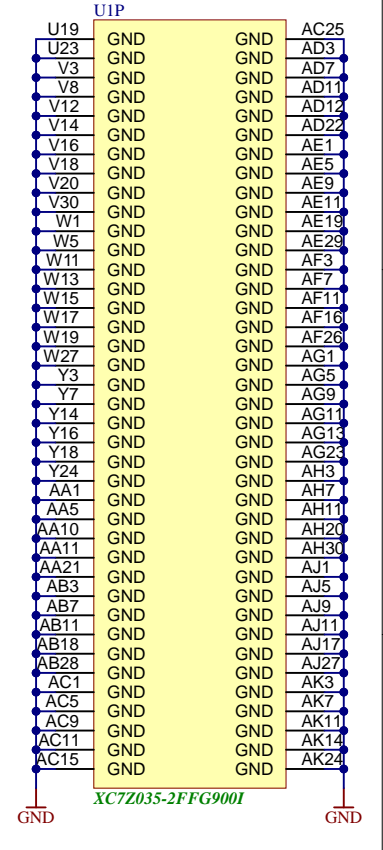
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XC7Z035-2FFG900I



U10

XC7Z035-2FFG900I

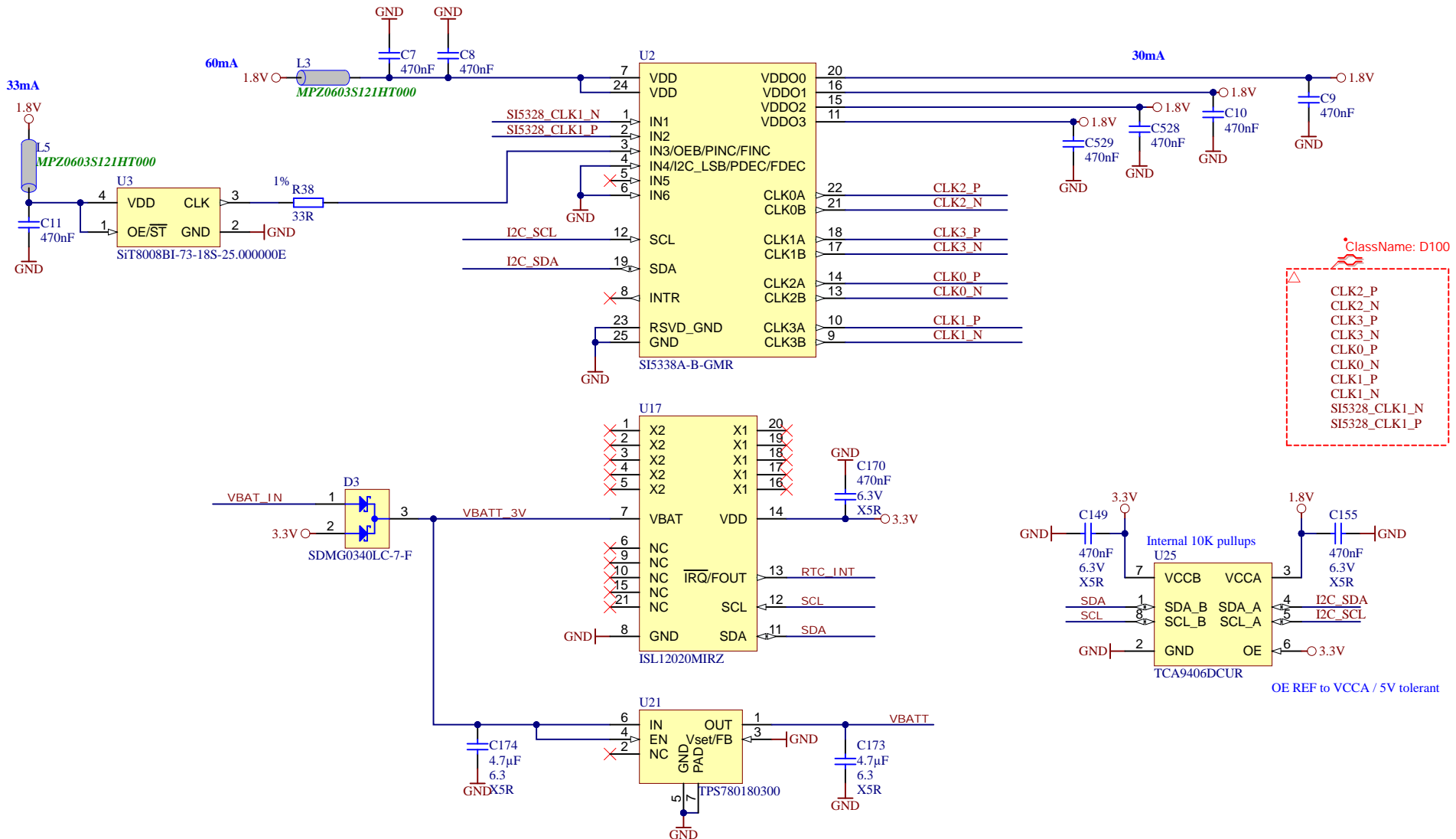


UIP


XC7Z035-2FFG900I



Title: TE0782 - ZYNQ POWER		
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Filename: FPGA-PWR.SchDoc		Page20 of 31



- ClassName: D100
- CLK2_P
 - CLK2_N
 - CLK3_P
 - CLK3_N
 - CLK0_P
 - CLK0_N
 - CLK1_P
 - CLK1_N
 - SI5328_CLK1_N
 - SI5328_CLK1_P

			Title: TE0782 - Clock	
			A4	Number: TE0782 82133FA
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 21 of 31
Filename: Clock.SchDoc				

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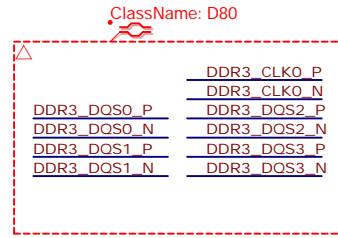
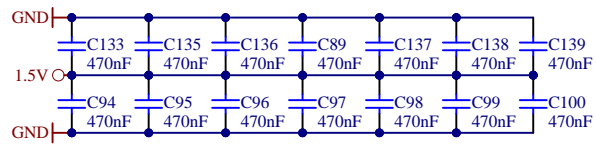
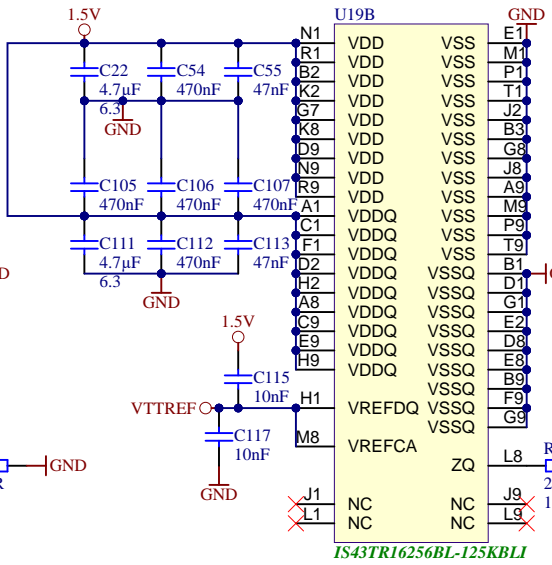
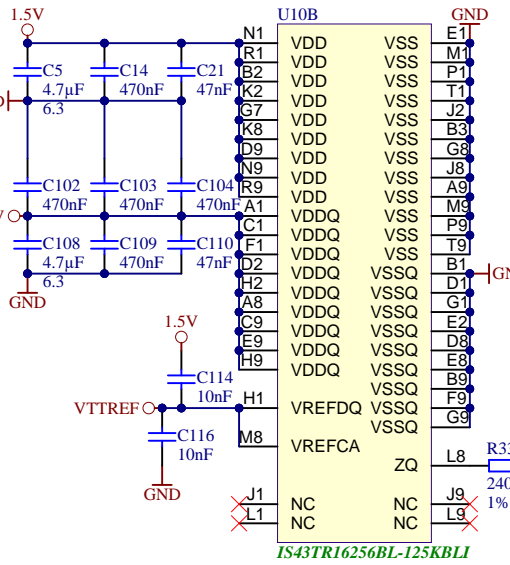
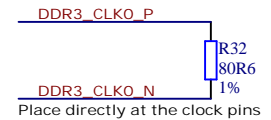
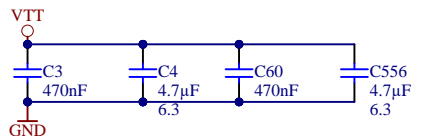
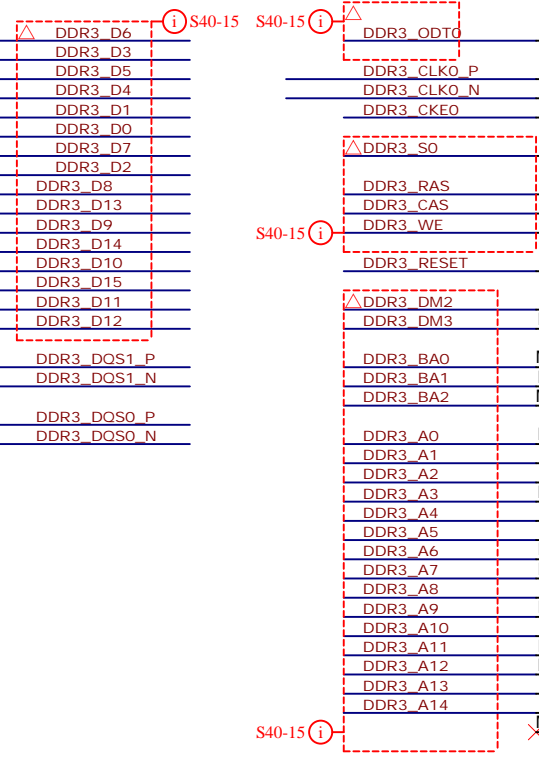
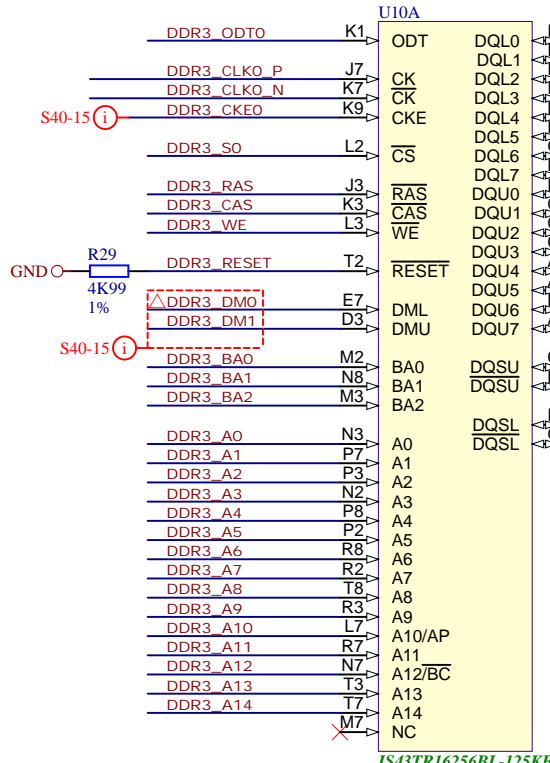
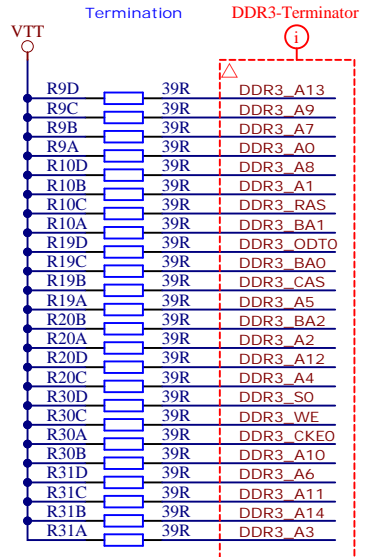
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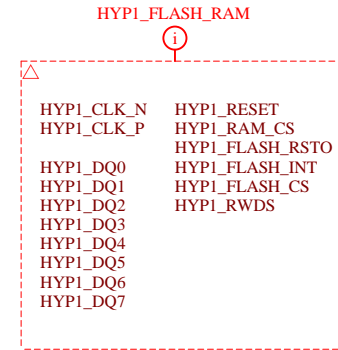
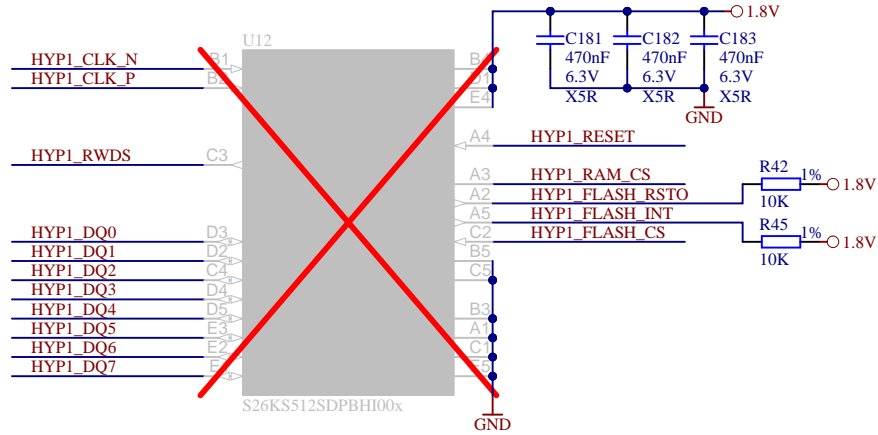
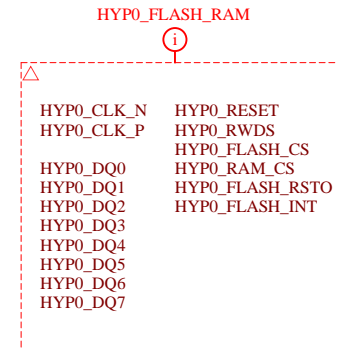
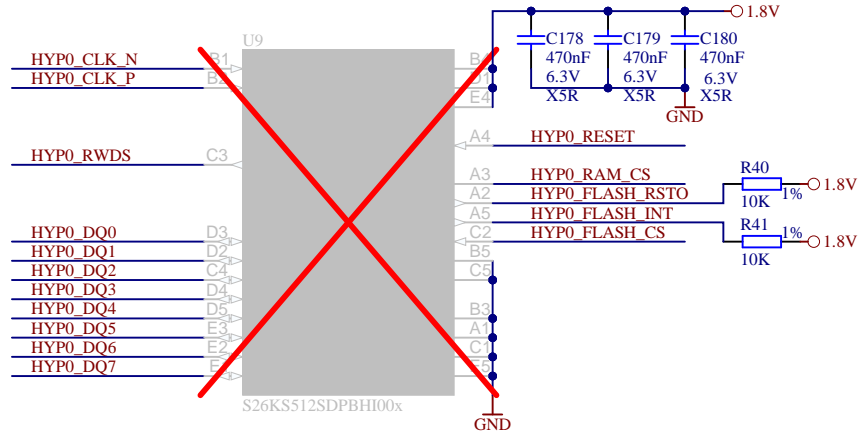
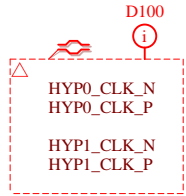

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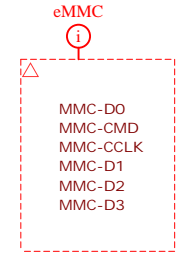
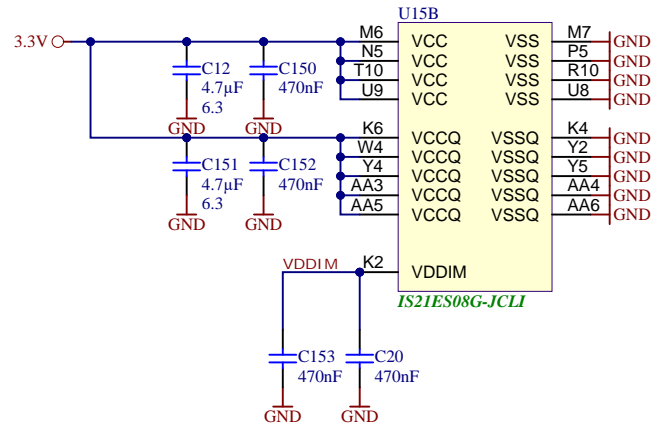
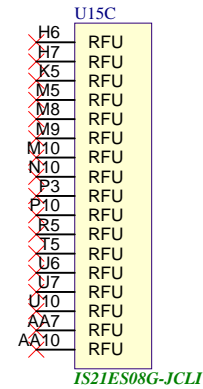
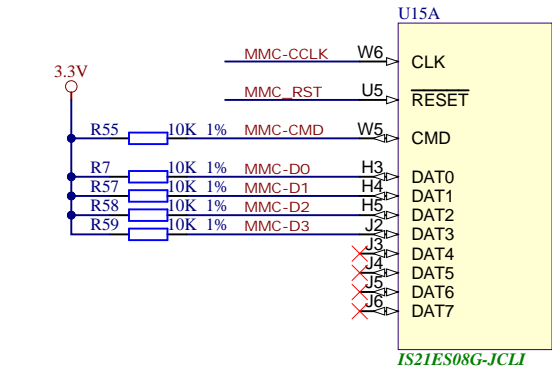
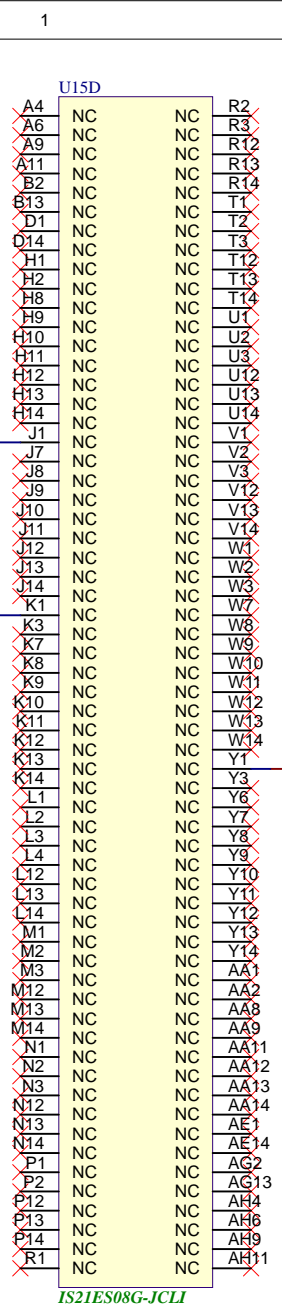
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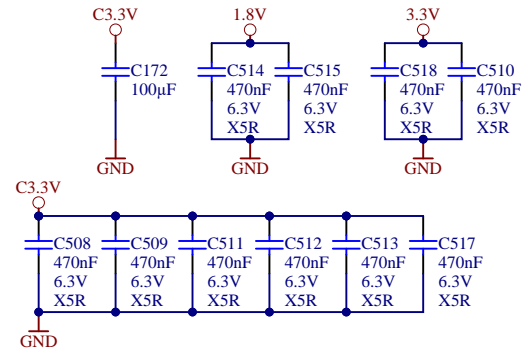
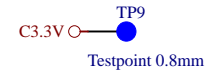
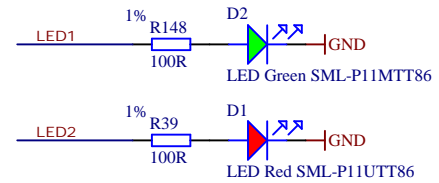
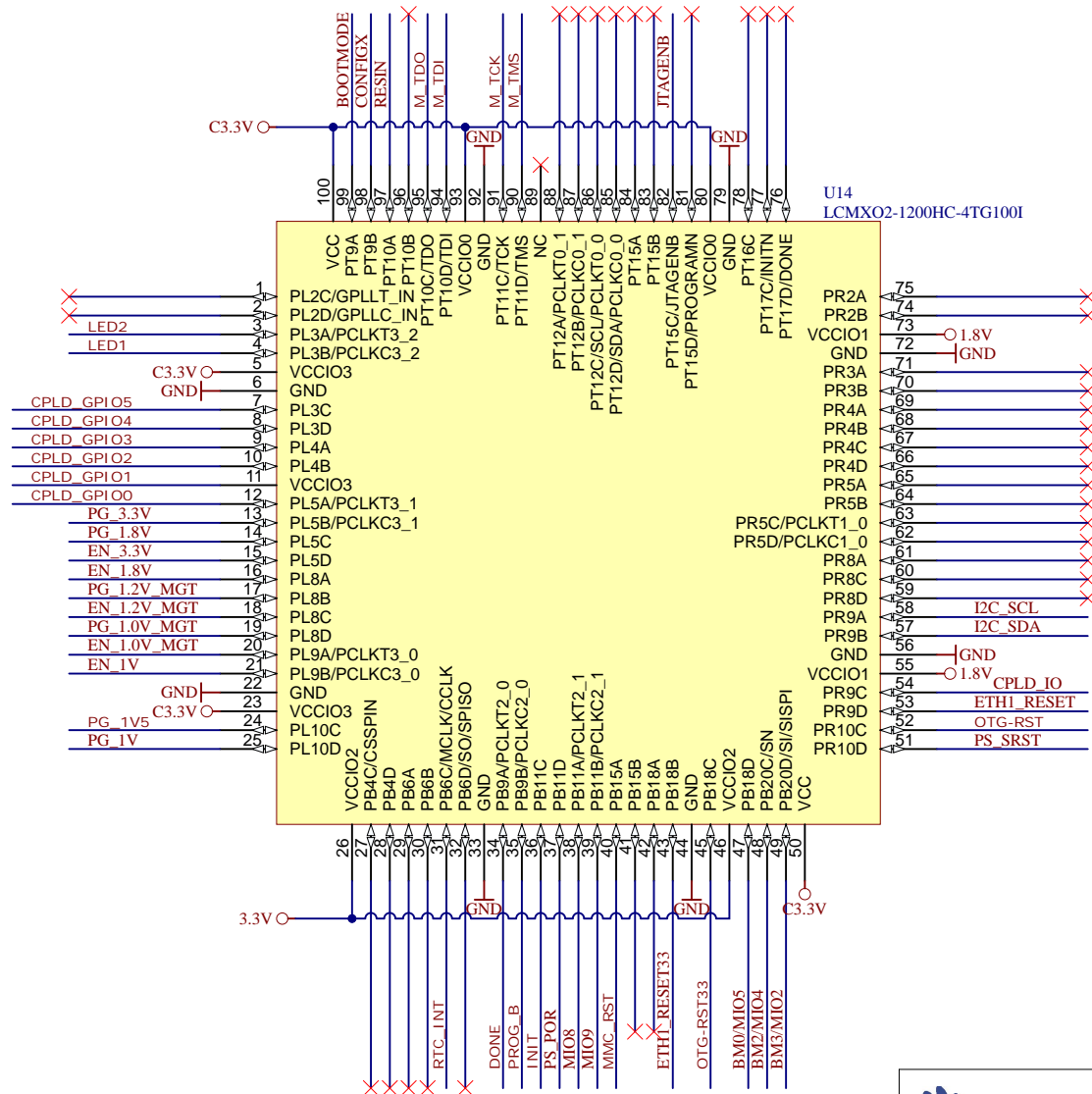
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 22 of 31
Filename: DDR3-RAM.SchDoc		

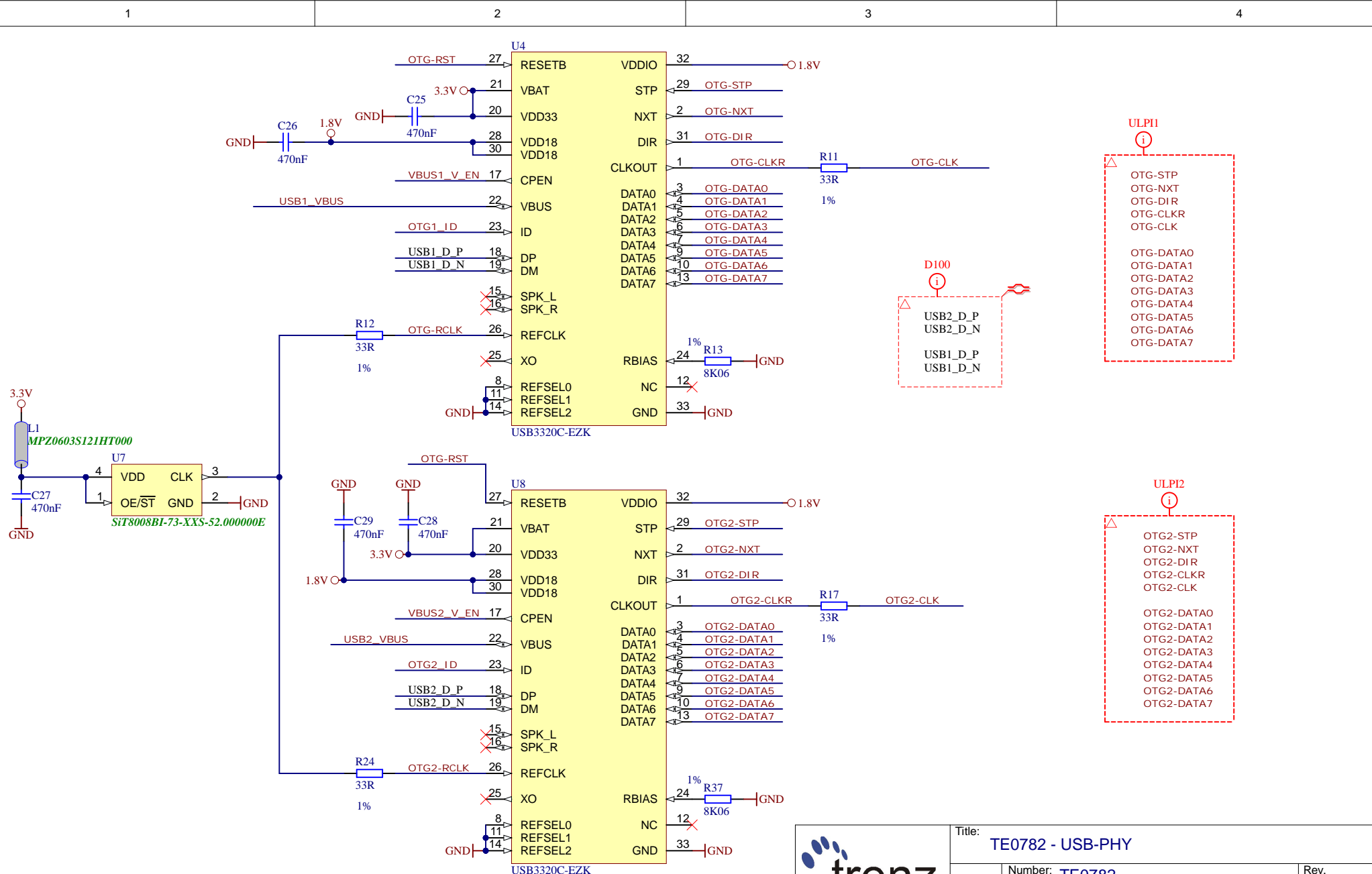
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A4	Number: TE0782 82I33FA	Rev. 02
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Filename: HyperFlash_RAM.SchDoc		




Title: TE0782 - eMMC		
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			Title: TE0782 - CPLD	
			A4	Number: TE0782 82133FA
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			Title: TE0782 - USB-PHY	
			A4	Number: TE0782 82I33FA
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Filename: USB-PHY.SchDoc				

1

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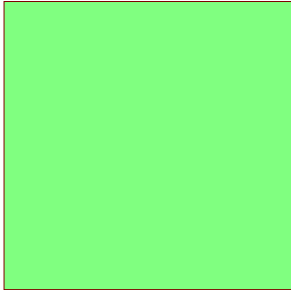
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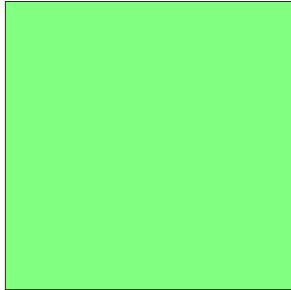
A

A

U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



B

B

C

C

D

D



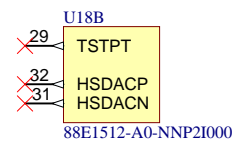
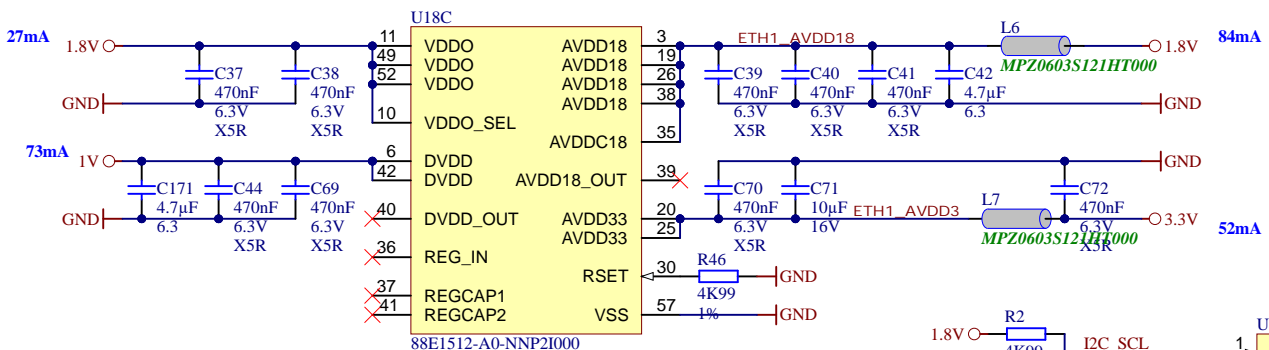
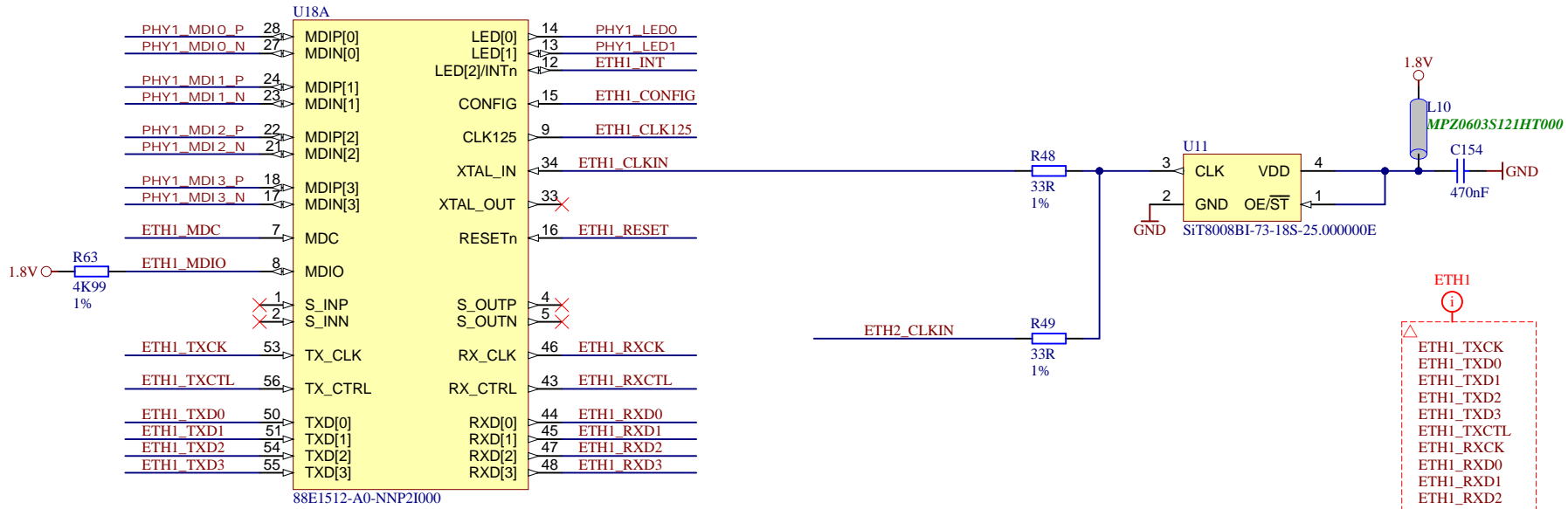
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A4	Number: TE0782 82I33FA	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 27 of 31
Filename: Ethernet.SchDoc		


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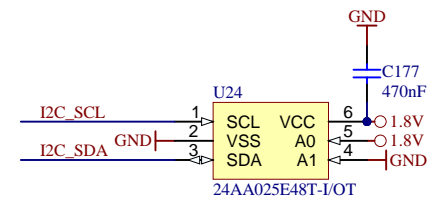
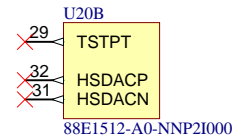
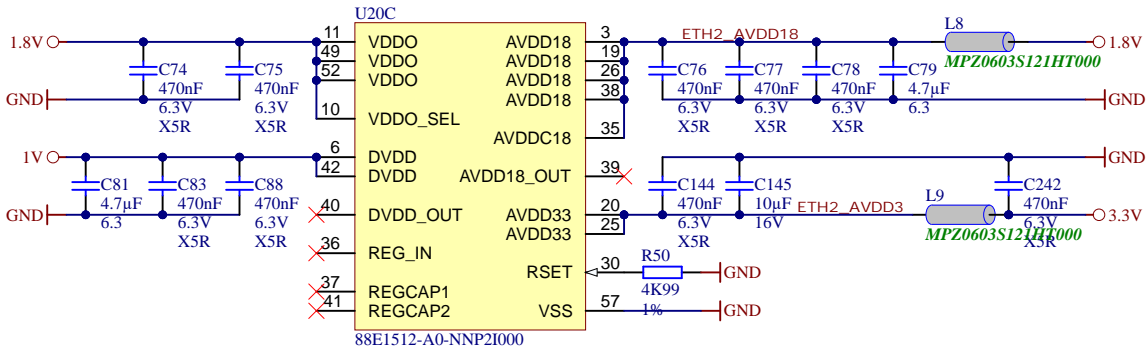
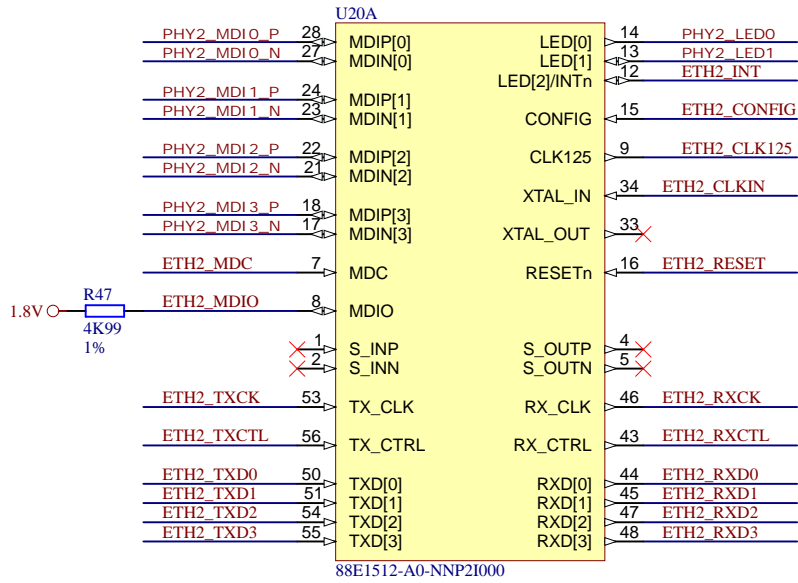
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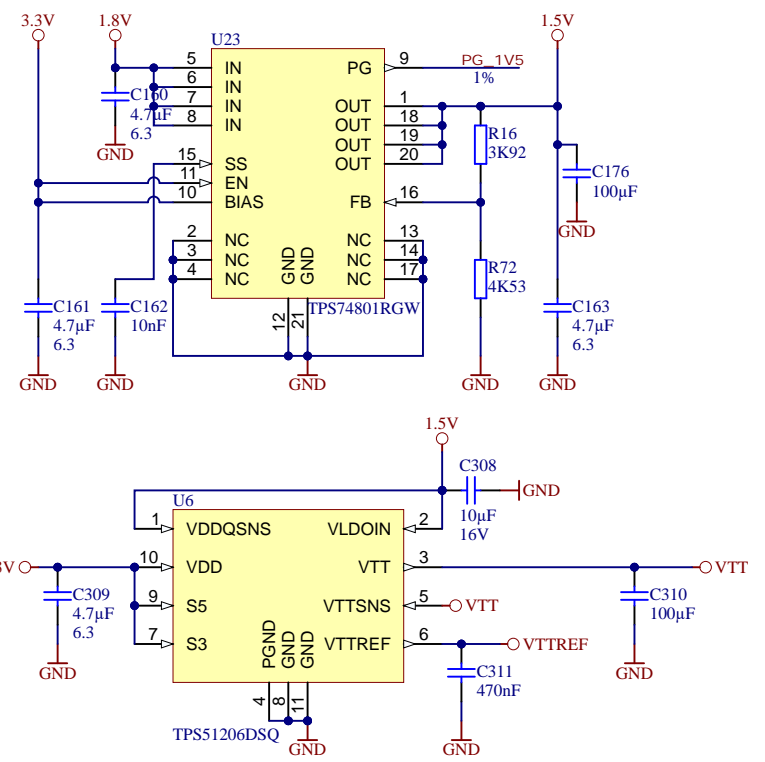
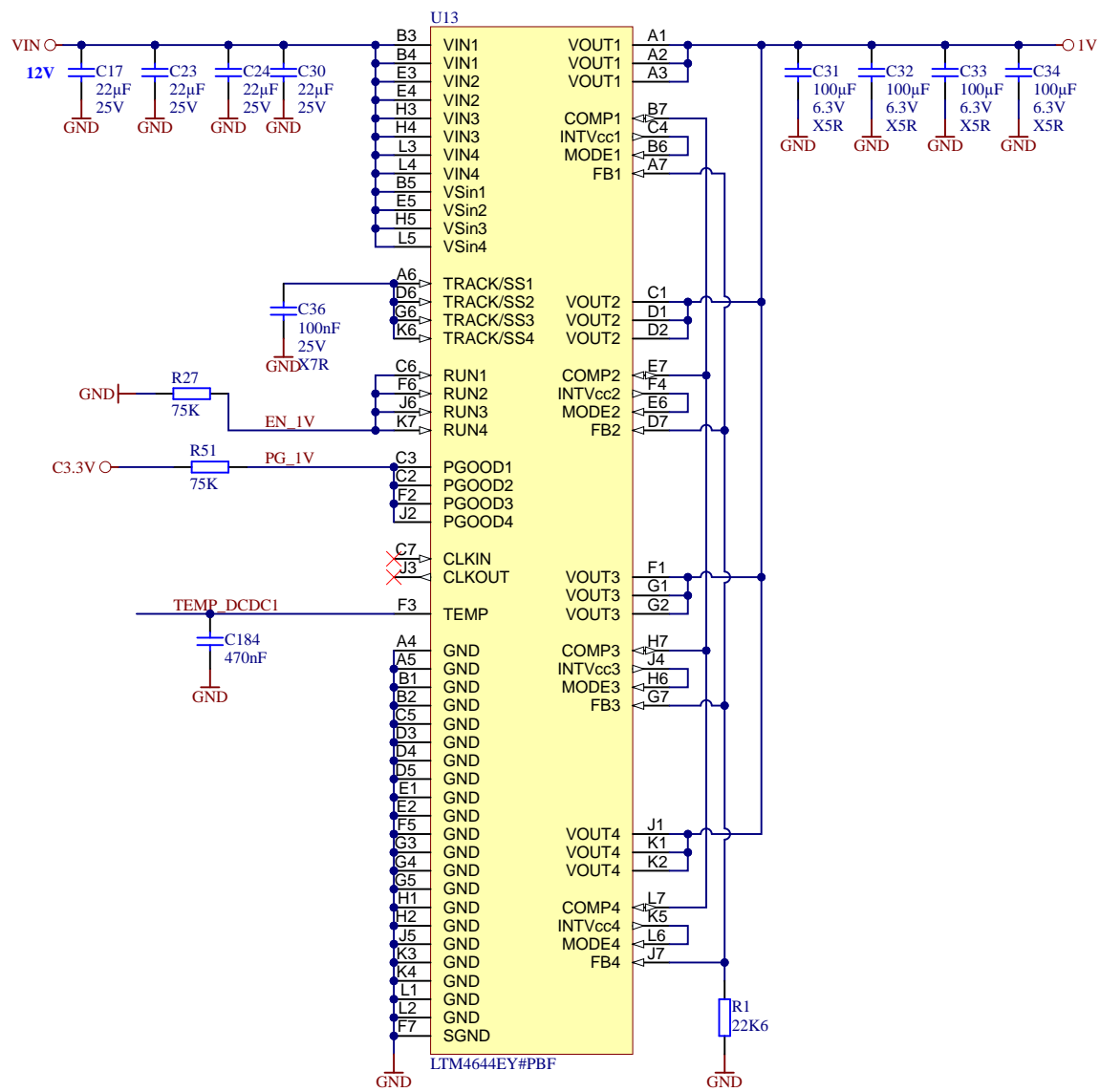


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Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 28 of 31
Filename: ETH1.SchDoc				



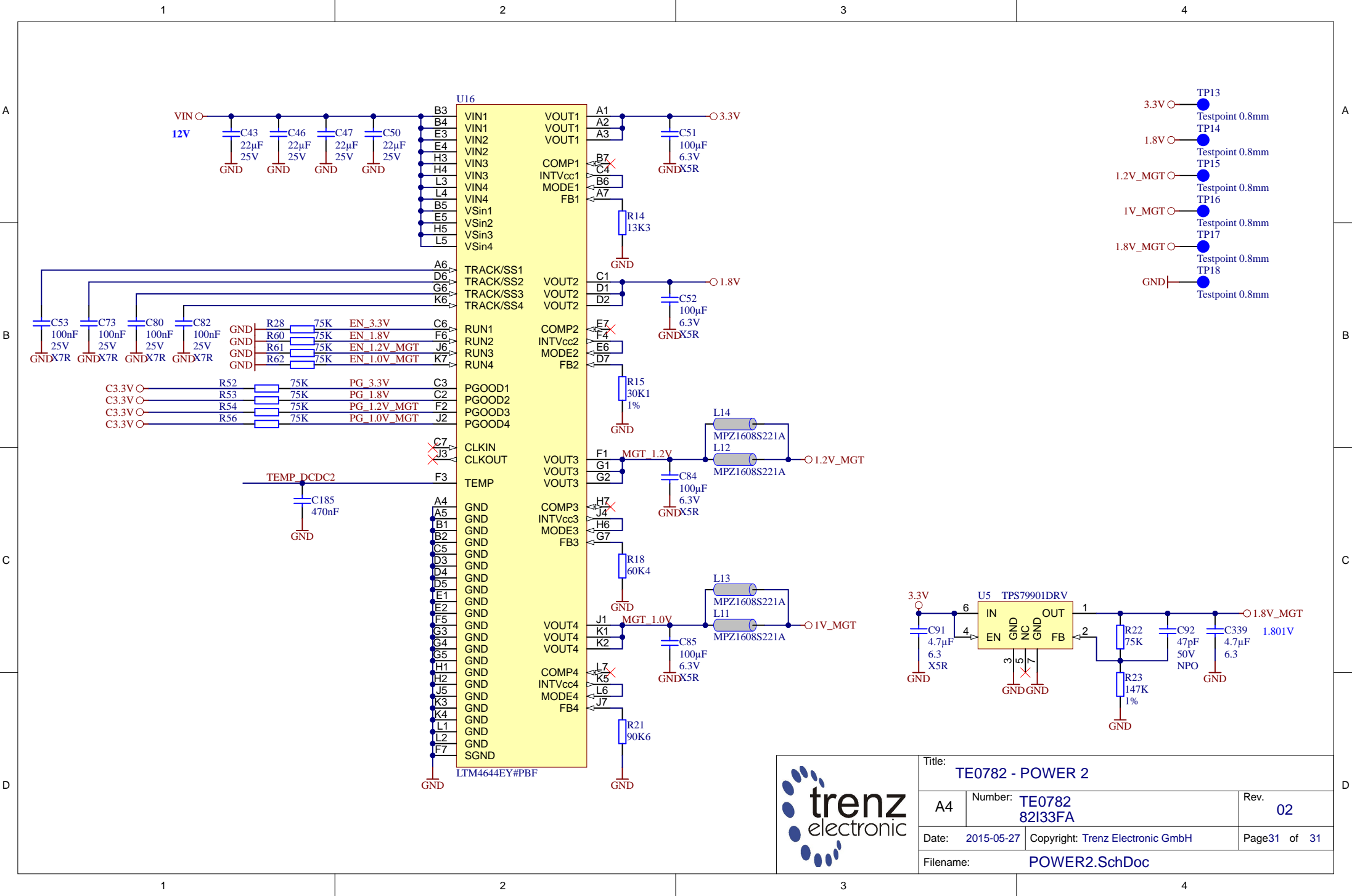
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Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 29 of 31
Filename: ETH2.SchDoc				



- TP7 1V Testpoint 0.8mm
- TP8 GND Testpoint 0.8mm
- TP10 1.5V Testpoint 0.8mm
- TP11 VTT Testpoint 0.8mm
- TP12 VTTREF0 Testpoint 0.8mm

	Title: TE0782 - POWER	
	A4	Number: TE0782 82I33FA
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH
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Filename: POWER.SchDoc		



			Title: TE0782 - POWER 2	
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Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 31 of 31
Filename: POWER2.SchDoc				