PC	N Nui	mber:	201501050	01				PCN Dat	te:	01/13/2015
Tit	tle:	Datasheet up	date for LM	K04	180x					
Cu	stom	er Contact:	PCN Manager		Phone:			Dept:	Qua	lity Services
Ch	ange	Туре:				1		•		•
		embly Site			Design			Wafer	Bumı	Site
	Asse	embly Process			Data Sh	eet		Wafer Bump Material		
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	Mec	hanical Specif	ication		Test Site			Wafer Fab Site		
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111	e prou	uct datasneet	(s) is being u	pu	ateu as si	ummarize below.				
Th	e follo	wing change h	nistory provid	6 5	further d	etails				
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Ch	nanges f	rom Revision J (M	larch 2013) to Re	visi	on K					Page
_	Change	od 90 to 90 and 90 to	to 90 for f	n	rameter in E	Lectrical Characteristics				11
	Changed 90 to 80 and 80 to 90 for f _{CLKout-startup} parameter in Electrical Characteristics									
										11
						g titled "Charge Pump Ou				
			•							
•										
•	Changed from "n possible" to "D possible" in <i>0-Delay</i>									
•	Changed "can" to "cannot" in Input Clock Switching - Pin Select Mode									
•	Deleted Clock Switch Event without Holdover in Clock Switch Event with Holdover									
•	Added paragraph beginning "For applications" in PLL2 Frequency Doubler									
•	_									
•	Deleted Mode 5 row in Table 12									
•			-							
•	In Table 16, added [27:26], [23:22], and [21:20] for Register 27 row. Added [31:20] for R28. Added [26:24] for R30. Added [7:6]					51				
•	In Table 18, changed "Actual PLL2 N divider value used in calibration routine". Added footnote "Inversion for Status 0 and 1 pins is only valid for CLKin_SELECT_MODE = 0x06"					56				
•	In Table 28, added "to reduce supply" footnote for 9 through 14. Added footnote "To reduce supply switching and crosstalk noise, it is recommended to use a complementary LVCMOS output type such as 6 or 7"					ng and 64				
	Added footnote "To reduce supply" for 8 through 14 in Table 32									
		Changed "Divide" to "Definition" in Table 39, Table 40, Table 61, and Table 62								
	_	hanged to "MUX OUTPUT" in Table header row in Table 42								
	_	In Table 43, added footnote, "Contact TI Applications for more information on using this mode". Changed to "Dual								

Revision History (continued) Added "Inversion for Status 0 and 1 pins is only valid for CLKin SELECT MODE = 0x06" in CLKin Sel INV......78 In FORCE HOLDOVER, added "(EN TRACK = 0 or 1, EN MAN DAC =1)", Added "(EN TRACK = 1, In Table 90, added (0x0000), (0x0001), (0x0002), (0x0003). Changed "Divide" to "Value" in the header row. Added PLL2 Frequency Doubler 88 Added "Performance of other LMK0480x devices will be similar" in Optional Crystal Oscillator Implementation Changed to "(fs rms)" in Table 125 In Vcc2, Vcc3, Vcc10, Vcc11, Vcc12, Vcc13 (CLKout Vccs), added bullet point starting with "It is recommended..."

The datasheet number will be changing.

Device Family	Change From:	Change To:
LMK0480x	SNAS489J	SNAS489K

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/lmk04803

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

Electrical specification performance changes as indicated above.

Changes to product identification resulting from this PCN:

None.

Product Affected:

LMK04803BISQ/NOPB	LMK04805BISQX/NOPB	LMK04808BISQE/NOPB	LMK04808DISQ/NOPB
LMK04803BISQE/NOPB	LMK04806BISQ/NOPB	LMK04808BISQX/NOPB	LMK04808DISQE/NOPB
LMK04803BISQX/NOPB	LMK04806BISQE/NOPB	LMK04808CISQ/NOPB	LMK04808DISQX/NOPB
LMK04805BISQ/NOPB	LMK04806BISQX/NOPB	LMK04808CISQE/NOPB	
LMK04805BISQE/NOPB	LMK04808BISQ/NOPB	LMK04808CISQX/NOPB	

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

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