

The documentation and process conversion measures necessary to comply with this document shall be completed by 30 October 2015.

INCH-POUND

MIL-PRF-19500/558K  
 30 July 2015  
 SUPERSEDING  
 MIL-PRF-19500/558J  
 29 March 2013

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, UNITIZED, PNP, SILICON, SWITCHING,  
 FOUR TRANSISTOR ARRAY, TYPES 2N6987, AND 2N6988,  
 JAN, JANTX, JANTXV, JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP, silicon, switching transistors, four independent chip array. Four levels of product assurance are provided for each device type as specified in MIL-PRF-19500. Radiation hardness assurance (RHA) level designators "M", "D", "P", "L", "R", "F", "G", and "H" are appended to the device prefix to identify devices which have passed RHA requirements.

\* 1.2 Package outlines. The device package for the encapsulated device types are as follows: 14-pin dual-in-line in accordance with figure 1, 14-pin flat-pack in accordance with figure 2, and 20-pin leadless chip carrier in accordance with figure 3.

1.3 Maximum ratings, unless otherwise specified  $T_A = +25^\circ\text{C}$ . (1)

	$P_T$ $T_A = +25^\circ\text{C}$ (2)	$P_T$ $T_{A(AM)} = +25^\circ\text{C}$ (2)	$R_{\theta JA}$ (3)	$R_{\theta JA(AM)}$ (3) (4)	$V_{CBO}$ (5)	$V_{EBO}$ (5)	$V_{CEO}$ (5)	$I_c$ (3)	$T_J$ and $T_{STG}$
	<u>W</u>	<u>W</u>	<u><math>^\circ\text{C/W}</math></u>	<u><math>^\circ\text{C/W}</math></u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u><math>^\circ\text{C}</math></u>
2N6987	1.5	N/A	85	N/A	60	5	60	600	-65
2N6987U	1.0	N/A	160	N/A	60	5	60	600	to
2N6988	1.0	1.0	175	23	60	5	60	600	+200

- (1) Maximum voltage between transistors shall be  $\geq 500$  V dc.
- (2) For derating see figures 5, 6, 7, and 8.
- (3) For thermal impedance graphs, see figures 9, 10, 11, and 12.
- (4) Thermally conductive adhesive mount to infinite heat sink.
- (5) Ratings apply to each transistor in the array.

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



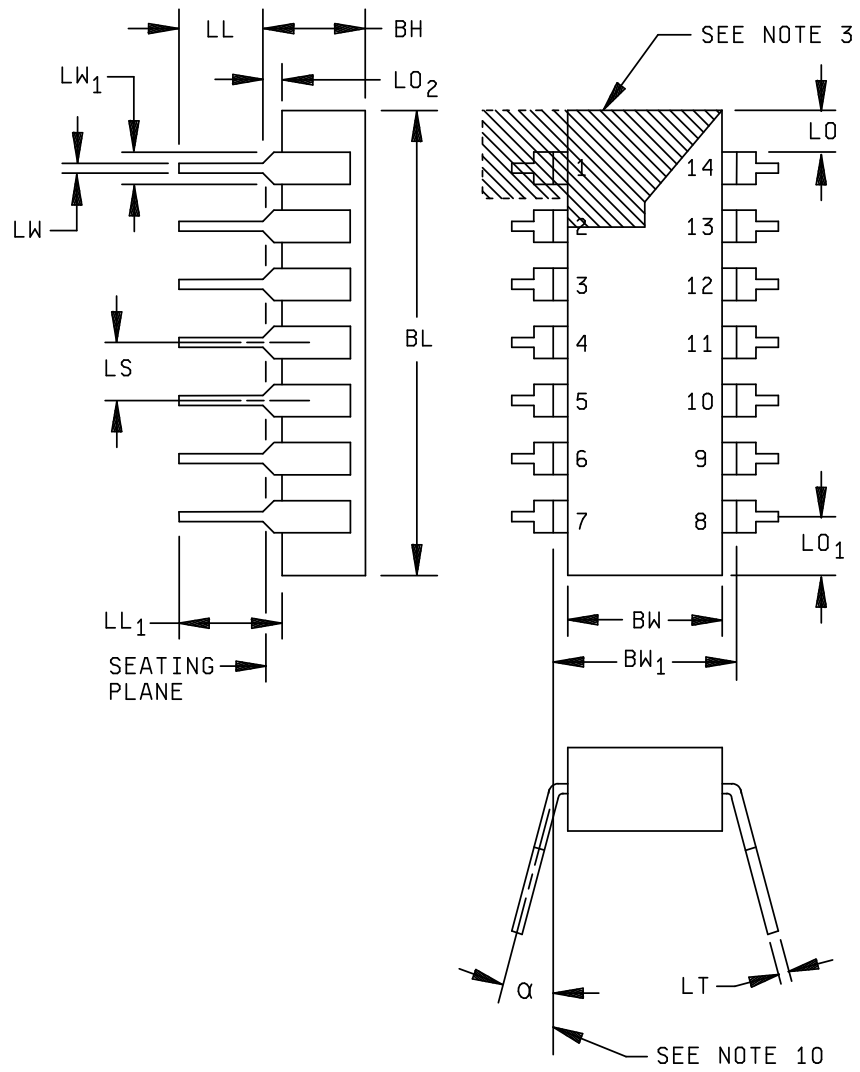


FIGURE 1. Dimensions and configuration for type 2N6987.

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Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BH		.200		5.08	
LW	.014	.023	0.36	0.58	8
LW <sub>1</sub>	.030	.070	0.76	1.78	4, 8
LT	.008	.015	0.20	0.38	8
BL		.785		19.94	4
BW	.220	.310	5.59	7.87	4
BW <sub>1</sub>	.290	.320	7.37	8.13	7
LS	.100 BSC		2.54 BSC		5, 9
LL	.125	.200	3.18	5.08	
LL <sub>1</sub>	.150		3.81		
LO <sub>2</sub>	.015	.060	0.38	1.52	3
LO <sub>1</sub>		.098		2.49	6
LO	.005		0.13		6
$\alpha$	0°	15°	0°	15°	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for information only.
3. Index area; a notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
4. The minimum limit for dimension LW<sub>1</sub> may be .023 inch (0.58 mm) for lead numbers 1, 7, 8, and 14 only.
5. Dimension LO<sub>2</sub> shall be measured from the seating plane to the base plane.
6. This dimension allows for off-center lid, meniscus, and glass overrun.
7. The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within  $\pm 0.010$  inch ( $\pm 0.25$  mm) of its exact longitudinal position relative to pins 1 and 14.
8. Applies to all four corners (lead numbers 1, 7, 8, and 14).
9. Lead center when  $\alpha$  is 0 degrees. BW<sub>1</sub> shall be measured at the centerline of the leads.
10. All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish A is applied. Pointed or round lead ends are allowed.
11. Twelve spaces.
12. No organic or polymeric materials shall be molded to the bottom of the package to cover leads.
13. For terminal connections, see [figure 4](#).
14. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 1. Dimensions and configuration for type 2N6987 - Continued.

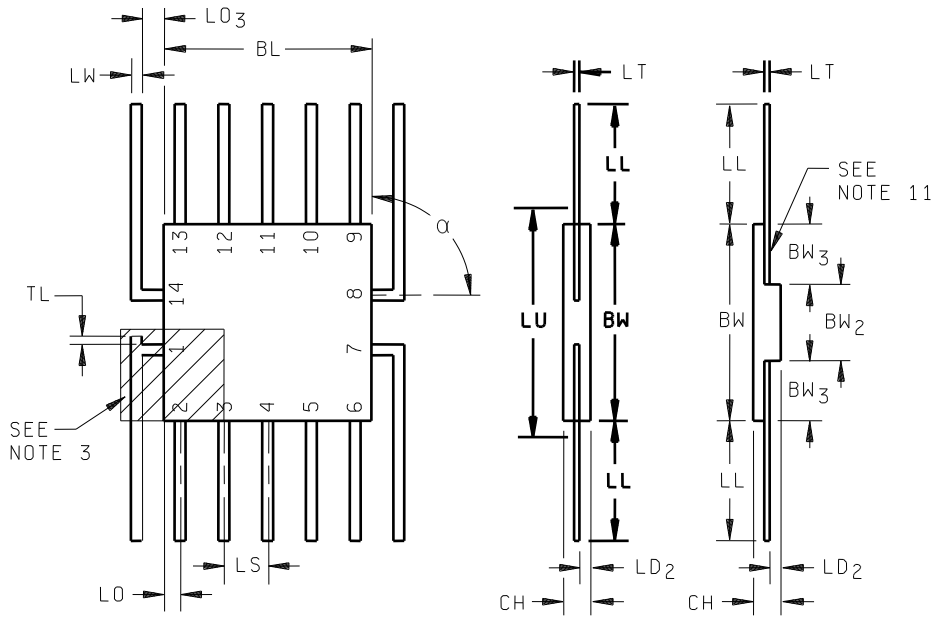


FIGURE 2. Physical dimensions for type 2N6988.

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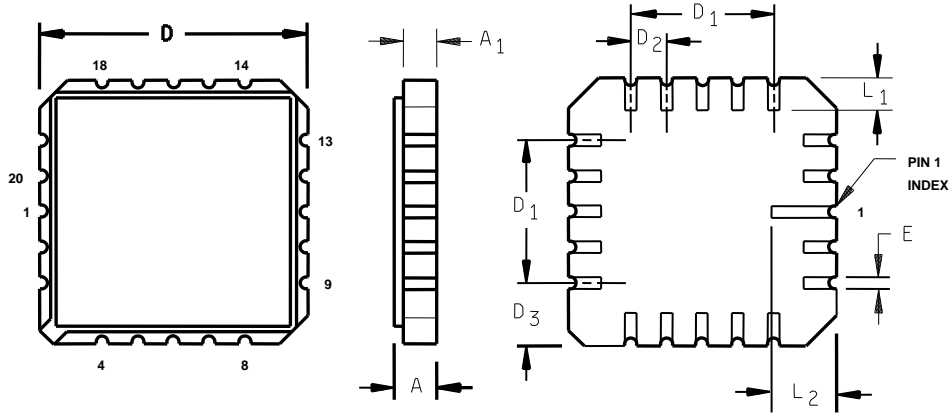
Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CH	.030	.115	0.76	2.92	
LW	.010	.019	0.25	0.48	7
TL	.008	.015	0.20	0.38	12
BL		.280		7.11	5
BW	.240	.260	6.10	6.60	
LU		.290		7.37	5
BW <sub>2</sub>	.125		3.18		

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BW <sub>3</sub>	.030		0.76		
LS	.050 BSC		1.27 BSC		6, 8
LT	.003	.006	0.076	0.152	7
LL	.250	.370	6.35	9.40	
LD <sub>2</sub>	.005	.040	0.13	1.02	4
LO	.005		0.13		9, 10
LO <sub>3</sub>	.004		0.10		13
$\alpha$	30°	90°	30°	90°	14

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Index area: A notch or pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dim TL) may be used to identify pin one.
4. Dimension LD<sub>2</sub> shall be measured at the point of exit of the lead from the body.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within  $\pm 0.005$  inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
7. All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat when the lead finish is solder.
8. Twelve spaces.
9. Applies to all four corners (leads number 2, 6, 9, and 13).
10. Dimension LO may be .000 inch (0.00 mm) if leads number 2, 6, 9, and 13) bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metallized ceramic body.
11. No organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
12. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply.
13. Applies to leads number 1, 7, 8, and 14.
14. Lead configuration is optional within dimension BW except dimensions LW and LT apply.
15. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.
16. Pins 1, 7, 8, and 14 are collectors.
17. Pins 2, 6, 9, and 13 are bases.
18. Pins 3, 5, 10, and 12 are emitters.
19. Pins 4 and 11 are no contacts.

FIGURE 2. Physical dimensions for type 2N6988 - Continued.

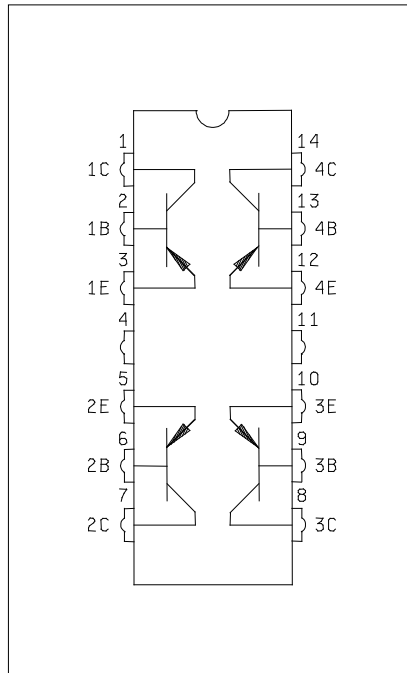


Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.073	.085	1.85	2.16
A <sub>1</sub>	.063	.075	1.60	1.90
D	.345	.355	8.76	9.02
D <sub>1</sub>	.195	.205	4.95	5.21
D <sub>2</sub>	.050 TYP		1.27 TYP	
D <sub>3</sub>	.070	.080	1.76	2.03
E	.025 REF		0.64 REF	
L <sub>1</sub>	.050 REF		1.27 REF	
L <sub>2</sub>	.080	.090	2.03	2.28

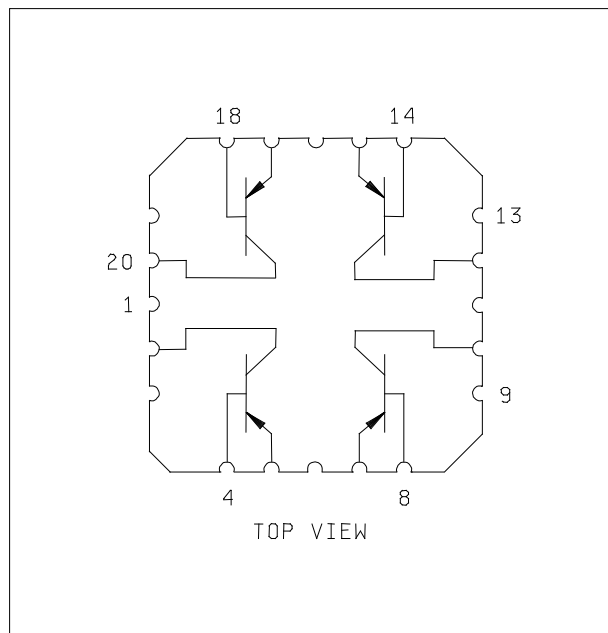
NOTES:

1. Dimensions are in inches.
2. Millimeters equivalents are given for general information only.
3. Unless otherwise specified, tolerance is  $\pm 0.005$  inch (0.13 mm).
4. For terminal connections, see figure 4.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 3. Physical dimensions for type 2N6987U.



14-lead flat-package or dual-in-line (top view)



20 pin leadless chip carrier (top view).

FIGURE 4. Schematic and terminal connections.

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1.4 Primary electrical characteristics. Characteristics apply to each transistor in the array.

Limits	$h_{FE2}$ (1) $V_{CE} = 10$ V dc $I_C = 1.0$ mA dc	$h_{FE4}$ (1) $V_{CE} = 10$ V dc $I_C = 150$ mA dc	$C_{obo}$ $V_{CB} = 10$ V dc $I_E = 0$ $100$ kHz $\leq f \leq 1$ MHz	Switching	
				$t_{on}$ see <a href="#">figure 13</a>	$t_{off}$ see <a href="#">figure 14</a>
Min	100	100	$\mu F$	ns	ns
Max	450	300	8	45	300

Limits	$ h_{fe} $ $V_{CE} = 20$ V dc $I_C = 50$ mA dc $f = 100$ MHz	$V_{CE(sat)2}$ (1) $I_C = 500$ mA dc $I_B = 50$ mA dc	$V_{BE(sat)2}$ (1) $I_C = 500$ mA dc $I_B = 50$ mA dc
Min	2.0	<u>V dc</u>	<u>V dc</u>
Max	8.0	1.6	2.6

(1) Pulsed (see [4.5.1](#)).

\* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

\* 1.5.1 JAN certification mark and quality level.

\* 1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

\* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for JANS devices in this specification sheet from lowest to highest are as follows: ("M", "D", "P", "L", "R", "F", "G", and "H"). The RHA levels that are applicable for JANTXV devices in this specification sheet from lowest to highest are as follows: ("R", and "F").

\* 1.5.3 Device type. The designation system for the device types of semiconductors covered by this specification sheet are as follows.

\* 1.5.3.1 First number and first letter symbols. The semiconductors of this specification sheet use the first number and letter symbols "2N".

\* 1.5.3.2 Second number symbols. The second number symbols for the semiconductors covered by this specification sheet are as follows: "6987", and "6988".

\* 1.5.4 Suffix symbols. The following suffix symbols are incorporated in the PIN for this specification sheet:

	A blank second suffix symbol indicates a 14-pin dual-in-line (2N6987) in accordance with <a href="#">figure 1</a> , or a 14-pin flat-pack (2N6988) in accordance with <a href="#">figure 2</a> .
U	Indicates a 20-pin leadless chip carrier. (see <a href="#">figure 3</a> ).

\* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).



## 2. APPLICABLE DOCUMENTS

\* 2.1 General. The documents listed in this section are specified in sections 3, and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <http://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1. General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2. Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3. Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

PCB	Printed circuit board.
$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JA(AM)}$	Thermal resistance ambient (adhesive mount to PCB).
$T_{A(AM)}$	Temperature ambient (adhesive mount to PCB).

3.4. Interface requirements and physical dimensions. The interface requirements and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1, 2, 3, and 4 herein.

3.4.1. Lead finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2. Schematic and terminal connections. The schematic and terminal connections shall be as shown on figure 4.

3.5. Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in MIL-PRF-19500.

3.6. Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7. Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8. Marking. Marking shall be in accordance with MIL-PRF-19500. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device "2N" identifier (depending upon degree of abbreviation required).

3.9. Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

### 4. VERIFICATION

4.1. Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 appendix E, and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen (see appendix E, table E-IV of MIL-PRF-19500)	Measurements	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750, see <a href="#">4.3.2</a> .	Thermal impedance, method 3131 of MIL-STD-750, see <a href="#">4.3.2</a> .
9	$I_{CBO2}$ and $h_{FE4}$	Not applicable.
10	24 hours minimum.	24 hours minimum.
11	$I_{CBO2}$ and $h_{FE4}$ $\Delta I_{CBO2}$ = 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4}$ = $\pm 15$ percent of initial value.	$I_{CBO2}$ and $h_{FE4}$
12	See <a href="#">4.3.1</a> .	See <a href="#">4.3.1</a> .
13	Subgroups 2 and 3 of <a href="#">table I</a> herein; $\Delta I_{CBO2}$ = 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4}$ = $\pm 15$ percent of initial value.	Subgroup 2 of <a href="#">table I</a> herein; $\Delta I_{CBO2}$ = 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE4}$ = $\pm 15$ percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; TX and TXV do not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:  $V_{CB} = 10 - 30$  V dc;  $P_T = 1.5$  W for 2N6987;  $P_T = 1.0$  W for 2N6987U, and  $P_T = 1.0$  W for 2N6988.  $T_A$  ambient rated as defined in [1.3](#). NOTE: No heat sink or forced air-cooling on the devices shall be permitted. Power ratings apply to total package. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions,  $T_J$ , and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed on each die in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{MD}$  (and  $V_C$  where appropriate). The thermal impedance limit shall comply with the thermal impedance graph on figures 9, 10, 11, and 12 (less than or equal to the curve value at the same  $t_H$  time) and shall be less than the process determined statistical maximum limit as outlined in method 3131. See [table II](#), subgroup 4 herein.

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4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of [table I](#), group A1 and group A2 inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with [4.4.2](#) herein).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and [table I](#) herein.

\* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-19500 and [4.4.2.1](#) herein. Delta requirements shall be in accordance with [4.5.5](#) herein, delta parameters apply to subgroups B4 and B5. See [4.4.2.2](#) for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in [4.4.2.2](#) and shall be in accordance with [table I](#), subgroup 2 and [4.5.5](#) herein.

4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$V_{CB} = 10 \text{ V dc}$ .
B5	1027	$V_{CB} = 10 \text{ V dc}$ , $P_D \geq 100$ percent of max rated $P_T$ (see <a href="#">1.3</a> ). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.)  Option 1: 96 hours minimum sample size in accordance with MIL-PRF-19500, table E-VIa, adjust $T_A$ or $P_D$ to achieve $T_J = +275^\circ\text{C}$ minimum.  Option 2: 216 hours minimum, sample size = 45, $c = 0$ ; adjust $T_A$ or $P_D$ to achieve $T_J = +225^\circ\text{C}$ minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10 \text{ V dc}$ , power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated $P_T$ as defined in <a href="#">1.3</a> . $n = 45$ devices, $c = 0$ .
2	1048	Blocking life, $T_A = +150^\circ\text{C}$ , $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$ .
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$ . $n = 22$ , $c = 0$ .

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.
- b. Shall be chosen from an inspection lot that has been submitted to and passed [table I](#), subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and in [4.4.3.1](#) (JANS).and [4.4.3.2](#) (JAN, JANTX, and JANTXV) herein for group C testing. Delta requirements shall be in accordance with [4.5.5](#) herein, delta parameters apply to subgroup C6.

4.4.3.1 Group C inspection, table E-VII (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, 3 ounce weight: Three bends of 15 degrees for 2N6988; three bends of 90 degrees for 2N6987; not applicable to 2N6987U.
C6	1026	1,000 hours at $V_{CB} = 10 - 30$ V dc; $T_J = +150^\circ\text{C}$ minimum. No heat sink or forced-air cooling on device shall be permitted.

4.4.3.2 Group C inspection, table E-VII (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, 3 ounce weight: Three bends of 15 degrees for 2N6988; three bends of 90 degrees for 2N6987; not applicable to 2N6987U.
C5	3131	$R_{\theta JA}$ , see <a href="#">1.3</a> .
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes group A tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in [table II](#) herein. These tests shall be performed as required in accordance with MIL-PRF-19500 and method 1019 of MIL-STD-750 for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence, as applicable (see [6.2](#) herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse affect to the fluence profile.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL-PRF-19500 and as specified in [table III](#) herein.

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4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.3 Independent transistor inspections. Inspections shall be performed on each transistor in the array.

4.5.4 Transistor-to-transistor resistance. The leads of each transistor shall be shorted together for this test. The resistance shall be measured between each transistor in the array.

4.5.5 Delta requirements. Delta requirements shall be as specified below:

Step	Inspection	MIL-STD-750		Symbol	Limit
		Method	Conditions		
1	Collector-base cutoff current	3036	Bias condition D, $V_{CB} = 50 \text{ V dc}$	$\Delta I_{CB02} (1)$	100 percent of initial value or $\pm 8 \text{ nA dc}$ , whichever is greater.
2	Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}$ ; $I_C = 150 \text{ mA dc}$ ; pulsed see <a href="#">4.5.1</a>	$\Delta h_{FE4} (1)$	$\pm 25$ percent change from initial reading.

(1) Devices which exceed the [table I](#) limits for this test shall not be accepted.

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TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to solvents 3/ 4/ 5/	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal 4/ Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements 4/		Table I, subgroup 2				
Bond strength 3/ 4/	2037	Precondition T <sub>A</sub> = +250°C at t = 24 hours or T <sub>A</sub> = +300°C at t = 2 hours. n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 1 device, c = 0				
<u>Subgroup 2</u>						
* Thermal impedance 6/	3131	See 4.3.2	Z <sub>θJX</sub>			°C/W
* Collector to base, cutoff current	3036	Bias condition D; V <sub>CB</sub> = 60 V dc	I <sub>CBO1</sub>		10	μA dc
* Emitter to base, cutoff current	3061	Bias condition D; V <sub>BE</sub> = 5 V dc	I <sub>EBO1</sub>		10	μA dc
Breakdown voltage collector to emitter	3011	Bias condition D; I <sub>C</sub> = 10 mA dc; pulsed (see 4.5.1)	V <sub>(BR)CEO</sub>	60		V dc
Collector to base cutoff current	3036	Bias condition D; V <sub>CB</sub> = 50 V dc	I <sub>CBO2</sub>		10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V <sub>EB</sub> = 4 V dc	I <sub>EBO2</sub>		50	nA dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 0.1 \text{ mA dc}$	$h_{FE1}$	75		
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 1.0 \text{ mA dc}$	$h_{FE2}$	100	450	
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc}$	$h_{FE3}$	100		
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc}$ pulsed (see 4.5.1)	$h_{FE4}$	100	300	
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 500 \text{ mA dc}$ pulsed (see 4.5.1)	$h_{FE5}$	50		
Collector to emitter voltage (saturated)	3071	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.4	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 500 \text{ mA dc}; I_B = 50 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.6	V dc
Base to emitter saturated voltage	3066	Test condition A; $I_C = 150 \text{ mA dc};$ $I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.3	V dc
Base to emitter saturated voltage	3066	Test condition A; $I_C = 500 \text{ mA dc};$ $I_B = 50 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)2}$		2.6	V dc
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +150^\circ\text{C}$				
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 50 \text{ V dc}$	$I_{CBO3}$		10	$\mu\text{A dc}$
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 1.0 \text{ mA dc}$	$h_{FE6}$	50		

See footnotes at end of table.



TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Small-signal short-circuit forward-current transfer ratio	3206	$V_{CE} = 10 \text{ V dc}; I_C = 1 \text{ mA dc}; f = 1 \text{ kHz}$	$h_{fe}$	100		
Magnitude of small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 20 \text{ V dc}; I_C = 50 \text{ mA dc}; f = 100 \text{ MHz}$	$ h_{fe} $	2.0	8.0	
Open circuit output capacitance	3236	$V_{CB} = 10 \text{ V dc}; I_E = 0; 100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	$C_{obo}$		8.0	pF
Input capacitance (output open-circuited)	3240	$V_{EB} = 2.0 \text{ V dc}; I_C = 0; 100 \text{ kHz} \leq f \leq 1 \text{ MHz}; \text{ see } 4.5.2$	$C_{ibo}$		30	pF
Turn-on time		See <a href="#">figure 13</a>	$t_{on}$		45	ns
Turn-off time		See <a href="#">figure 14</a>	$t_{off}$		300	ns
Transistor-to-transistor resistance		$ V_{T-T}  = 500 \text{ V dc}; \text{ see } 4.5.4$	$R_{T-T}$	$10^{10}$		ohms
<u>Subgroups 5 and 6</u>						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in group A, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for JANS devices.

5/ Not required for laser marked devices.

\* 6/ This test required for the following end-point measurements only:

Group B, subgroups 3, 4 and 5 (JANS).

Group B, step 1 (JAN, JANTX, JANTXV).

Group C, subgroups 2 and 6.

Group E, subgroup 1.

TABLE II. Group D inspection and end-point limits.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 4/</u>						
Neutron irradiation	1017	Neutron exposure $V_{CES} = 0$ V				
* Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 60$ V dc	$I_{CBO1}$		20	$\mu$ A dc
* Emitter to base cutoff current	3061	Bias condition D; $V_{BE} = 5$ V dc	$I_{EBO1}$		20	$\mu$ A dc
Breakdown voltage collector to emitter	3011	Bias condition D; $I_C = 10$ mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 50$ V dc	$I_{CBO2}$		20	$\eta$ A dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 4.0$ V dc	$I_{EBO2}$		100	$\eta$ A dc
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 0.1$ mA dc	$[h_{FE1}] \underline{5/}$	[37.5]		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 1.0$ mA dc	$[h_{FE2}] \underline{5/}$	[50]	450	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 10$ mA dc	$[h_{FE3}] \underline{5/}$	[50]		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 150$ mA dc; pulsed (see 4.5.1)	$[h_{FE4}] \underline{5/}$	[50]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 500$ mA dc; pulsed (see 4.5.1)	$[h_{FE5}] \underline{5/}$	[25]		
Collector to emitter voltage (saturated)	3071	$I_C = 150$ mA dc, $I_B = 15$ mA dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.46	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 500$ mA dc, $I_B = 50$ mA dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.84	V dc
Base to emitter saturated voltage	3066	Test condition A, $I_C = 150$ mA dc, $I_B = 15$ mA dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.50	V dc
Base to emitter saturated voltage	3066	Test condition A, $I_C = 500$ mA dc, $I_B = 50$ mA dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		3.00	V dc

See footnotes at end of table.

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TABLE II. Group D inspection and end-point limits – Continued.

Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u>						
Steady-state total dose irradiation	1019	Gamma exposure $V_{ECS} = 48$ V				
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 60$ V dc	$I_{CBO1}$		20	$\mu$ A dc
Emitter to base cutoff current	3061	Bias condition D; $V_{BE} = 5$ V dc	$I_{EBO1}$		20	$\mu$ A dc
Breakdown voltage Collector to emitter	3011	Bias condition D; $I_C = 10$ mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	60		V dc
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 50$ V dc	$I_{CBO2}$		20	$\eta$ A dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 4.0$ V dc	$I_{EBO2}$		100	$\eta$ A dc
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 0.1$ mA dc	$[h_{FE1}]$ <u>5/</u>	[37.5]		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 1.0$ mA dc	$[h_{FE2}]$ <u>5/</u>	[50]	450	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 10$ mA dc	$[h_{FE3}]$ <u>5/</u>	[50]		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 150$ mA dc; pulsed (see 4.5.1)	$[h_{FE4}]$ <u>5/</u>	[50]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc, $I_C = 500$ mA dc; pulsed (see 4.5.1)	$[h_{FE5}]$ <u>5/</u>	[25]		
Collector to emitter voltage (saturated)	3071	$I_C = 150$ mA dc, $I_B = 15$ mA dc, pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.46	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 500$ mA dc, $I_B = 50$ mA dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		1.84	V dc
Base to emitter saturated voltage	3066	Test condition A, $I_C = 150$ mA dc, $I_B = 15$ mA dc, pulsed (see 4.5.1)	$V_{BE(sat)1}$		1.50	V dc
Base to emitter saturated voltage	3066	Test condition A, $I_C = 500$ mA dc, $I_B = 50$ mA dc, pulsed (see 4.5.1)	$V_{BE(sat)2}$		3.00	V dc

1/ Tests to be performed on all devices receiving radiation exposure.

2/ For sampling plan, see MIL-PRF-19500.

3/ Electrical characteristics apply to all device types unless otherwise noted.

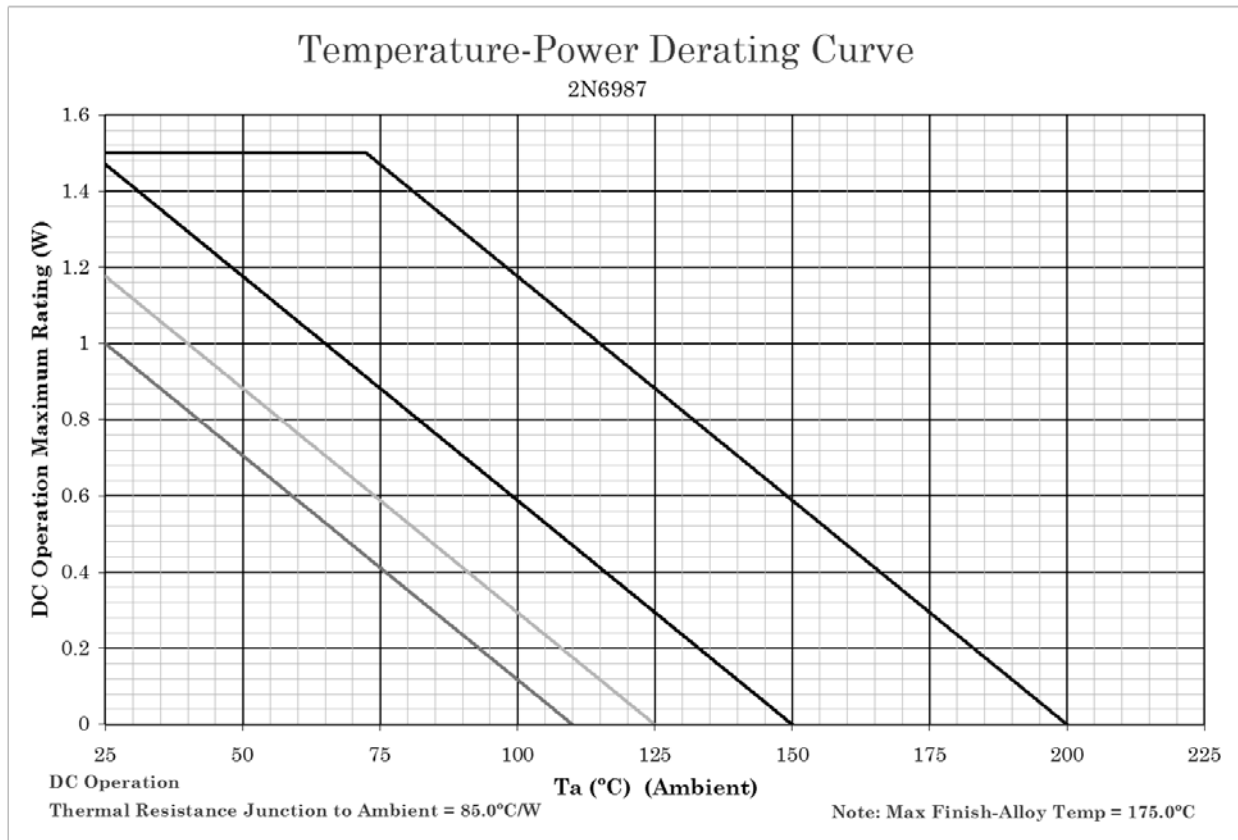
4/ See 6.2.e herein.

5/ See method 1019 of MIL-STD-750 for how to determine  $[h_{FE}]$  by first calculating the delta ( $1/h_{FE}$ ) from the pre and post-radiation  $h_{FE}$ . Notice that  $[h_{FE}]$  is not the same as  $h_{FE}$  and cannot be measured directly. The  $[h_{FE}]$  value can never exceed the pre-radiation minimum  $h_{FE}$  that it is based upon.

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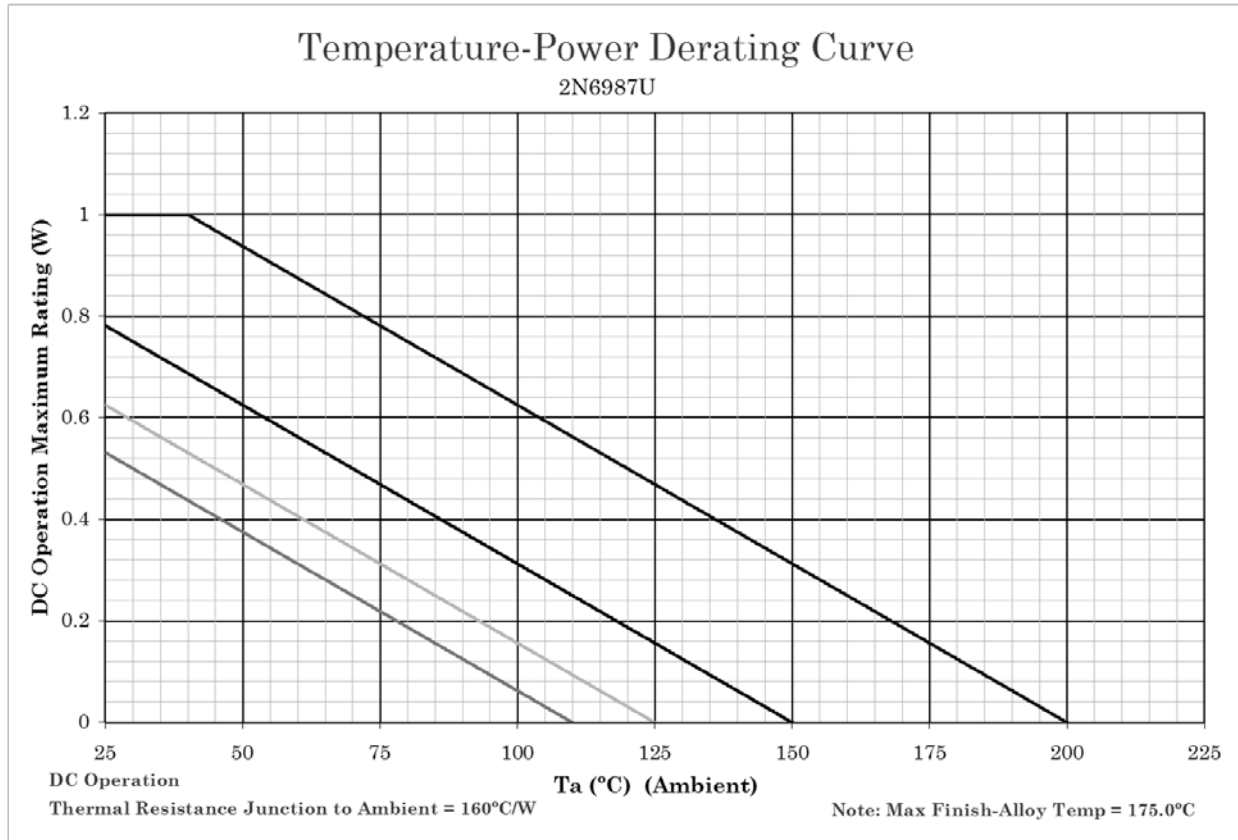
TABLE III. Group E inspection (all quality levels) - for qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See <a href="#">table I</a> , subgroup 2 and <a href="#">4.5.5</a> herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} = 10 - 30$ V dc, 6,000 cycles. Adjust device current, or power, to achieve a minimum $\Delta T_J$ of +100°C.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2 and <a href="#">4.5.5</a> herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See MIL-PRF-19500.	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			
ESD	1020		11 devices
<u>Subgroup 8</u>			
Reverse stability	1033	Condition B.	45 devices c = 0

**NOTES:**

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

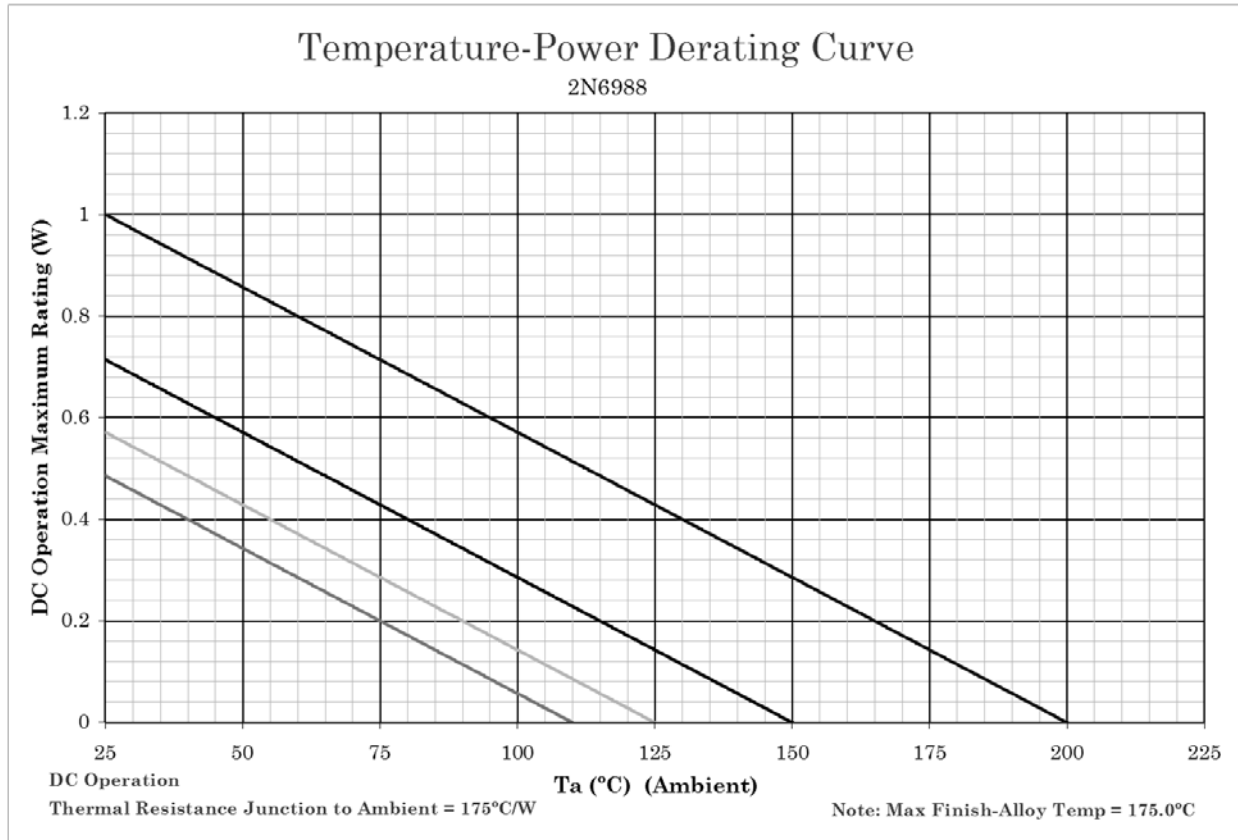
FIGURE 5. Temperature-power derating ( $R_{\theta JA}$ ) for 2N6987 (DIP14).



## NOTES:

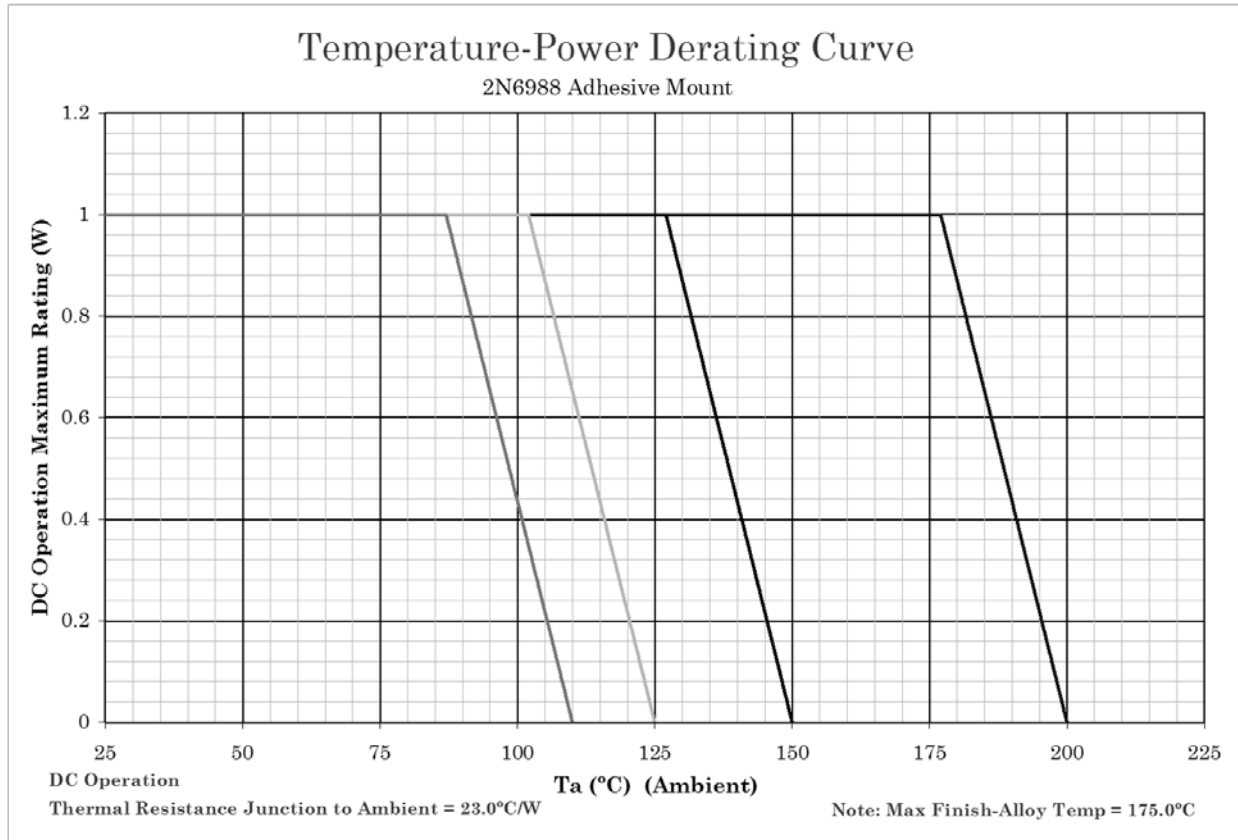
1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 6. Temperature-power derating ( $R_{\theta JA}$ ) for 2N6987U, (20 pin leadless chip).

**NOTES:**

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 7. Temperature-power derating ( $R_{\theta JA}$ ) for 2N6988 (14 pin flat pack).



## NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperature ( $T_J \leq 200^\circ\text{C}$ ) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq 150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq 125^\circ\text{C}$ , and  $110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 8. Temperature-power derating ( $R_{\theta JC(AM)}$ ) for 2N6988 (14 pin flat pack epoxy mount).



### Maximum Thermal Impedance

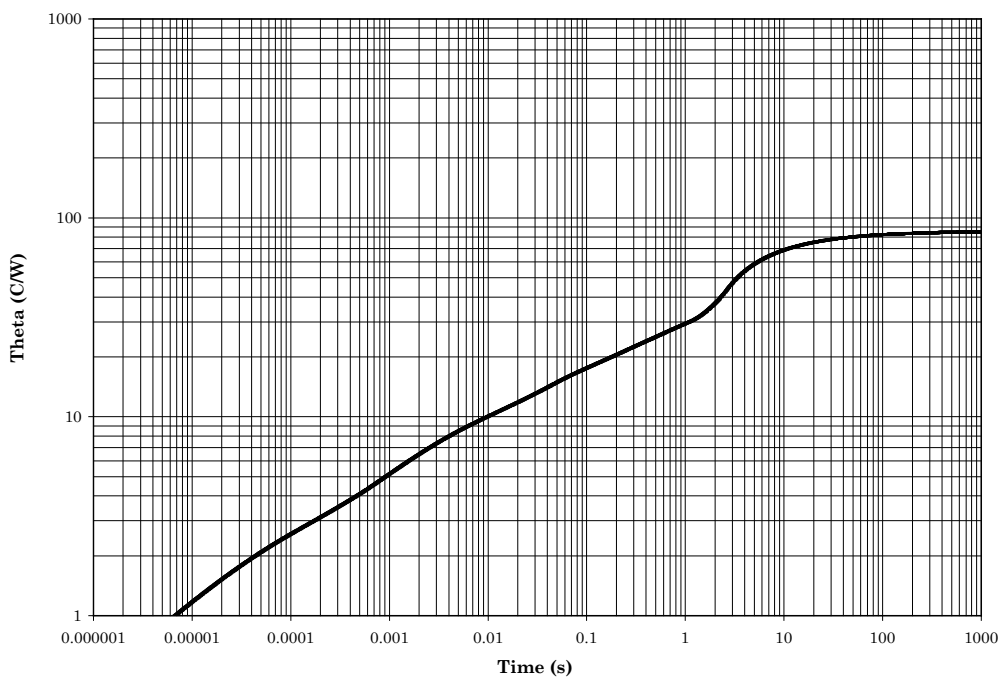


FIGURE 9. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N6987 (DIP14).

### Maximum Thermal Impedance

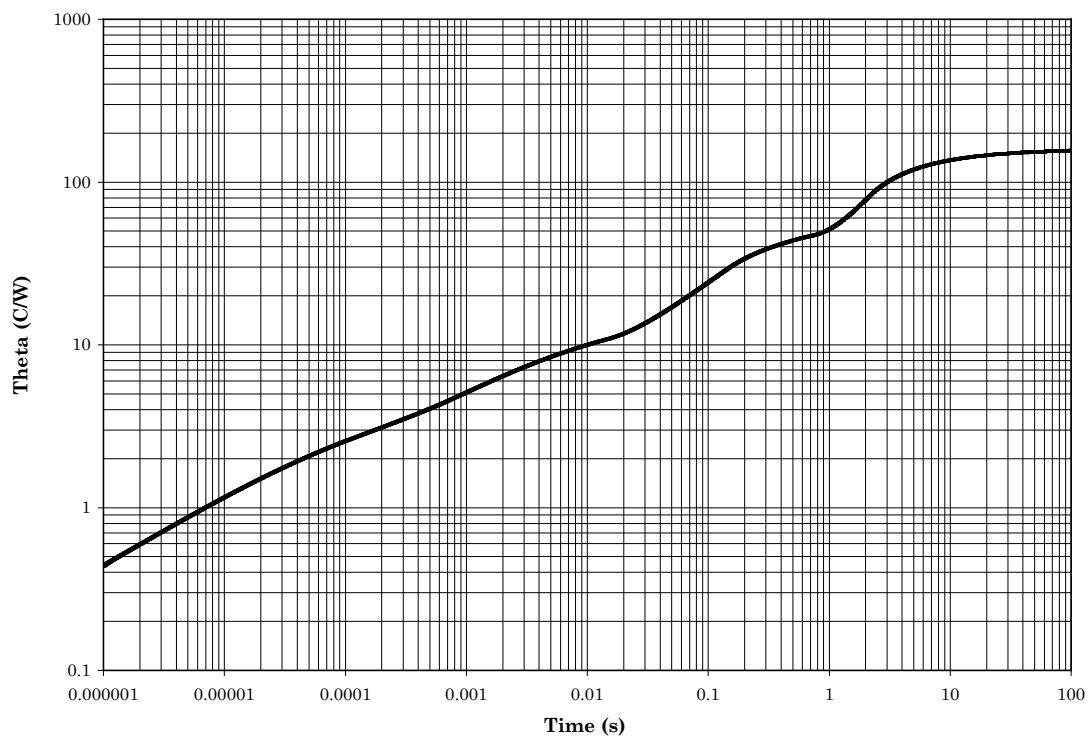


FIGURE 10. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N6987U (20 pin leadless chip).

### Maximum Thermal Impedance

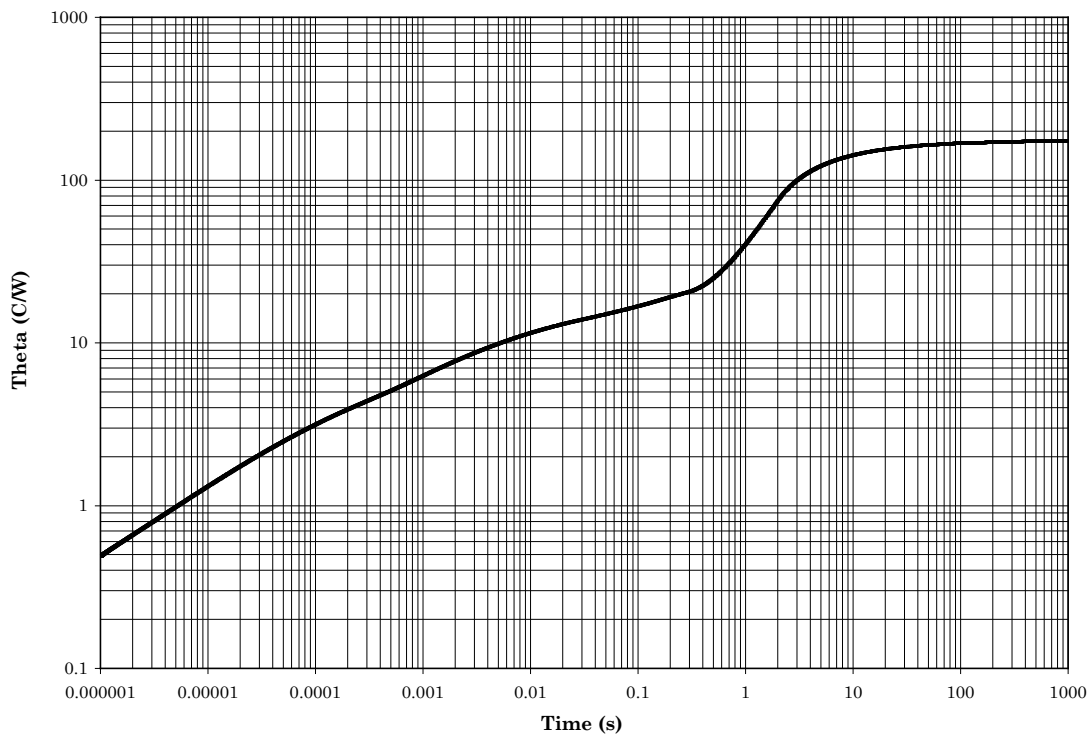


FIGURE 11. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N6988 (14 pin flat pack).

### Maximum Thermal Impedance

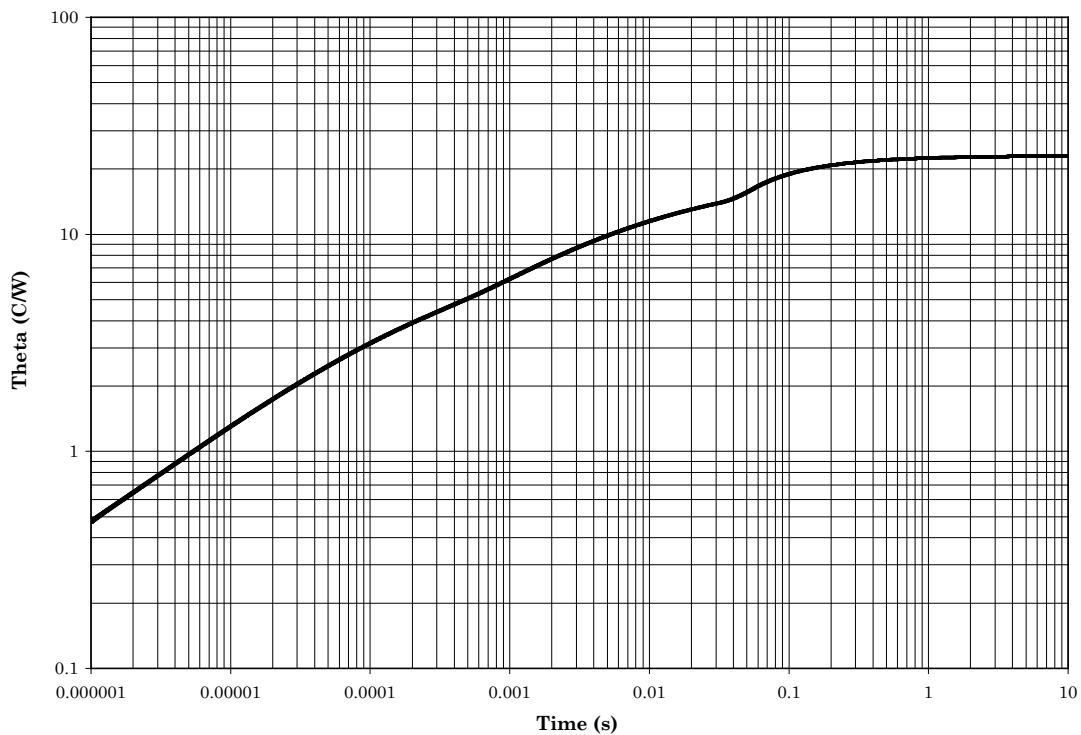
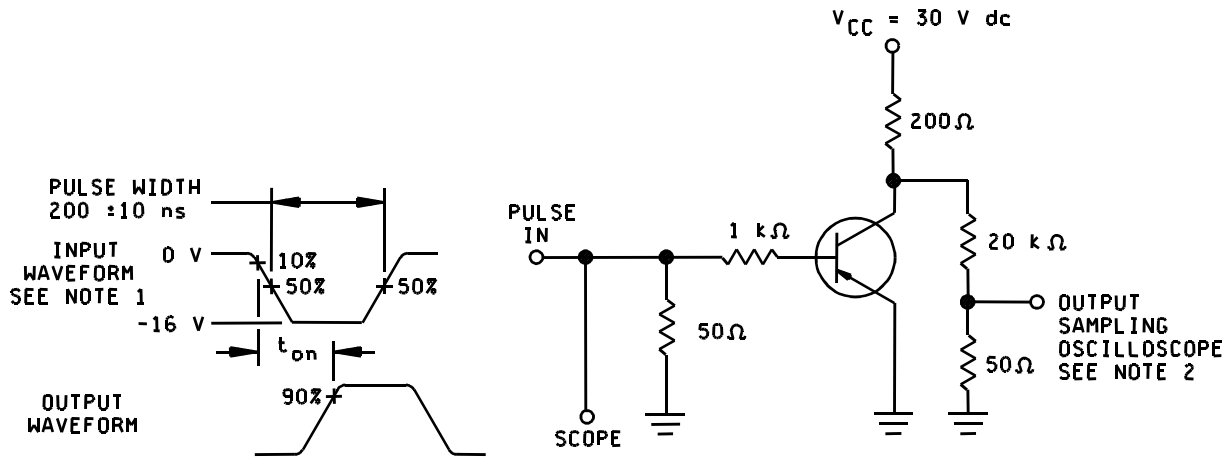


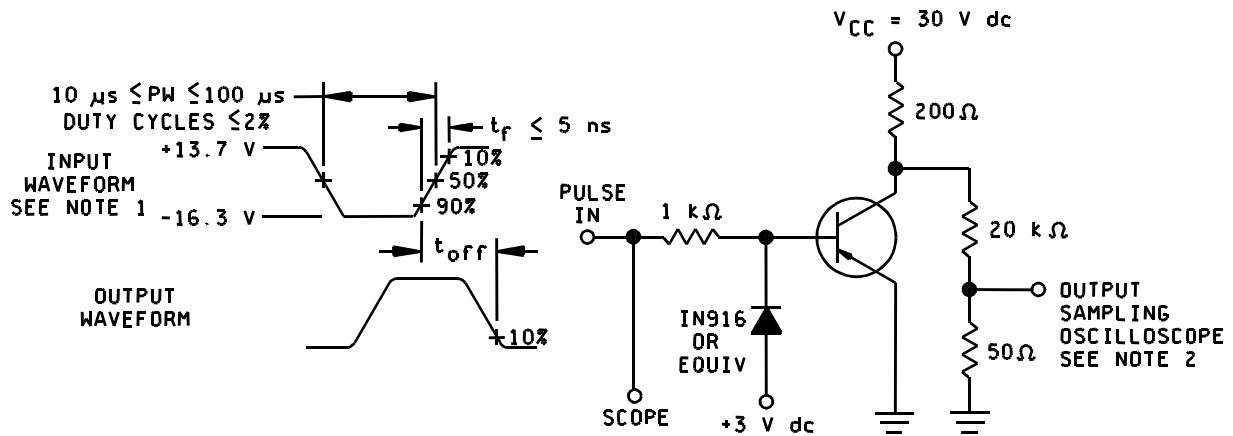
FIGURE 12. Thermal impedance graph ( $R_{\theta JC(AM)}$ ) for 2N6988 (14 pin flat pack epoxy mount).



NOTES:

1. The rise time ( $t_r$ ) and fall time ( $t_f$ ) of the applied pulse shall be each  $\leq 2.0 \text{ ns}$ ; duty cycle  $\leq 2$  percent; generator source impedance shall be  $50 \Omega$ .
2. Output sampling oscilloscope:  $Z_{in} \geq 100 \text{ k}\Omega$ ;  $C_{in} \leq 12 \text{ pF}$ ; rise time  $\leq 5.0 \text{ ns}$ .

FIGURE 13. Saturated turn-on switching time test circuit and waveform.



NOTES:

1. The rise time ( $t_r$ ) and fall time ( $t_f$ ) of the applied pulse shall be each  $\leq 2.0 \text{ ns}$ ; duty cycle  $\leq 2$  percent; generator source impedance shall be  $50 \Omega$ .
2. Output sampling oscilloscope:  $Z_{in} \geq 100 \text{ k}\Omega$ ;  $C_{in} \leq 12 \text{ pF}$ ; rise time  $\leq 5.0 \text{ ns}$ .

FIGURE 14. Saturated turn-off switching time test circuit and waveform.

## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

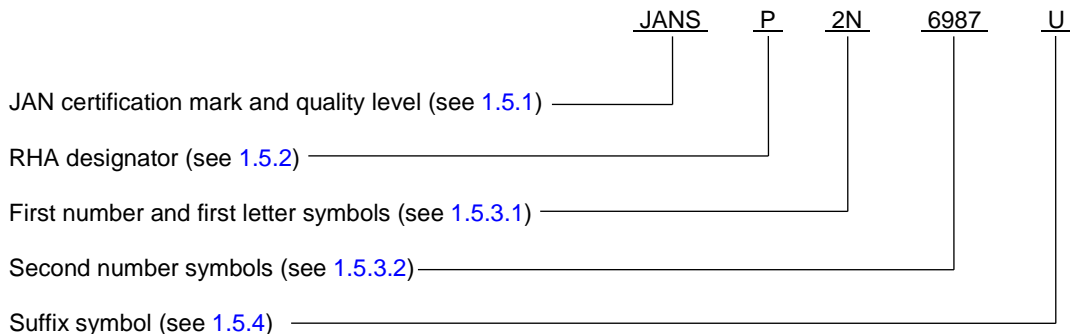
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.
- \* e. The complete Part or Identifying Number (PIN), see 1.5 and 6.4.
- f. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it should be specified in the contract.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

\* 6.4 PIN construction example.

\* 6.4.1 Encapsulated devices. The PINs for encapsulated devices are constructed using the following form.



\* 6.5 List of PINs.

\* 6.5.1 PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for types 2N6987 (1)	PINs for types 2N6988 (1)
JAN2N6987	JAN2N6988
JAN2N6987U	JANTX2N6988
JANTX2N6987	JANTXV2N6988
JANTX2N6987U	JANTXVR2N6988
JANTXV2N6987	JANTXVF2N6988
JANTXV2N6987U	JANS2N6988
JANTXVR2N6987	JANS#2N6988
JANTXVF2N6987	
JANTXVR2N6987U	
JANTXVF2N6987U	
JANS2N6987	
JANS2N6987U	
JANS#2N6987	
JANS#2N6987U	

(1) The number sign (#) represents one of eight RHA designators available (M, D, P, L, R, F, G, or H).

\* 6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR  
Navy - EC  
Air Force - 85  
DLA - CC

Preparing activity:

DLA - CC

(Project 5961-2015-057)

Review activities:

Army - AR, MI, SM  
Navy - AS  
Air Force - 19, 71, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.