

Q1PACK Module

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

This high-density, integrated power module combines high-performance IGBTs with rugged anti-parallel diodes.

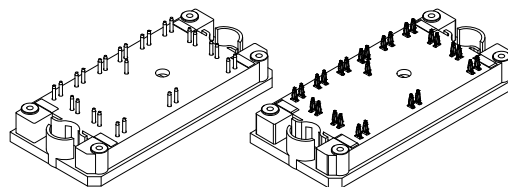
Features

- Extremely Efficient Trench with Fieldstop Technology
- Low Switching Loss Reduces System Power Dissipation
- Module Design Offers High Power Density
- Low Inductive Layout
- Q1PACK Packages with Solder and Pressfit Pins

Typical Applications

- Solar Inverters
- Uninterruptable Power Supplies

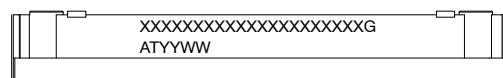
50 A, 650 V Module



PIM27, 71x37.4
(SOLDER PIN)
CASE 180CA

PIM27, 71x37.4
(PRESSFIT PIN)
CASE 180CP

MARKING DIAGRAM



XXXXXX = Specific Device Code
G = Pb-Free Package
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

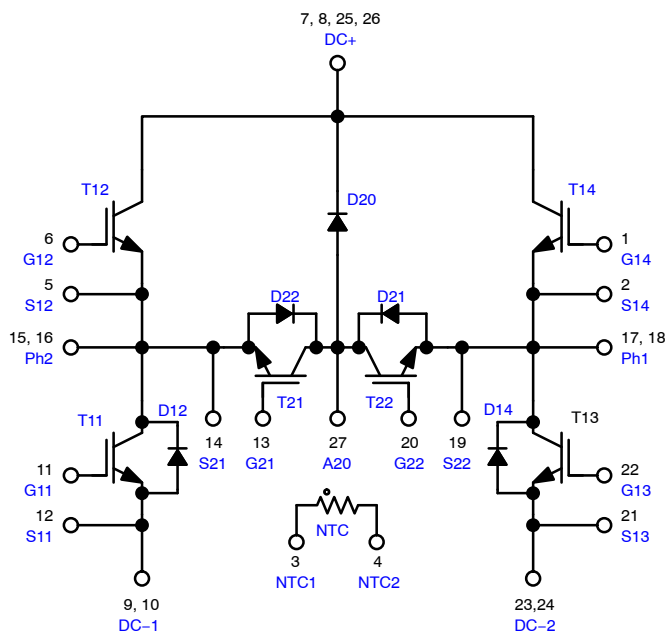


Figure 1. Schematic

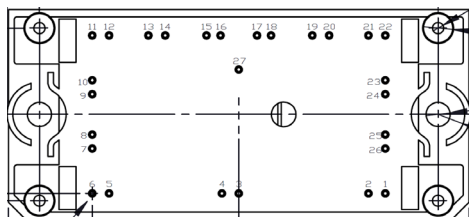


Figure 2. Pin Assignments

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IGBT (T11, T12, T13, T14, T21, T22)			
Collector-emitter voltage	V_{CES}	650	V
Collector current @ $T_h = 80^\circ\text{C}$ (per IGBT)	I_C	48	A
Pulsed collector current, T_{pulse} limited by $T_{j\text{max}}$	I_{CM}	144	A
Power Dissipation Per IGBT $T_j = T_{j\text{max}}, T_h = 80^\circ\text{C}$	P_{tot}	72	W
Gate-emitter voltage	V_{GE}	± 20	V
Maximum Junction Temperature	T_J	175	$^\circ\text{C}$

DIODE (D12, D14, D20, D21, D22)

Peak Repetitive Reverse Voltage	V_{RRM}	650	V
Forward Current, DC @ $T_h = 80^\circ\text{C}$ (per Diode)	I_F	50	A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	225	A
Power Dissipation Per Diode $T_j = T_{j\text{max}}, T_h = 80^\circ\text{C}$	P_{tot}	86	W
Maximum Junction Temperature	T_J	175	$^\circ\text{C}$

THERMAL PROPERTIES

Operating Temperature under switching condition	$T_{VJ\text{OP}}$	-40 to ($T_{j\text{max}} - 25$)	$^\circ\text{C}$
Storage Temperature range	T_{stg}	-40 to 125	$^\circ\text{C}$

INSULATION PROPERTIES

Isolation test voltage, $t = 2$ min, 60 Hz	V_{is}	4000	Vac
Creepage distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
IGBT (T11, T12, T13, T14, T21, T22)						
Collector-emitter cutoff current	$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}$	I_{CES}	-	-	300	μA
Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}, I_C = 50\text{ A}, T_j = 25^\circ\text{C}$ $V_{GE} = 15\text{ V}, I_C = 50\text{ A}, T_j = 150^\circ\text{C}$	$V_{CE(\text{sat})}$	-	1.56 1.76	2.22 -	V
Gate-emitter threshold voltage	$V_{GE} = V_{CE}, I_C = 50\text{ mA}$	$V_{GE(\text{TH})}$	3.1	4.45	5.2	V
Gate leakage current	$V_{GE} = 20\text{ V}, V_{CE} = 0\text{ V}$	I_{GES}	-	-	400	nA
Turn-on delay time	$T_j = 25^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 50\text{ A}$ $V_{GE} = 15\text{ V}, -9\text{ V}, R_G = 6\ \Omega$	$t_{d(\text{on})}$	-	14	-	ns
Rise time		t_r	-	20	-	
Turn-off delay time		$t_{d(\text{off})}$	-	68	-	
Fall time		t_f	-	20	-	
Turn on switching loss		E_{on}	-	0.46	-	mJ
Turn off switching loss		E_{off}	-	0.44	-	
Turn-on delay time	$T_j = 125^\circ\text{C}$ $V_{CE} = 350\text{ V}, I_C = 50\text{ A}$ $V_{GE} = 15\text{ V}, -9\text{ V}, R_G = 6\ \Omega$	$t_{d(\text{on})}$	-	16	-	ns
Rise time		t_r	-	23	-	
Turn-off delay time		$t_{d(\text{off})}$	-	78	-	
Fall time		t_f	-	52	-	
Turn on switching loss		E_{on}	-	0.78	-	mJ
Turn off switching loss		E_{off}	-	0.60	-	

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
IGBT (T11, T12, T13, T14, T21, T22)						
Input capacitance	V _{CE} = 20 V, V _{GE} = 0 V, f = 1 MHz	C _{ies}	–	3137	–	pF
Output capacitance		C _{oes}	–	146	–	
Reverse transfer capacitance		C _{res}	–	17	–	
Gate charge total	V _{CE} = 350 V, I _C = 40 A, V _{GE} = ±15 V	Q _g	–	180	–	nC
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness = 2.1 Mil ±2% λ = 2.9 W/mK	R _{thJH}	–	1.32	–	°C/W
Thermal Resistance – chip–to–case		R _{thJC}	–	0.96	–	°C/W

IGBT INVERSE DIODE (D12, D14, D21, D22)

Forward voltage	I _F = 50 A, T _J = 25°C I _F = 50 A, T _J = 175°C	V _F	– –	2.25 1.7	2.7 –	V
Reverse Recovery Time	T _J = 25°C V _{CE} = 350 V, I _C = 50 A V _{GE} = 15 V, –9 V, R _G = 6 Ω	t _{rr}	–	28	–	ns
Reverse Recovery Current		Q _{rr}	–	281	–	nc
Peak Reverse Recovery Current		I _{rrm}	–	18	–	A
Peak Rate of Fall of Recovery Current		Di/dt _{max}	–	1.42	–	A/μs
Reverse Recovery Energy		E _{rr}	–	33	–	μJ
Reverse Recovery Time	T _J = 125°C V _{CE} = 350 V, I _C = 50 A V _{GE} = 15 V, –9 V, R _G = 6 Ω	t _{rr}	–	65	–	ns
Reverse Recovery Current		Q _{rr}	–	1094	–	nc
Peak Reverse Recovery Current		I _{rrm}	–	33	–	A
Peak Rate of Fall of Recovery Current		Di/dt _{max}	–	1.32	–	A/μs
Reverse Recovery Energy		E _{rr}	–	198	–	μJ
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness = 2.1 Mil ±2% λ = 2.9 W/mK	R _{thJH}	–	1.10	–	°C/W
Thermal Resistance – chip–to–case		R _{thJC}	–	0.79	–	°C/W

DIODE (D20)

Forward voltage	I _F = 50 A, T _J = 25°C I _F = 50 A, T _J = 175°C	V _F	– –	2.25 1.7	2.7 –	V
Reverse leakage current	V _{CE} = 650 V, V _{GE} = 0 V	I _r	–	–	300	μA
Thermal Resistance – chip–to–heatsink	Thermal grease, Thickness = 2.1 Mil ±2% λ = 2.9 W/mK	R _{thJH}	–	1.10	–	°C/W
Thermal Resistance – chip–to–case		R _{thJC}	–	0.79	–	°C/W

THERMISTOR CHARACTERISTICS

Nominal resistance	T = 25°C	R ₂₅	–	22	–	kΩ
Nominal resistance	T = 100°C	R ₁₀₀	–	1486	–	Ω
Deviation of R25		R/R	–5	–	5	%
Power dissipation		P _D	–	200	–	mW
Power dissipation constant			–	2	–	mW/°C
B-value	B (25/50), tol ±3%		–	–	3950	°C
B-value	B (25/100), tol ±3%		–	–	3998	°C
NTC reference			–	–	B	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

TYPICAL CHARACTERISTICS – IGBT (T11, T12, T13, T14, T21, T22)

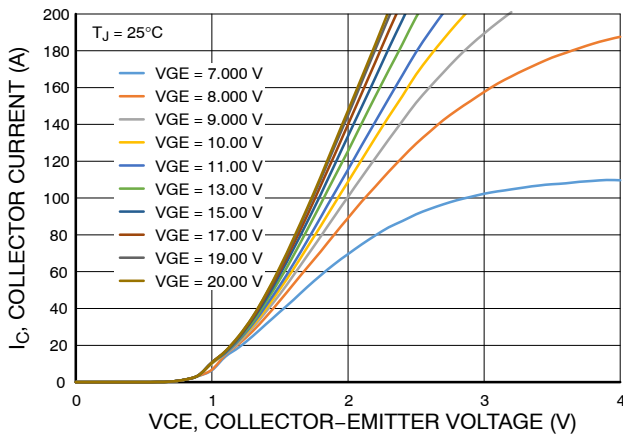


Figure 3. Typical Output Characteristics

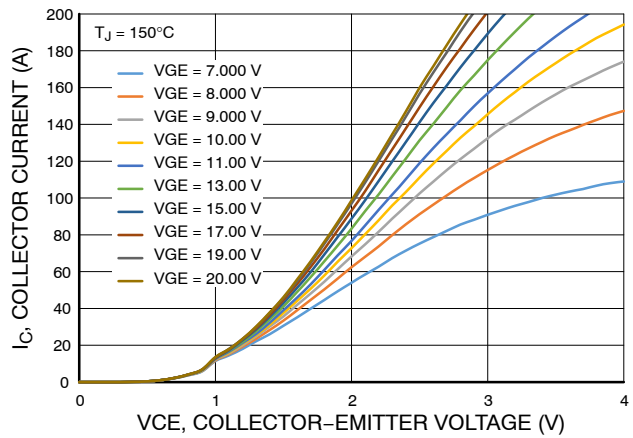


Figure 4. Typical Output Characteristics

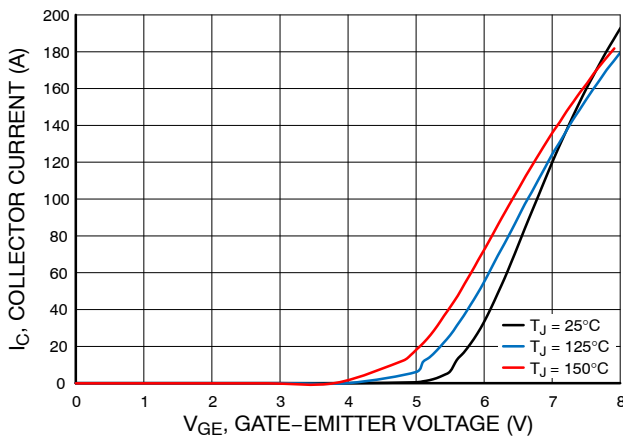


Figure 5. Typical Transfer Characteristics

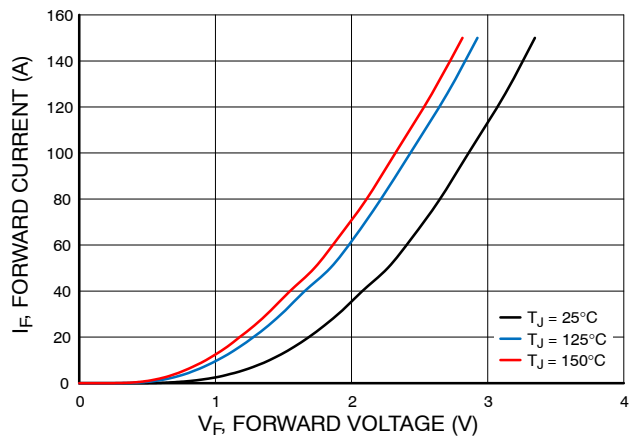


Figure 6. Diode Forward Characteristics

TYPICAL CHARACTERISTICS – (T11, T12, T13, T14) IGBT COMMUTATES D21, D22 DIODE

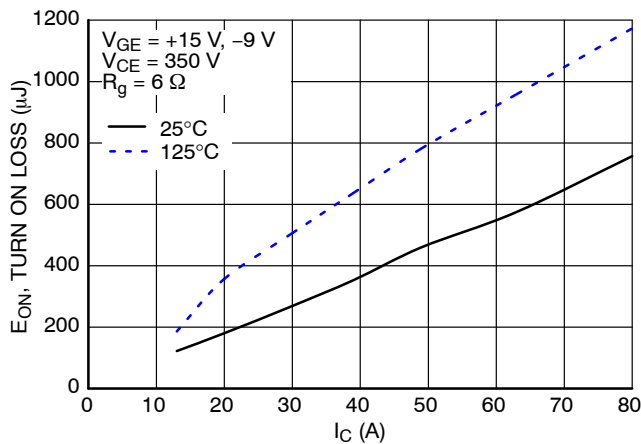


Figure 7. Typical Turn ON Loss vs. IC

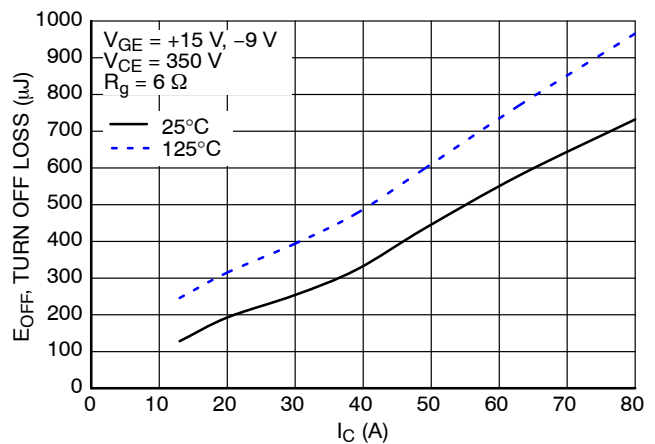


Figure 8. Typical Turn OFF Loss vs. IC

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

TYPICAL CHARACTERISTICS – (T11, T12, T13, T14) IGBT COMMUTATES D21, D22 DIODE (CONTINUED)

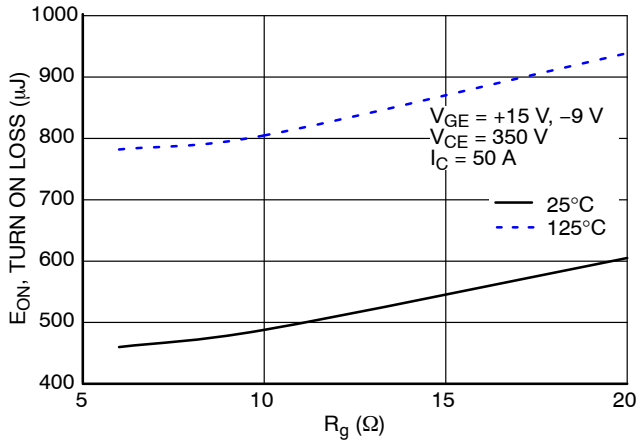


Figure 9. Typical Turn ON Loss vs. Rg

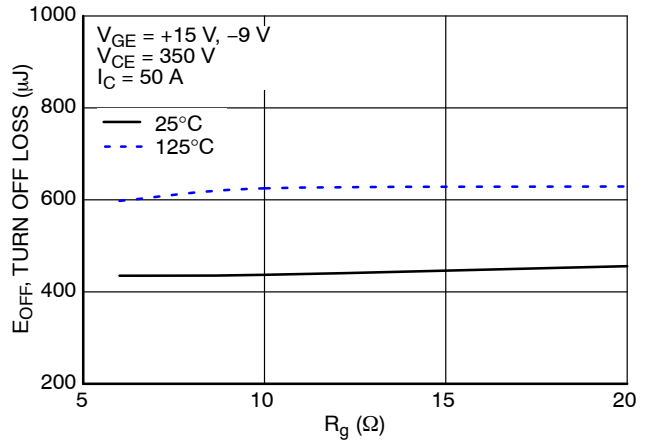


Figure 10. Typical Turn OFF Loss vs. Rg

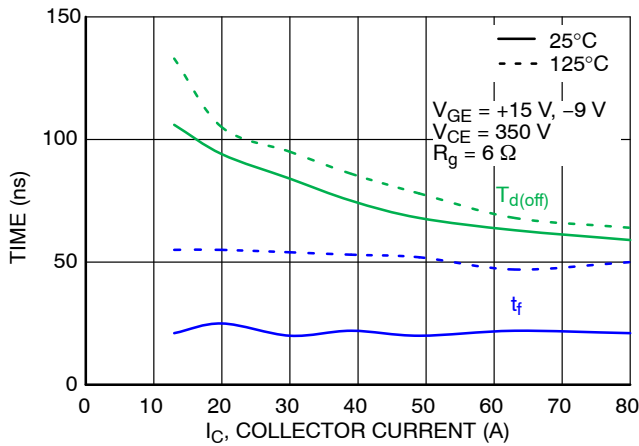


Figure 11. Typical Turn-Off Switching Time vs. IC

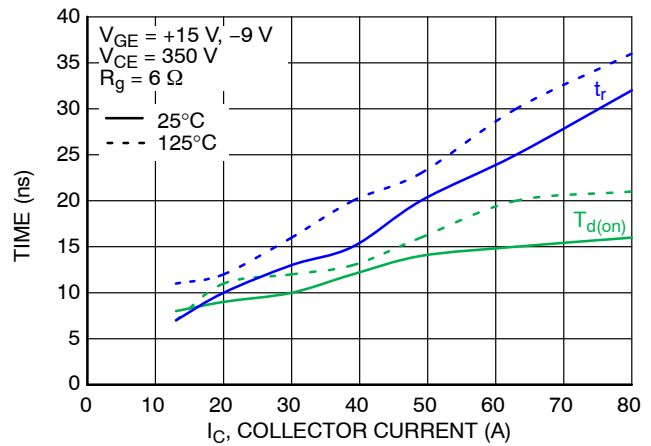


Figure 12. Typical Turn-On Switching Time vs. IC

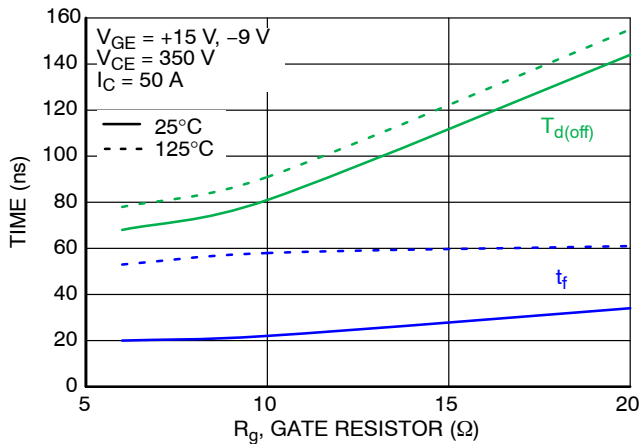


Figure 13. Typical Turn-Off Switching Time vs. Rg

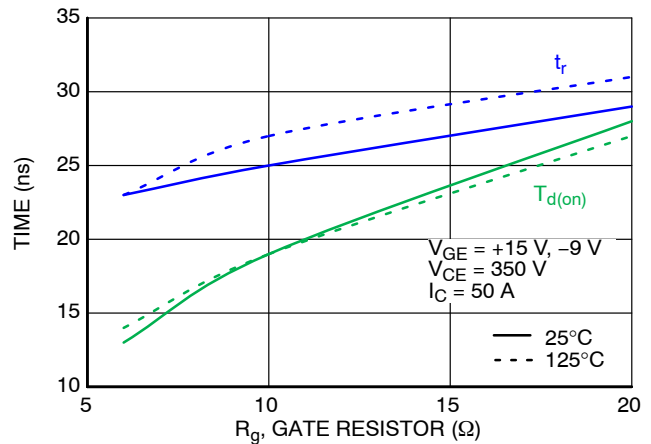


Figure 14. Typical Turn-On Switching Time vs. Rg

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

TYPICAL CHARACTERISTICS – (T21, T22) IGBT COMMUTATES D20 DIODE

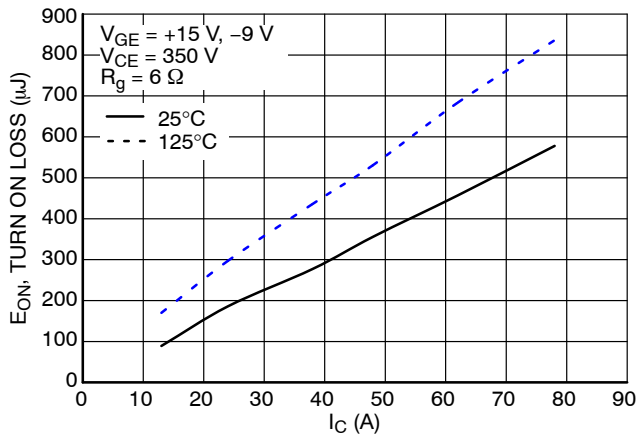


Figure 15. Typical Turn ON Loss vs. IC

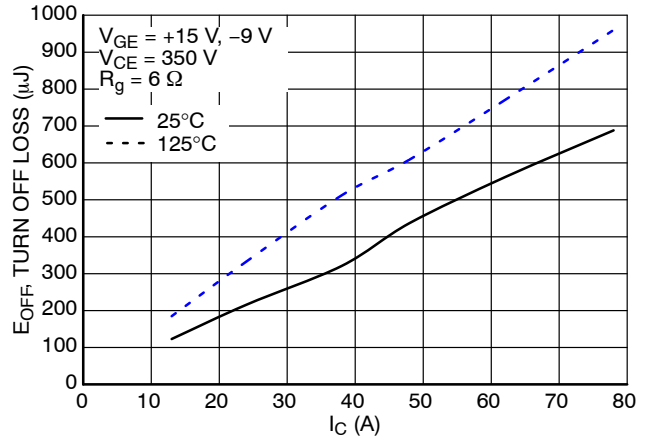


Figure 16. Typical Turn OFF Loss vs. IC

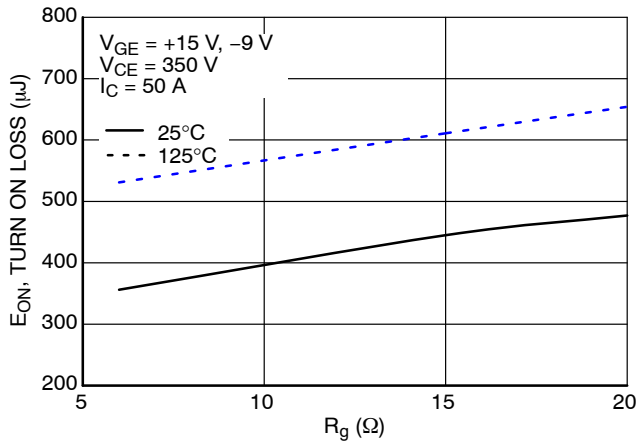


Figure 17. Typical Turn ON Loss vs. R_G

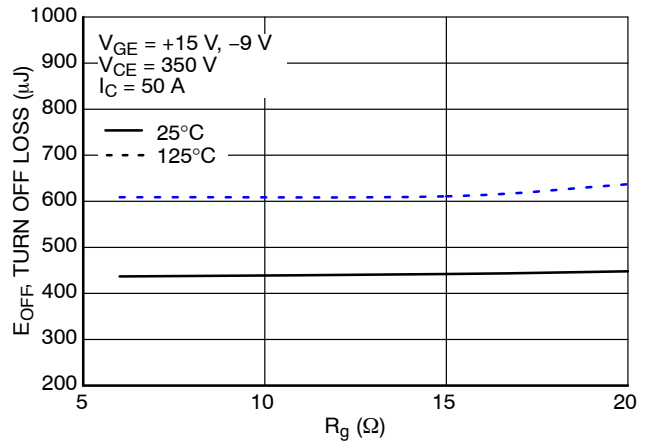


Figure 18. Typical Turn OFF Loss vs. R_G

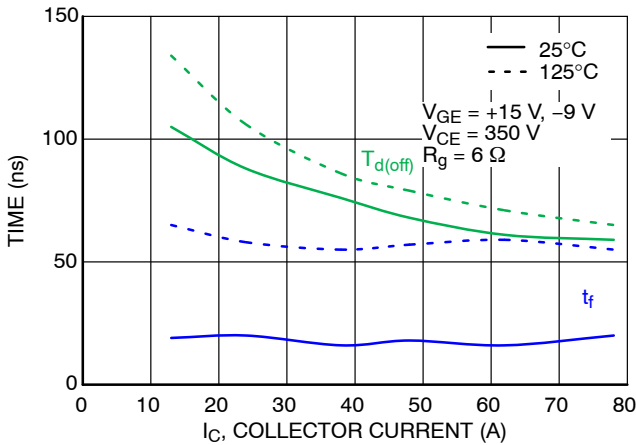


Figure 19. Typical Turn-Off Switching Time vs. IC

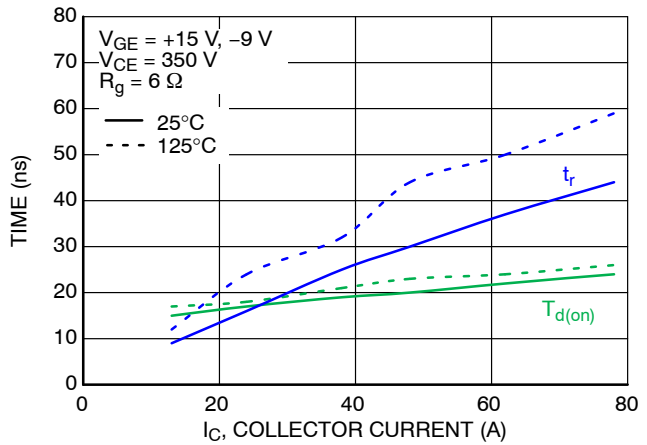


Figure 20. Typical Turn-On Switching Time vs. IC

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

TYPICAL CHARACTERISTICS – (T21, T22) IGBT COMMUTATES D20 DIODE (CONTINUED)

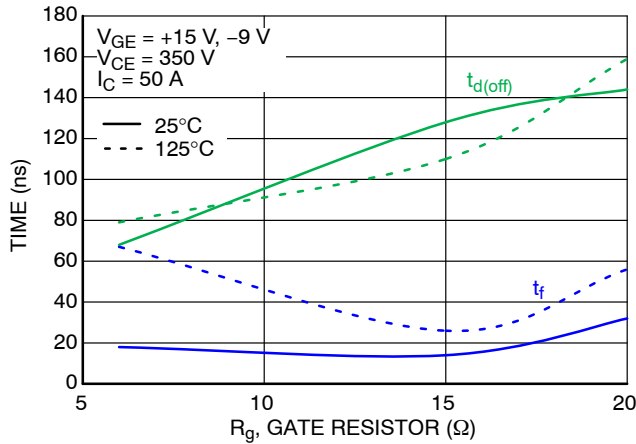


Figure 21. Typical Turn-Off Switching Time vs. R_g

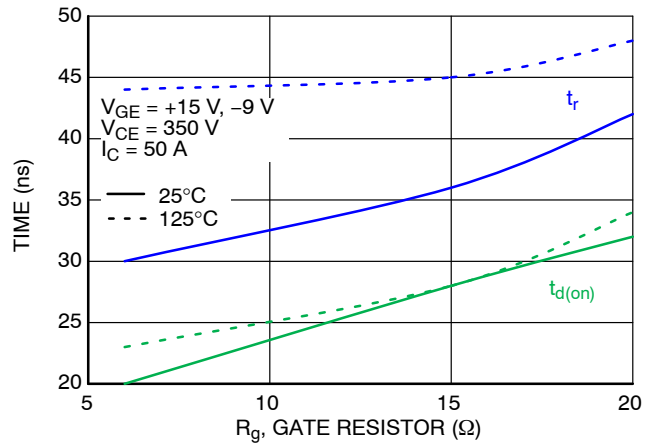


Figure 22. Typical Turn-On Switching Time vs. R_g

TYPICAL CHARACTERISTICS – DIODE

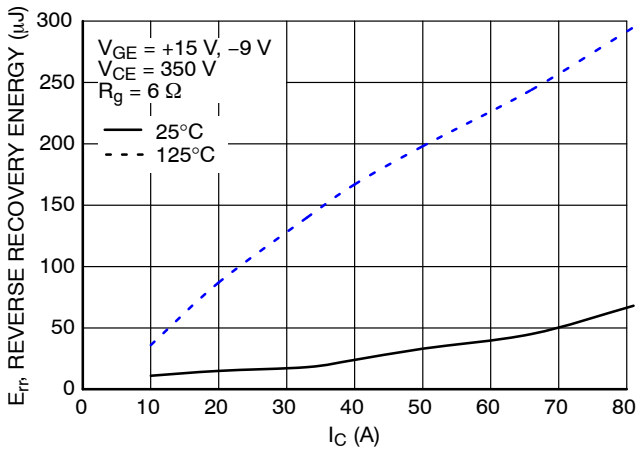


Figure 23. Typical Reverse Recovery Energy Loss vs. I_C

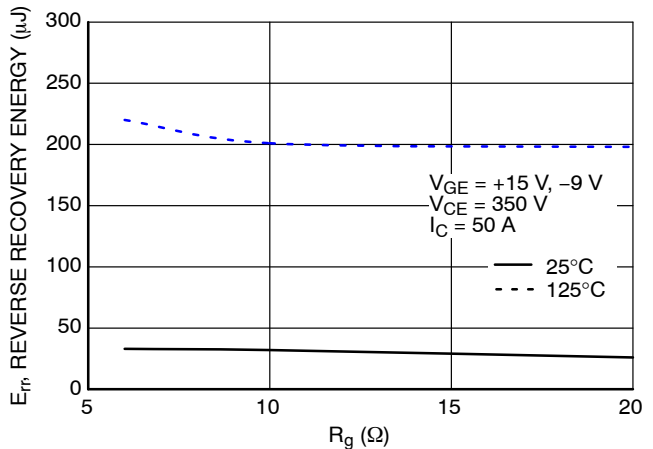


Figure 24. Typical Reverse Recovery Energy Loss vs. R_g

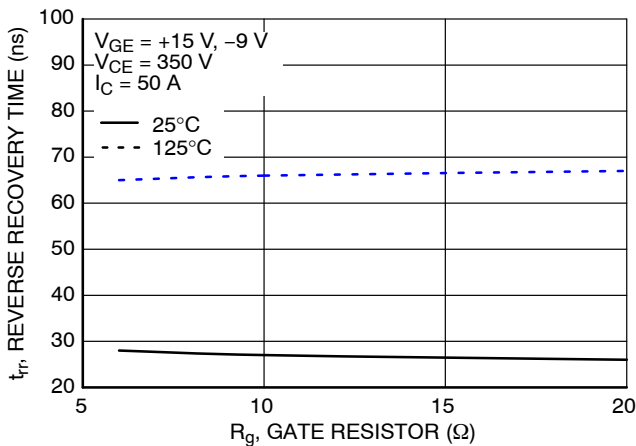


Figure 25. Typical Reverse Recovery Time vs. R_g

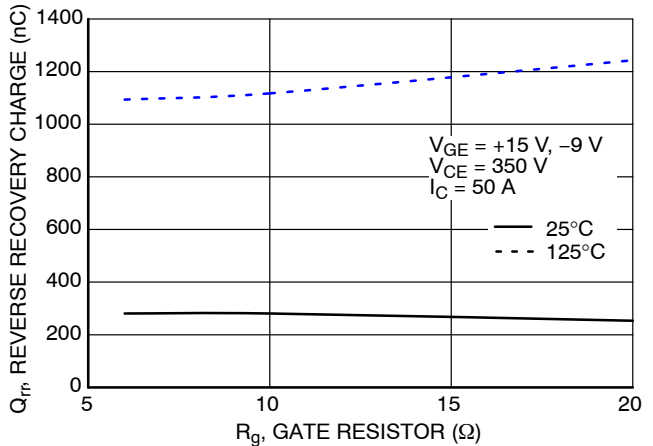


Figure 26. Typical Reverse Recovery Charge vs. R_g

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

TYPICAL CHARACTERISTICS – DIODE (CONTINUED)

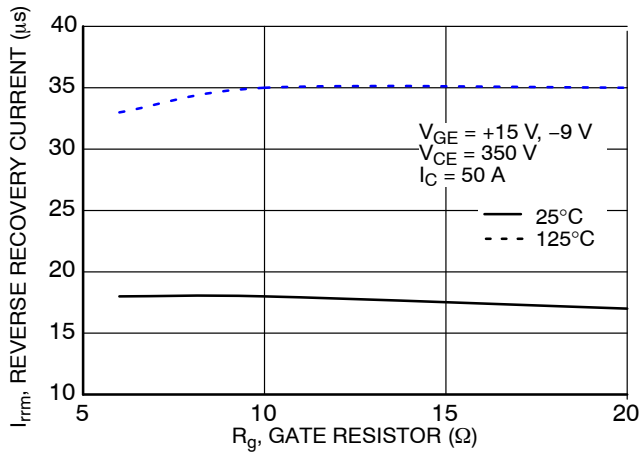


Figure 27. Typical Reverse Recovery Peak Current vs. Rg

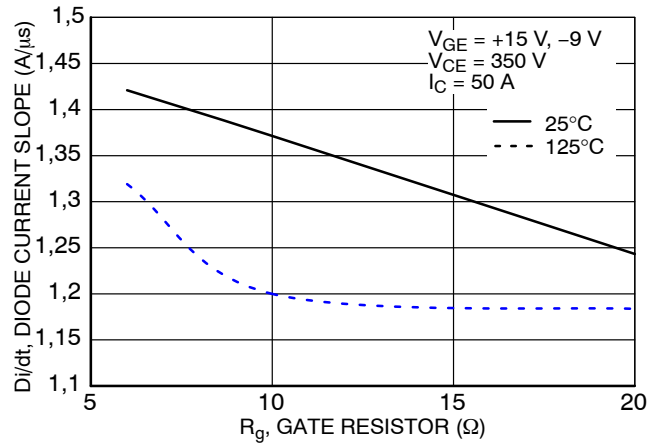


Figure 28. Typical di/dt vs. Rg

TYPICAL CHARACTERISTICS

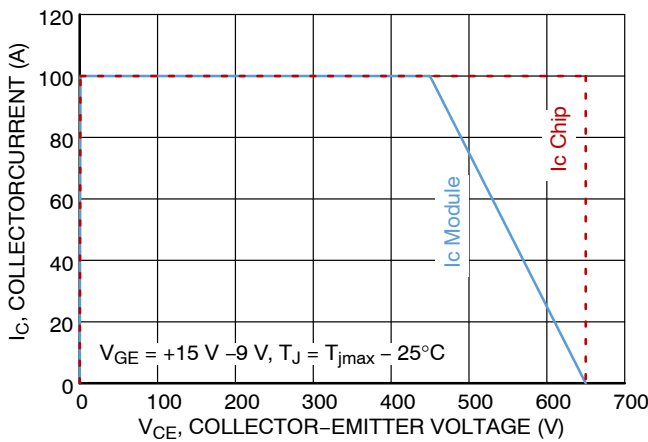


Figure 29. RBSOA Reverse Safe Operating Area

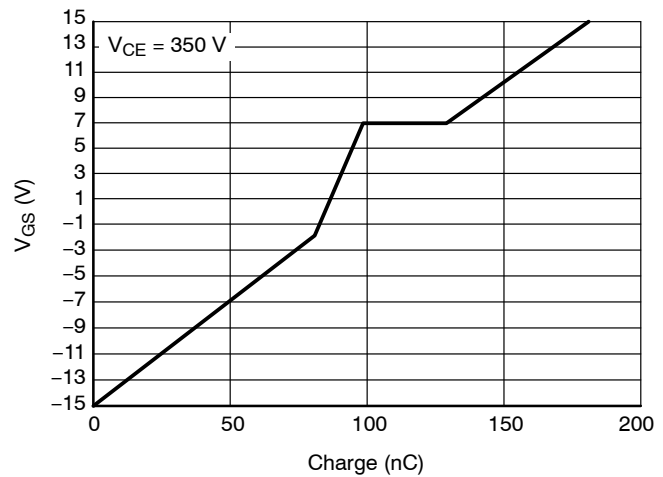


Figure 30. IGBT Gate Charge

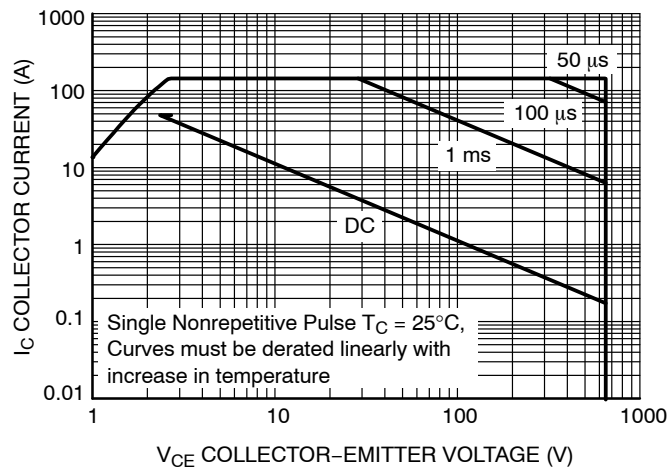


Figure 31. IGBT Safe Operating Area

NXH50M65L4Q1SG, NXH50M65L4Q1PTG

TYPICAL THERMAL CHARACTERISTICS

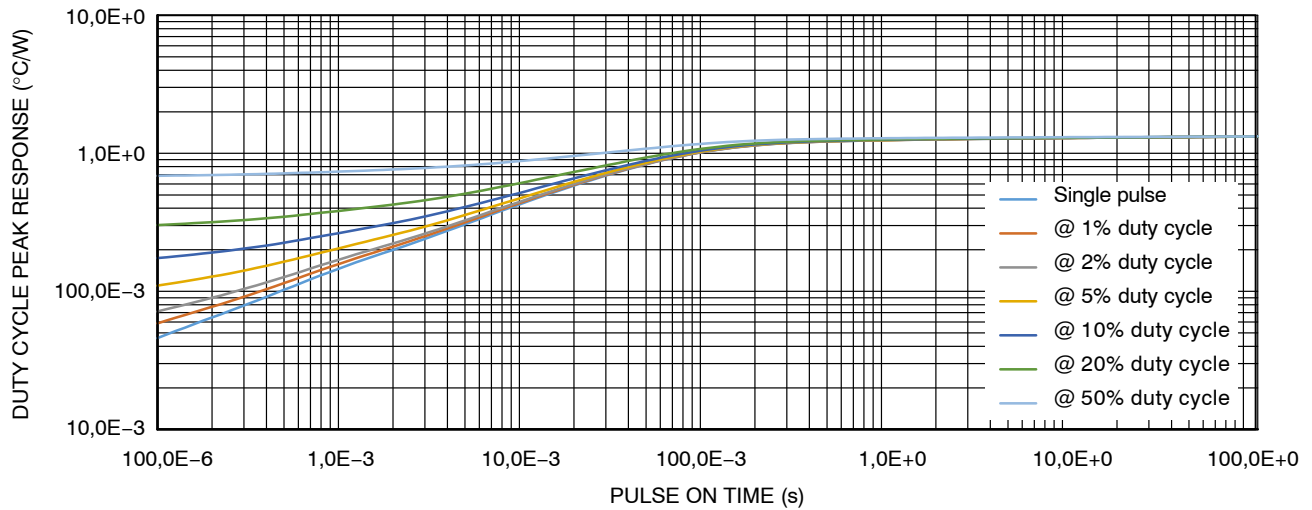


Figure 32. Transient Thermal Impedance – IGBT

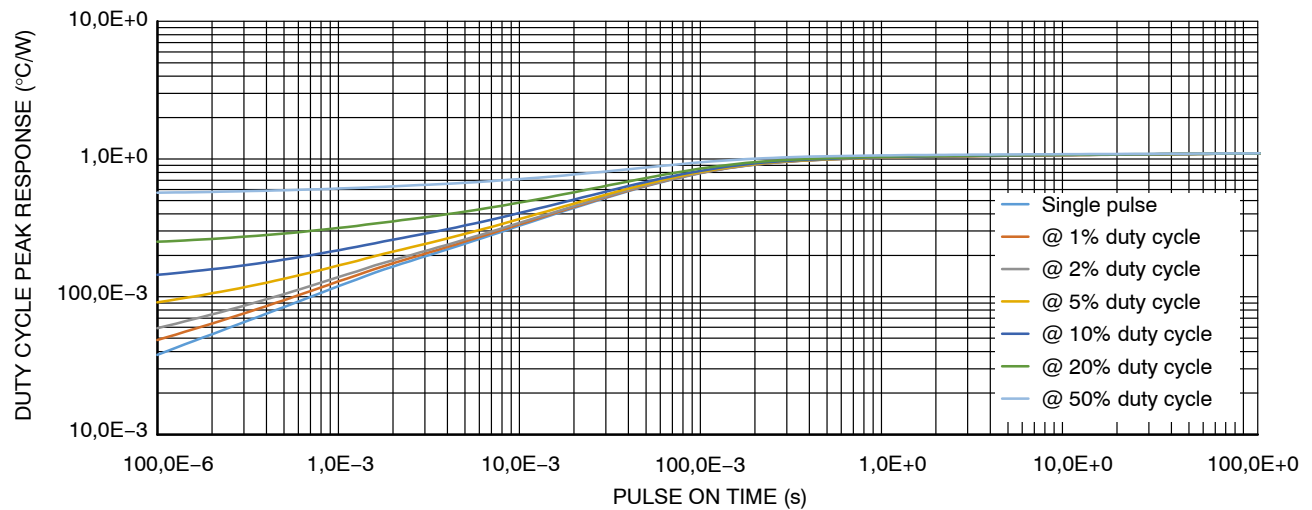


Figure 33. Transient Thermal Impedance – Diode

ORDERING INFORMATION

Device	Package Type	Status	Shipping
NXH50M65L4Q1SG (Solder Pin)	PIM27, 71x37.4 Q1PACK	In Development	21 Units / BTRAY
NXH50M65L4Q1PTG (Pressfit Pin)	PIM27, 71x37.4 Q1PACK	In Development	21 Units / BTRAY

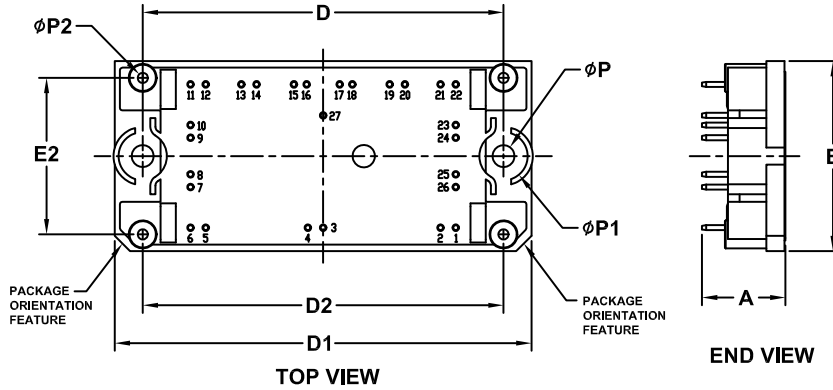
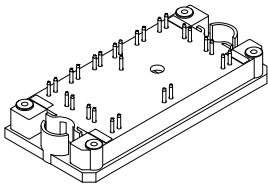
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

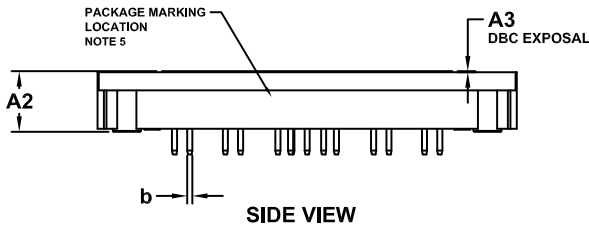


PIM27, 71x37.4 (SOLDER PIN)
CASE 180CA
ISSUE B

DATE 14 DEC 2022



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	15.90	16.40	16.90
A2	11.70	11.90	12.10
A3	0.00	0.20	0.60
b	0.95	1.00	1.05
b1	0.75	0.80	0.85
D	70.80	71.00	71.20
D1	81.70	82.00	82.30
D2	70.80	71.00	71.20
E	37.10	37.40	37.70
E2	30.60	30.80	31.00
P	4.10	4.30	4.50
P1	9.30	9.50	9.70
P2	1.80	2.00	2.20



NOTE 4

PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	52.20	0.00	15	20.35	28.20
2	49.20	0.00	16	22.85	28.20
3	26.10	0.00	17	29.35	28.20
4	23.10	0.00	18	31.85	28.20
5	3.00	0.00	19	39.20	28.20
6	0.00	0.00	20	42.20	28.20
7	0.00	8.00	21	49.20	28.20
8	0.00	10.50	22	52.20	28.20
9	0.00	17.70	23	52.20	20.20
10	0.00	20.20	24	52.20	17.70
11	0.00	28.20	25	52.20	10.50
12	3.00	28.20	26	52.20	8.00
13	10.00	28.20	27	26.10	22.10
14	13.00	28.20			

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009
2. CONTROLLING DIMENSION : MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A1
4. PIN POSITION TOLERANCE IS $\pm 0.4\text{mm}$
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES

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DESCRIPTION:	PIM27, 71X37.4 (SOLDER PIN)	PAGE 1 OF 2

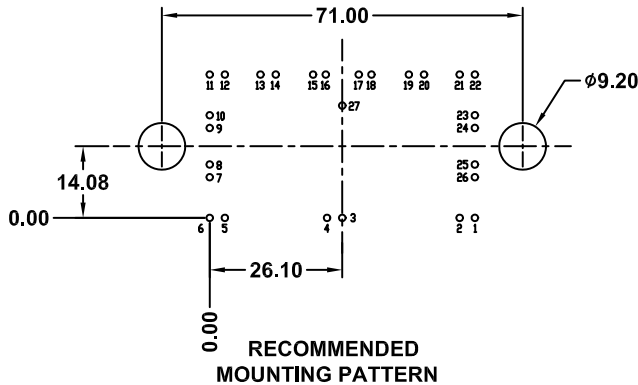
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



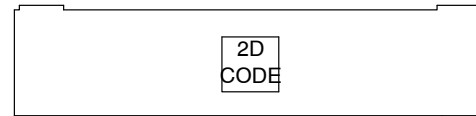
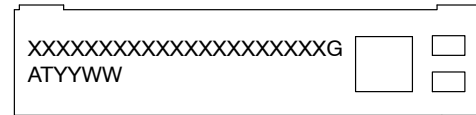
PIM27, 71x37.4 (SOLDER PIN)
CASE 180CA
ISSUE B

DATE 14 DEC 2022



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
 G = Pb-Free Device
 AT = Assembly & Test Site Code
 YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	PIM27, 71X37.4 (SOLDER PIN)	PAGE 2 OF 2

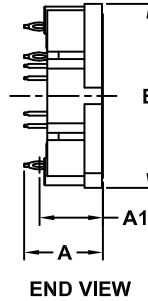
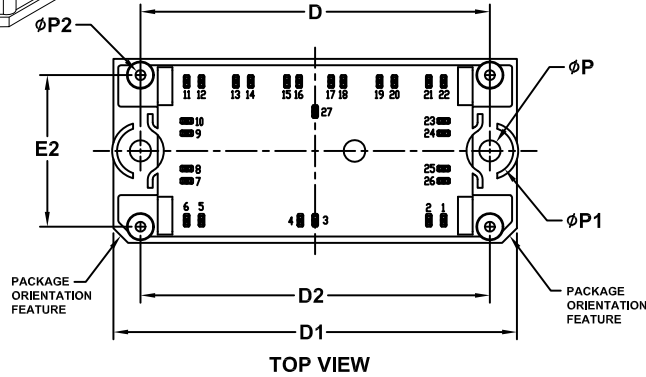
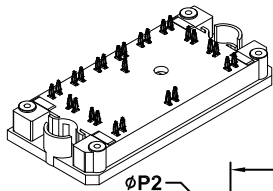
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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

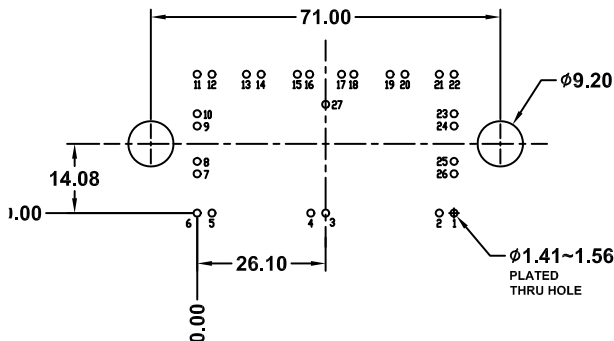
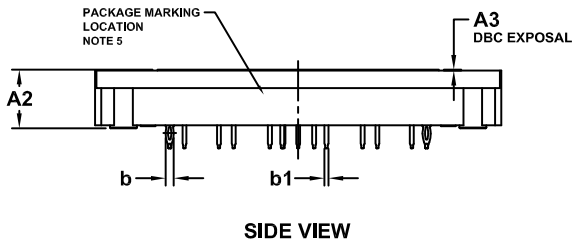


PIM27, 71x37.4 (PRESSFIT PIN) CASE 180CP ISSUE A

DATE 20 DEC 2022



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	15.50	16.00	16.50
A1	12.38	12.88	13.38
A2	11.70	11.90	12.10
A3	0.00	0.20	0.60
b	1.61	1.66	1.71
b1	0.75	0.80	0.85
D	70.80	71.00	71.20
D1	81.70	82.00	82.30
D2	70.80	71.00	71.20
E	37.10	37.40	37.70
E2	30.60	30.80	31.00
P	4.10	4.30	4.50
P1	9.30	9.50	9.70
P2	1.80	2.00	2.20



NOTE 4

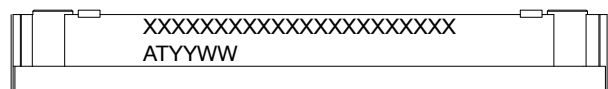
PIN	PIN POSITION		PIN	PIN POSITION	
	X	Y		X	Y
1	52.20	0.00	15	20.35	28.20
2	49.20	0.00	16	22.85	28.20
3	26.10	0.00	17	29.35	28.20
4	23.10	0.00	18	31.85	28.20
5	3.00	0.00	19	39.20	28.20
6	0.00	0.00	20	42.20	28.20
7	0.00	8.00	21	49.20	28.20
8	0.00	10.50	22	52.20	28.20
9	0.00	17.70	23	52.20	20.20
10	0.00	20.20	24	52.20	17.70
11	0.00	28.20	25	52.20	10.50
12	3.00	28.20	26	52.20	8.00
13	10.00	28.20	27	26.10	22.10
14	13.00	28.20			

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009
2. CONTROLLING DIMENSION : MILLIMETERS
3. DIMENSIONS b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED AT DIMENSION A1
4. PIN POSITION TOLERANCE IS $\pm 0.4\text{mm}$
5. PACKAGE MARKING IS LOCATED AS SHOWN ON THE SIDE OPPOSITE THE PACKAGE ORIENTATION FEATURES

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

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