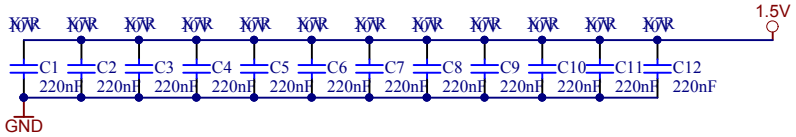
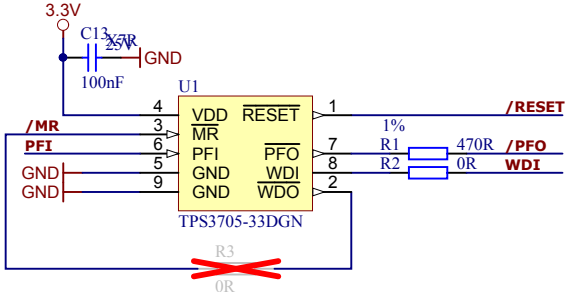
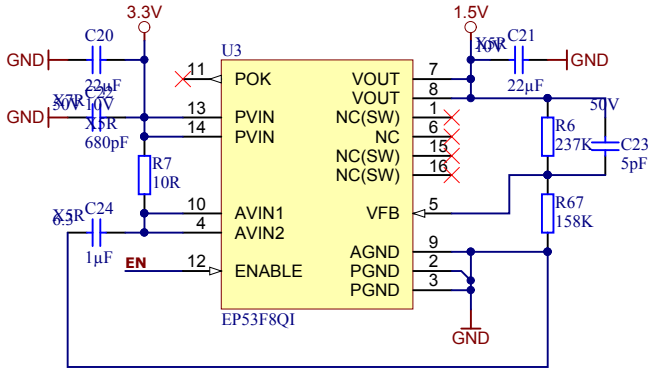
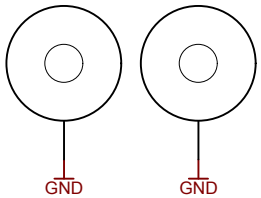
01.SchDoc
02.SchDoc
03.SchDoc
04.SchDoc
05.SchDoc
06.SchDoc
07.SchDoc
08.SchDoc
09.SchDoc
10.SchDoc



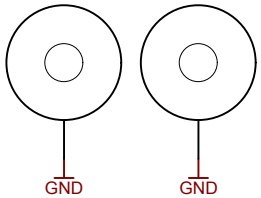


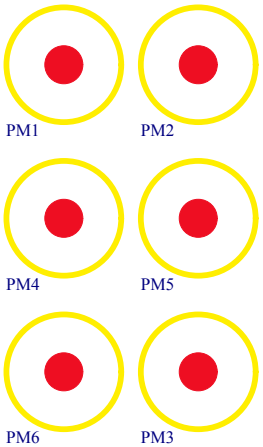


Mount.Hole 3.2mm Mount.Hole 3.2mm

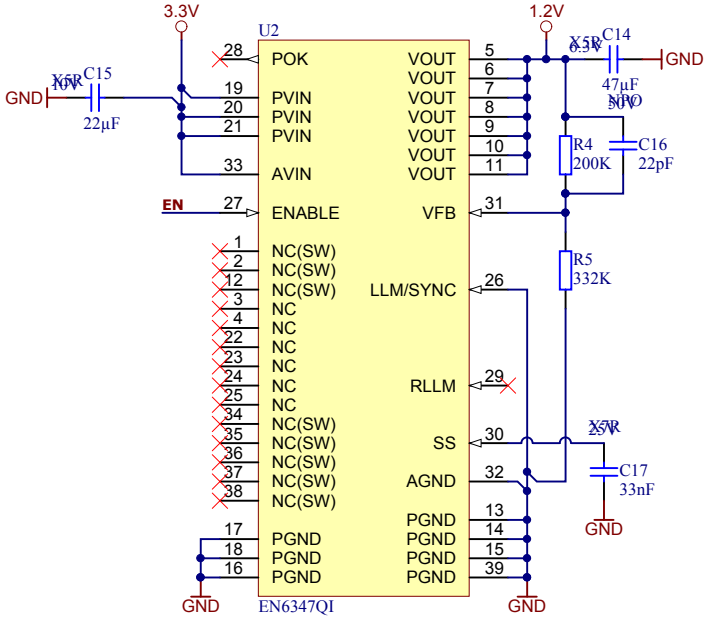


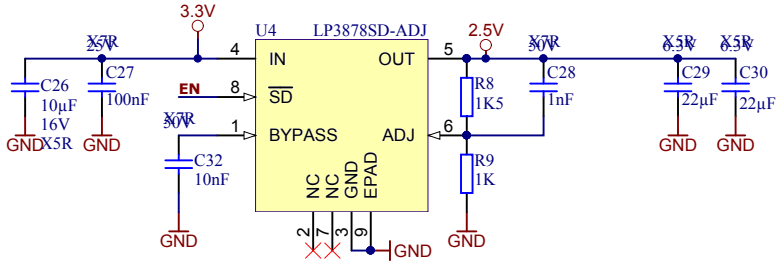
Mount.Hole 3.2mm Mount.Hole 3.2mm

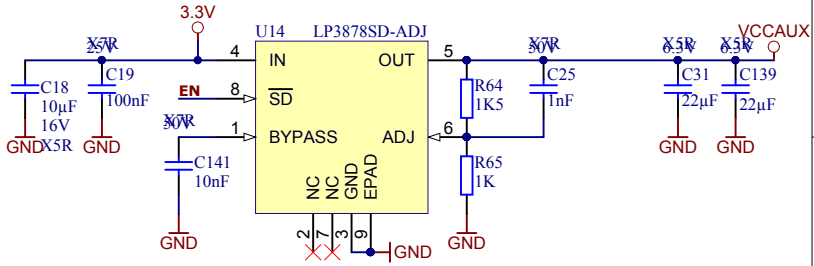




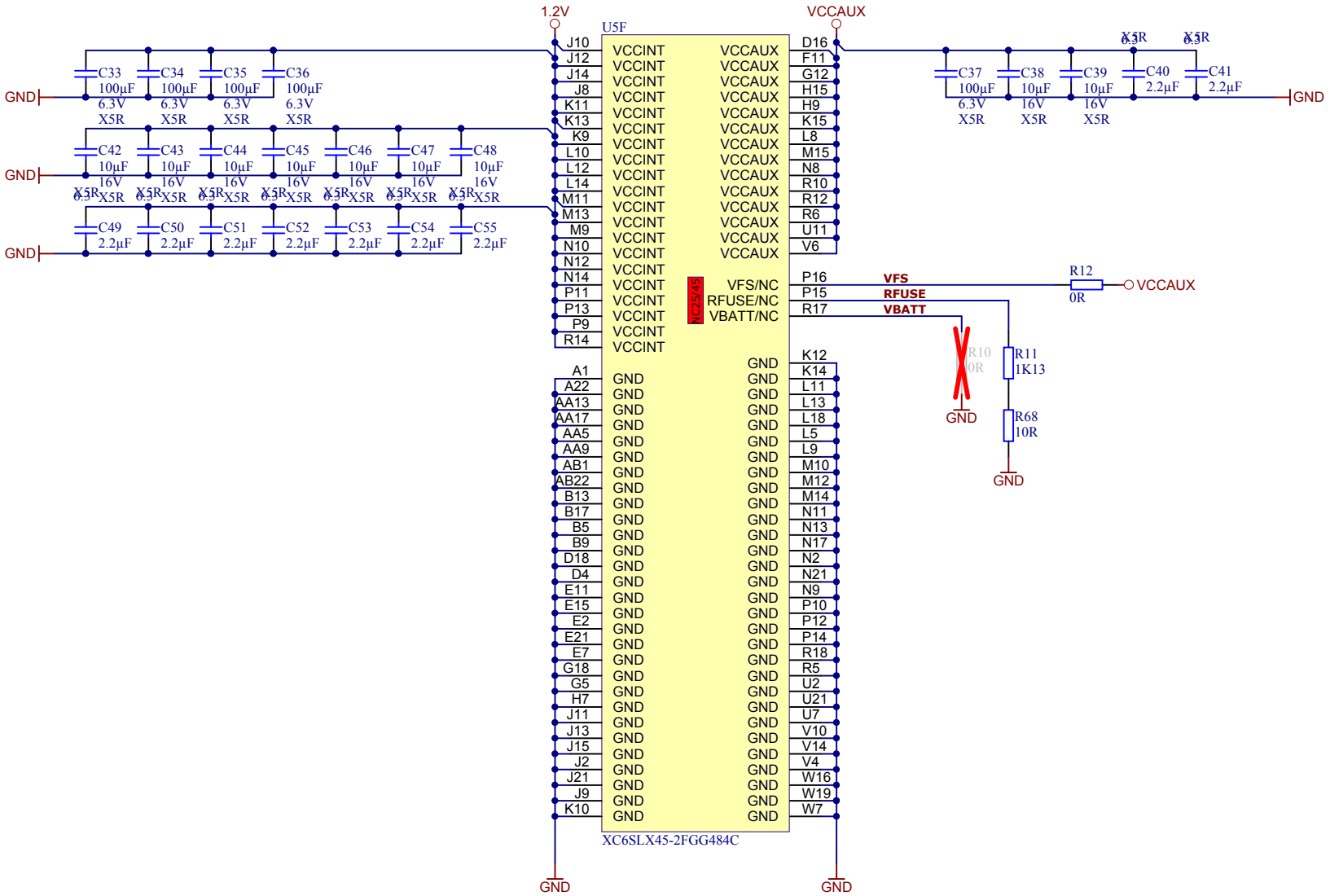
Top of Board







trenz electronic	Title:		
	A4	Nummer: GigaBee FPGA Module TE0600-02	Rev. 02
	Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 1 von 11
	Filename:	00.SchDoc	



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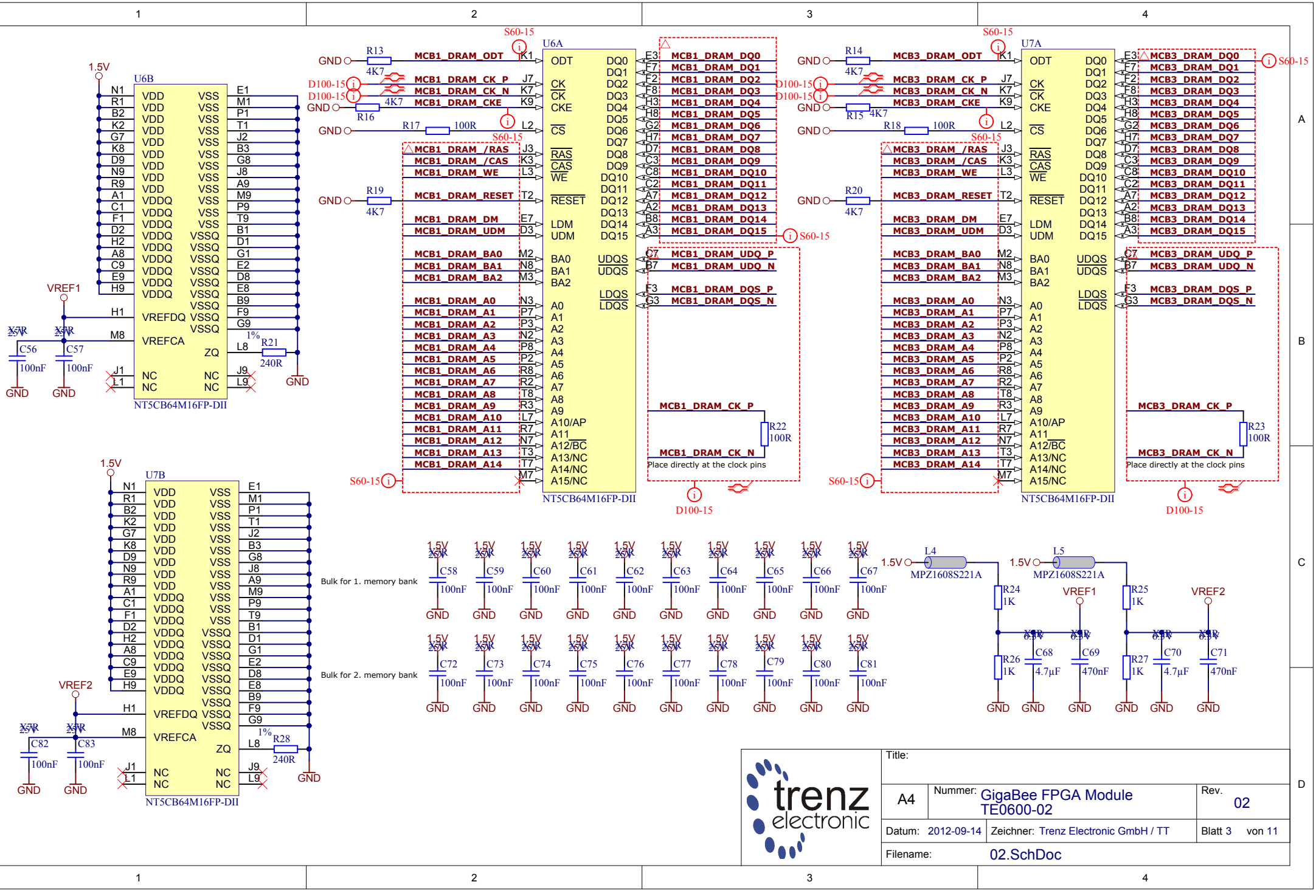
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 2 von 11
Filename:	01.SchDoc	


U6B
U6A
U7A
U7B
NT5CB64M16FP-DII
1.5V
VREF1
VREF2
GND
S60-15
D100-15
MCB1_DRAM_ODT
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
MCB1_DRAM_CKE
MCB1_DRAM_/RAS
MCB1_DRAM_/CAS
MCB1_DRAM_WE
MCB1_DRAM_RESET
MCB1_DRAM_DM
MCB1_DRAM_UDM
MCB1_DRAM_BA0
MCB1_DRAM_BA1
MCB1_DRAM_BA2
MCB1_DRAM_A0
MCB1_DRAM_A1
MCB1_DRAM_A2
MCB1_DRAM_A3
MCB1_DRAM_A4
MCB1_DRAM_A5
MCB1_DRAM_A6
MCB1_DRAM_A7
MCB1_DRAM_A8
MCB1_DRAM_A9
MCB1_DRAM_A10
MCB1_DRAM_A11
MCB1_DRAM_A12
MCB1_DRAM_A13
MCB1_DRAM_A14
MCB1_DRAM_DQ0
MCB1_DRAM_DQ1
MCB1_DRAM_DQ2
MCB1_DRAM_DQ3
MCB1_DRAM_DQ4
MCB1_DRAM_DQ5
MCB1_DRAM_DQ6
MCB1_DRAM_DQ7
MCB1_DRAM_DQ8
MCB1_DRAM_DQ9
MCB1_DRAM_DQ10
MCB1_DRAM_DQ11
MCB1_DRAM_DQ12
MCB1_DRAM_DQ13
MCB1_DRAM_DQ14
MCB1_DRAM_DQ15
MCB1_DRAM_UDQ_P
MCB1_DRAM_UDQ_N
MCB1_DRAM_DQS_P
MCB1_DRAM_DQS_N
MCB1_DRAM_CK_P
MCB1_DRAM_CK_N
Place directly at the clock pins
MCB3_DRAM_ODT
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
MCB3_DRAM_CKE
MCB3_DRAM_/RAS
MCB3_DRAM_/CAS
MCB3_DRAM_WE
MCB3_DRAM_RESET
MCB3_DRAM_DM
MCB3_DRAM_UDM
MCB3_DRAM_BA0
MCB3_DRAM_BA1
MCB3_DRAM_BA2
MCB3_DRAM_A0
MCB3_DRAM_A1
MCB3_DRAM_A2
MCB3_DRAM_A3
MCB3_DRAM_A4
MCB3_DRAM_A5
MCB3_DRAM_A6
MCB3_DRAM_A7
MCB3_DRAM_A8
MCB3_DRAM_A9
MCB3_DRAM_A10
MCB3_DRAM_A11
MCB3_DRAM_A12
MCB3_DRAM_A13
MCB3_DRAM_A14
MCB3_DRAM_DQ0
MCB3_DRAM_DQ1
MCB3_DRAM_DQ2
MCB3_DRAM_DQ3
MCB3_DRAM_DQ4
MCB3_DRAM_DQ5
MCB3_DRAM_DQ6
MCB3_DRAM_DQ7
MCB3_DRAM_DQ8
MCB3_DRAM_DQ9
MCB3_DRAM_DQ10
MCB3_DRAM_DQ11
MCB3_DRAM_DQ12
MCB3_DRAM_DQ13
MCB3_DRAM_DQ14
MCB3_DRAM_DQ15
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
Place directly at the clock pins
Bulk for 1. memory bank
Bulk for 2. memory bank
MPZ1608S221A
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 3 von 11
Filename: 02.SchDoc
trenz electronic

Trace widths should be 3 to 5 mils.
• Trace spacing should be three times the trace width.
• Signals must not be routed over splits or voids.
• Routing of differential pairs adjacent to noisy signal lines or high-speed switching
devices such as clock chips should be avoided.
• The spacing between differential clocks/strobes and other signals on the same PCB
layer should be 20 mil. The 20 mil spacing should be maintained when using
serpentine routing for length matching.
Differential clocks/strobes are to be routed as 100O differential signals. The clock
pairs must be routed on the same PCB layer with no layer changes or hops after the
initial pad to via breakout.
The Data (DQ), Data Mask (DM), and Data Strobe (DQS) signals should receive the highest
priority (that is, routed first), because they are the highest speed DDR signals.
• DQ, DM, and DQS signals should be routed in a data group (per byte). Each group
should have similar loading and routing to maintain timing and signal integrity.
• The provided spacing should be 20 mil between a data group and any other signals.
• DQS signals should be isolated from other signals by 20 mil to avoid crosstalk.
• There should be a maximum of ±25 ps electrical delay (±150 mil) between any
DQ/DM and its associated DQS strobe.
• A data group should be referenced to a GROUND plane.
• DQ bit swapping at the memory interface is permitted to facilitate layout. Swapping
should only be done within a data group.
• DQS to DQS_N trace lengths should be matched (±10 mil).
• Memory terminations (if external terminations are used) should be placed after the
associated memory component in a fly-by fashion.
• For 16-bit DDR devices, the LDQS/LDQS_N and UDQS/UDQS_N trace lengths
should be matched within ±25 ps of the electrical delay (±150 mil).
When the data groups have been routed, the next highest priority is the differential clock
(CK / CK_N). The clock should be routed first because all address and control trace length
matching must be referenced to the differential clock PCB trace length, which might need
to be adjusted as the layout task proceeds.
• CK to CK_N trace lengths must be matched (±10 mil).
• CK and DQS trace lengths must be matched (±250 mil) to maximize setup and hold
margins.
• There must be a maximum ±50 ps electrical delay (±300 mil) between any
address/control signals and the associated CK and CK_N differential clock FPGA output.
• Address and control signals can be referenced to a POWER plane if a GROUND plane
is not next to this group of signals in the PCB stack-up.
To avoid crosstalk, address and command signals should be kept on a different routing layer from DQ, DQS, and DM.
• Differential clock terminations (if external terminations are used) must be located as
close as possible to the load, after the clock pads of the PCB. PCB trace lengths used in
trace length matching must exclude the CLINE length of the PCB trace from memory
ball to terminating resistor.

Classnames:
S60-15 uses 1.5V or GND plane as reference
D100-15 uses 1.5V or GND plane as reference

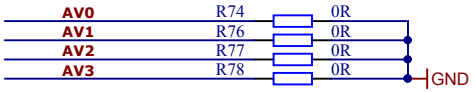
S60-25 uses 2.5V or GND plane as reference
D100-25 uses 2.5V or GND plane as reference

S60-IO uses VCCIO0 or GND plane as reference
D100-IO uses VCCIO0 or GND plane as reference

S60-33 uses 3.3V or GND plane as reference
D100-33 uses 3.3V or GND plane as reference

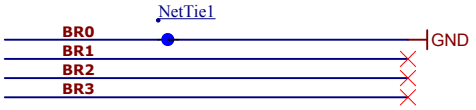
AV0 = 0 -> commercial AV0 = 1 -> Industrial
AV1 = 0 -> speedgrade 2 AV1 = 1 -> speedgrade 3
AV2 = 0 -> 2 x 128 MByte AV2 = 1 -> 2 x 512 MByte
AV3 = reserved

Assembly Variants



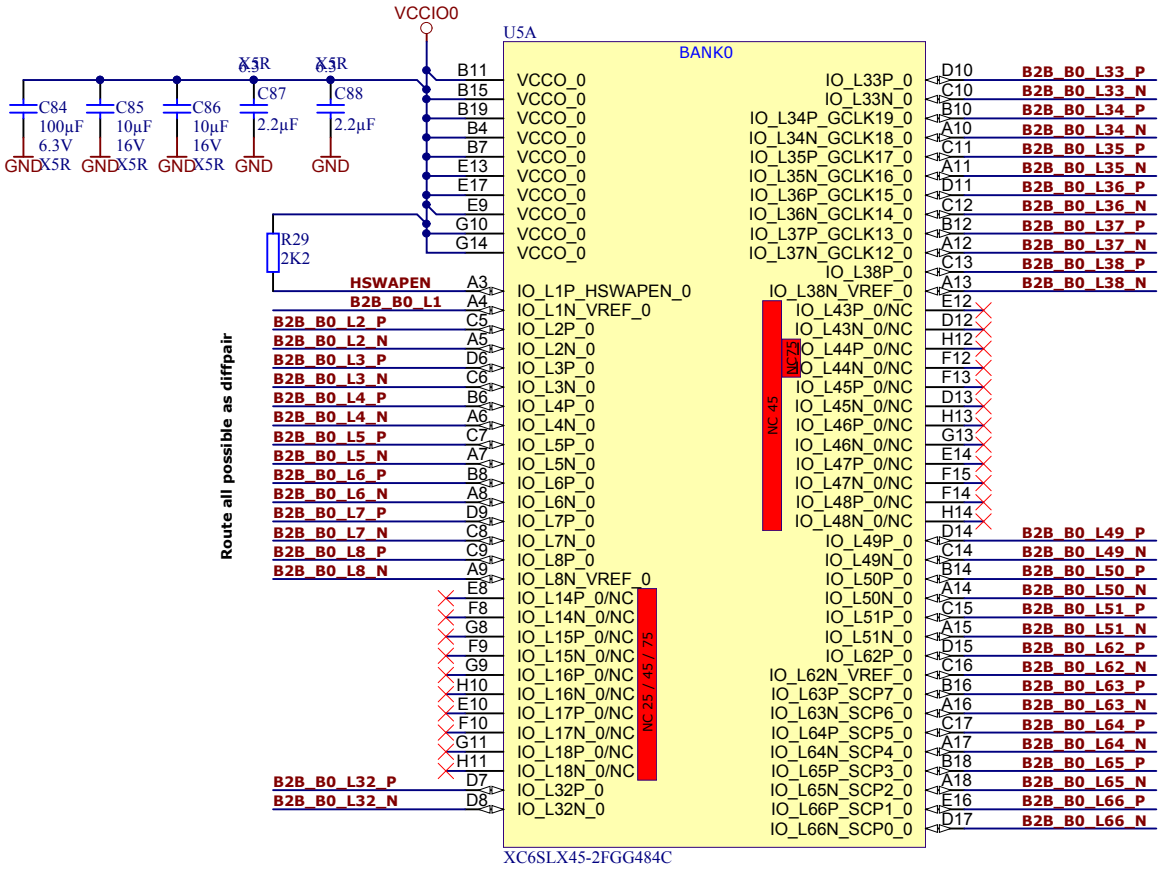
BR3	BR2	BR1	BR0	
1	1	1	1	-01 Initial revision
1	1	1	0	-02

Board Revisions



Enable pullups in FPGA

Title:			
A4	Nummer: GigaBee FPGA Module TE0600-02		Rev. 02
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT		Blatt 4 von 11
Filename: 03.SchDoc			



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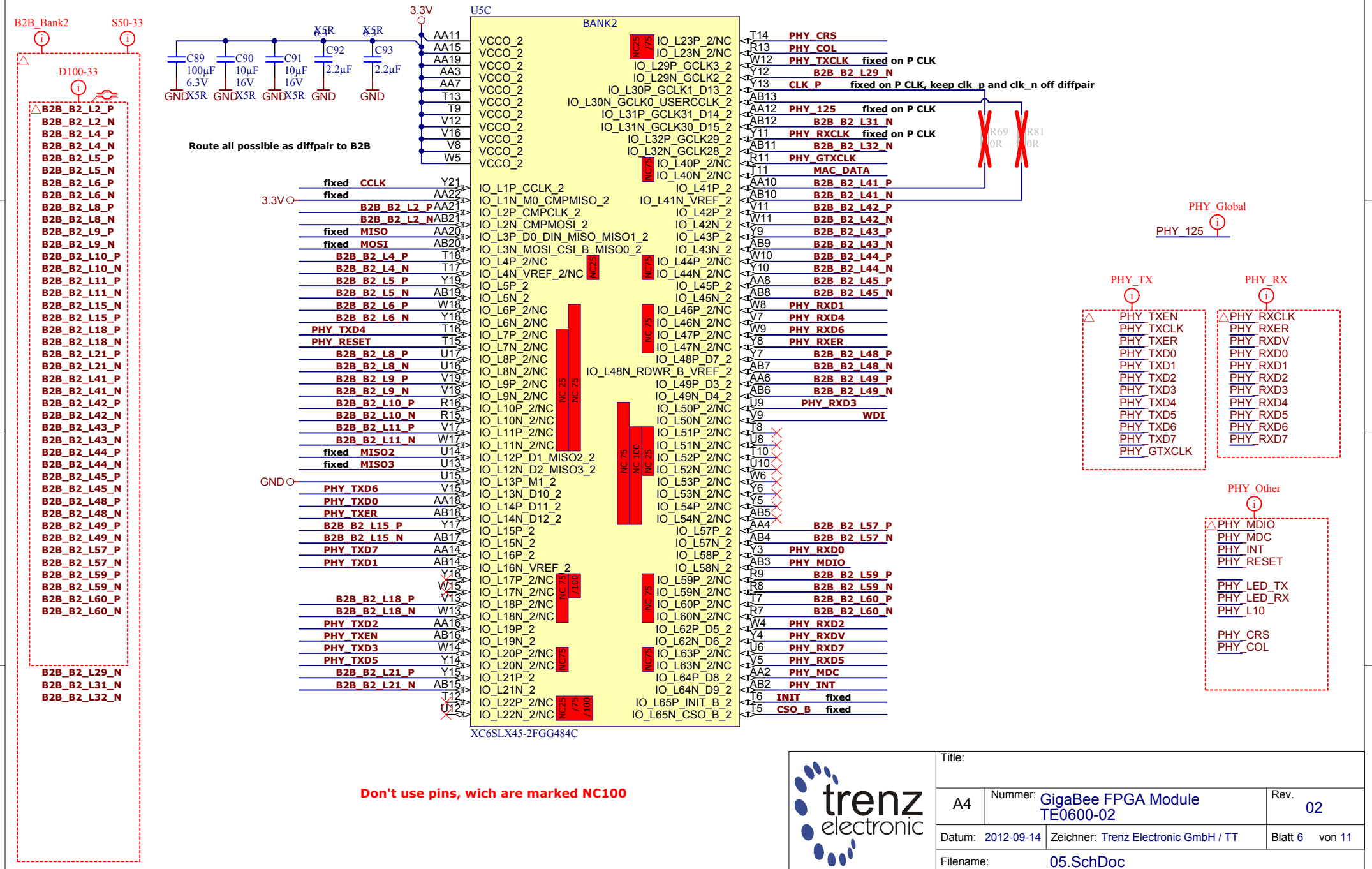
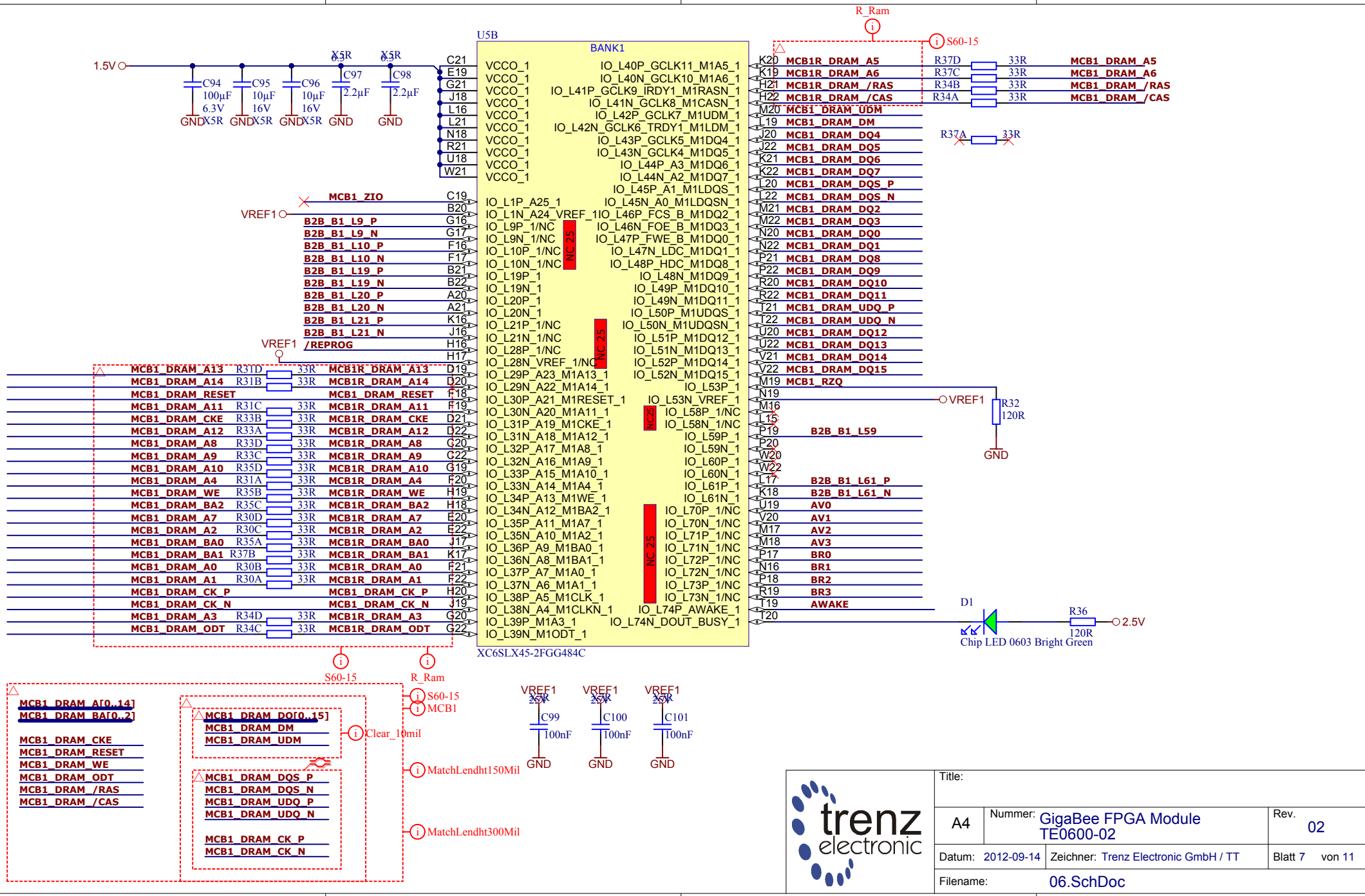
Title:			
A4	Nummer: GigaBee FPGA Module TE0600-02		Rev. 02
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT		Blatt 5 von 11
Filename: 04.SchDoc			


B2B_Bank2
S50-33
D100-33
B2B_B2_L2_P
B2B_B2_L2_N
B2B_B2_L4_P
B2B_B2_L4_N
B2B_B2_L5_P
B2B_B2_L5_N
B2B_B2_L6_P
B2B_B2_L6_N
B2B_B2_L8_P
B2B_B2_L8_N
B2B_B2_L9_P
B2B_B2_L9_N
B2B_B2_L10_P
B2B_B2_L10_N
B2B_B2_L11_P
B2B_B2_L11_N
B2B_B2_L15_N
B2B_B2_L15_P
B2B_B2_L18_P
B2B_B2_L18_N
B2B_B2_L21_P
B2B_B2_L21_N
B2B_B2_L41_P
B2B_B2_L41_N
B2B_B2_L42_P
B2B_B2_L42_N
B2B_B2_L43_P
B2B_B2_L43_N
B2B_B2_L44_P
B2B_B2_L44_N
B2B_B2_L45_P
B2B_B2_L45_N
B2B_B2_L48_P
B2B_B2_L48_N
B2B_B2_L49_P
B2B_B2_L49_N
B2B_B2_L57_P
B2B_B2_L57_N
B2B_B2_L59_P
B2B_B2_L59_N
B2B_B2_L60_P
B2B_B2_L60_N
B2B_B2_L29_N
B2B_B2_L31_N
B2B_B2_L32_N
3.3V
C89 100µF 6.3V X5R
C90 10µF 16V X5R
C91 10µF 16V X5R
C92 2.2µF X5R
C93 2.2µF
GND
Route all possible as diffpair to B2B
U5C
BANK2
XC6SLX45-2FGG484C
fixed CCLK
fixed
B2B_B2_L2_P
B2B_B2_L2_N
fixed MISO
fixed MOSI
B2B_B2_L4_P
B2B_B2_L4_N
B2B_B2_L5_P
B2B_B2_L5_N
B2B_B2_L6_P
B2B_B2_L6_N
PHY_TXD4
PHY_RESET
B2B_B2_L8_P
B2B_B2_L8_N
B2B_B2_L9_P
B2B_B2_L9_N
B2B_B2_L10_P
B2B_B2_L10_N
B2B_B2_L11_P
B2B_B2_L11_N
fixed MISO2
fixed MISO3
PHY_TXD6
PHY_TXD0
PHY_TXER
B2B_B2_L15_P
B2B_B2_L15_N
PHY_TXD7
PHY_TXD1
B2B_B2_L18_P
B2B_B2_L18_N
PHY_TXD2
PHY_TXEN
PHY_TXD3
PHY_TXD5
B2B_B2_L21_P
B2B_B2_L21_N
T14 PHY_CRS
R13 PHY_COL
W12 PHY_TXCLK fixed on P CLK
Y12 B2B_B2_L29_N
Y13 CLK_P fixed on P CLK, keep clk_p and clk_n off diffpair
AA12 PHY_125 fixed on P CLK
AB12 B2B_B2_L31_N
Y11 PHY_RXCLK fixed on P CLK
AB11 B2B_B2_L32_N
R11 PHY_GTXCLK
T11 MAC_DATA
AA10 B2B_B2_L41_P
AB10 B2B_B2_L41_N
V11 B2B_B2_L42_P
W11 B2B_B2_L42_N
Y9 B2B_B2_L43_P
AB9 B2B_B2_L43_N
W10 B2B_B2_L44_P
Y10 B2B_B2_L44_N
AA8 B2B_B2_L45_P
AB8 B2B_B2_L45_N
W8 PHY_RXD1
V7 PHY_RXD4
W9 PHY_RXD6
Y8 PHY_RXER
Y7 B2B_B2_L48_P
AB7 B2B_B2_L48_N
AA6 B2B_B2_L49_P
AB6 B2B_B2_L49_N
U9 PHY_RXD3
V9 WDI
AA4 B2B_B2_L57_P
AB4 B2B_B2_L57_N
Y3 PHY_RXD0
AB3 PHY_MDIO
R9 B2B_B2_L59_P
R8 B2B_B2_L59_N
T7 B2B_B2_L60_P
R7 B2B_B2_L60_N
W4 PHY_RXD2
Y4 PHY_RXDV
U6 PHY_RXD7
Y5 PHY_RXD5
AA2 PHY_MDC
AB2 PHY_INT
T6 INIT fixed
T5 CSO_B fixed
R69 0R
R81 0R
PHY_Global
PHY_125
PHY_TX
PHY_TXEN
PHY_TXCLK
PHY_TXER
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_GTXCLK
PHY_RX
PHY_RXCLK
PHY_RXER
PHY_RXDV
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_Other
PHY_MDIO
PHY_MDC
PHY_INT
PHY_RESET
PHY_LED_TX
PHY_LED_RX
PHY_L10
PHY_CRS
PHY_COL
Don't use pins, wich are marked NC100
trenz electronic
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 6 von 11
Filename: 05.SchDoc



Title:			
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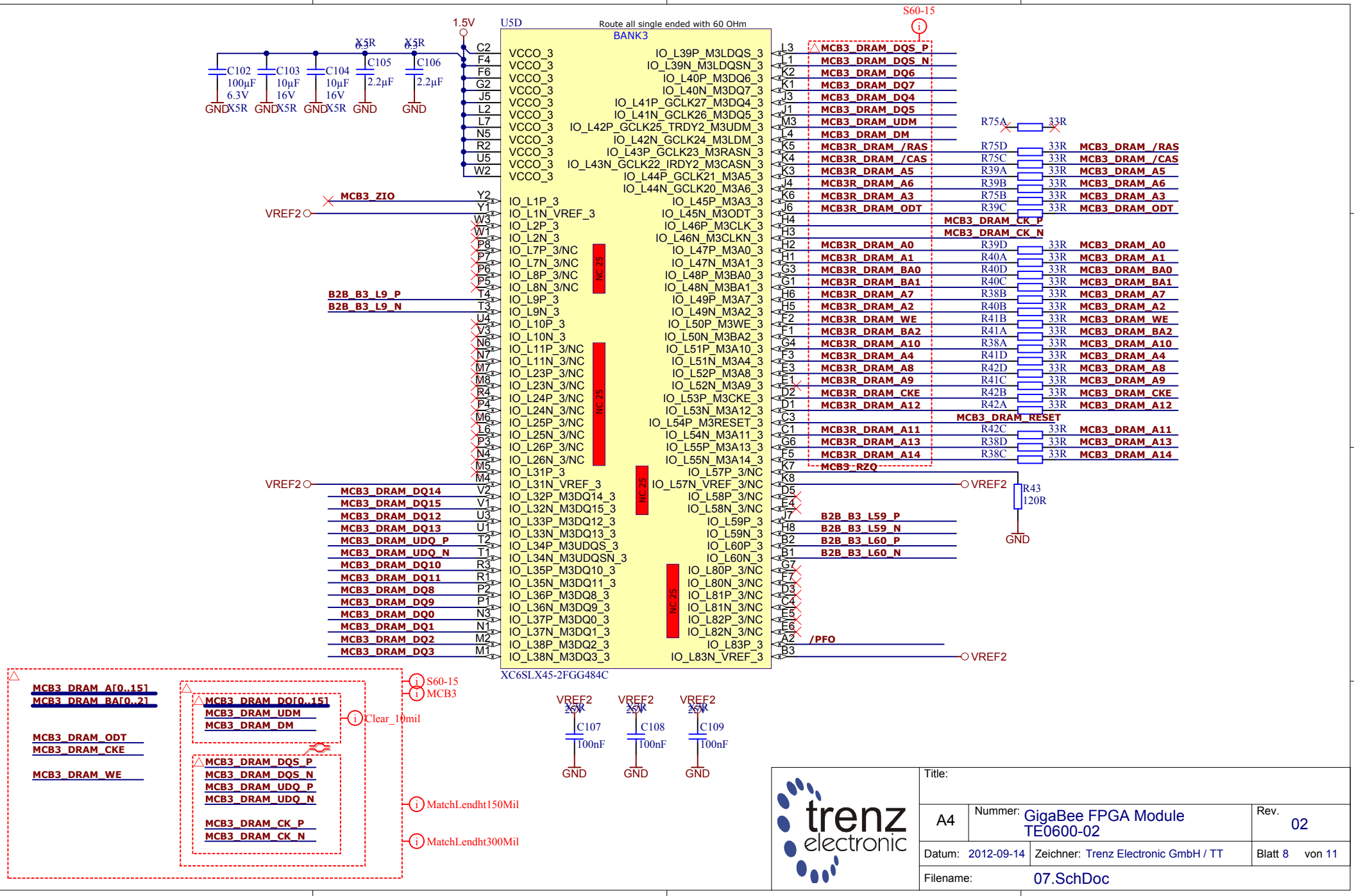
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT		Blatt 7 von 11
Filename: 06.SchDoc			


1.5V
U5D
Route all single ended with 60 OHm
BANK3
S60-15
C102 100µF 6.3V
C103 10µF 16V
C104 10µF 16V
C105 2.2µF
C106 2.2µF
X5R
GND
VCCO_3
IO_L39P_M3LDQS_3
IO_L39N_M3LDQSN_3
IO_L40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L41P_GCLK27_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L42P_GCLK25_TRDY2_M3UDM_3
IO_L42N_GCLK24_M3LDM_3
IO_L43P_GCLK23_M3RASN_3
IO_L43N_GCLK22_IRDY2_M3CASN_3
IO_L44P_GCLK21_M3A5_3
IO_L44N_GCLK20_M3A6_3
IO_L45P_M3A3_3
IO_L45N_M3ODT_3
IO_L46P_M3CLK_3
IO_L46N_M3CLKN_3
IO_L47P_M3A0_3
IO_L47N_M3A1_3
IO_L48P_M3BA0_3
IO_L48N_M3BA1_3
IO_L49P_M3A7_3
IO_L49N_M3A2_3
IO_L50P_M3WE_3
IO_L50N_M3BA2_3
IO_L51P_M3A10_3
IO_L51N_M3A4_3
IO_L52P_M3A8_3
IO_L52N_M3A9_3
IO_L53P_M3CKE_3
IO_L53N_M3A12_3
IO_L54P_M3RESET_3
IO_L54N_M3A11_3
IO_L55P_M3A13_3
IO_L55N_M3A14_3
IO_L57P_3/NC
IO_L57N_VREF_3/NC
IO_L58P_3/NC
IO_L58N_3/NC
IO_L59P_3
IO_L59N_3
IO_L60P_3
IO_L60N_3
IO_L80P_3/NC
IO_L80N_3/NC
IO_L81P_3/NC
IO_L81N_3/NC
IO_L82P_3/NC
IO_L82N_3/NC
IO_L83P_3
IO_L83N_VREF_3
NC 25
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_DQ6
MCB3_DRAM_DQ7
MCB3_DRAM_DQ4
MCB3_DRAM_DQ5
MCB3_DRAM_UDM
MCB3_DRAM_DM
MCB3R_DRAM_/RAS
MCB3R_DRAM_/CAS
MCB3R_DRAM_A5
MCB3R_DRAM_A6
MCB3R_DRAM_A3
MCB3R_DRAM_ODT
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
MCB3R_DRAM_A0
MCB3R_DRAM_A1
MCB3R_DRAM_BA0
MCB3R_DRAM_BA1
MCB3R_DRAM_A7
MCB3R_DRAM_A2
MCB3R_DRAM_WE
MCB3R_DRAM_BA2
MCB3R_DRAM_A10
MCB3R_DRAM_A4
MCB3R_DRAM_A8
MCB3R_DRAM_A9
MCB3R_DRAM_CKE
MCB3R_DRAM_A12
MCB3_DRAM_RESET
MCB3R_DRAM_A11
MCB3R_DRAM_A13
MCB3R_DRAM_A14
MCB3_RZQ
R75A 33R
R75D 33R
R75C 33R
R39A 33R
R39B 33R
R75B 33R
R39C 33R
R39D 33R
R40A 33R
R40D 33R
R40C 33R
R38B 33R
R40B 33R
R41B 33R
R41A 33R
R38A 33R
R41D 33R
R42D 33R
R41C 33R
R42B 33R
R42A 33R
R42C 33R
R38D 33R
R38C 33R
R43 120R
MCB3_ZIO
VREF2
B2B_B3_L9_P
B2B_B3_L9_N
MCB3_DRAM_DQ14
MCB3_DRAM_DQ15
MCB3_DRAM_DQ12
MCB3_DRAM_DQ13
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_DQ10
MCB3_DRAM_DQ11
MCB3_DRAM_DQ8
MCB3_DRAM_DQ9
MCB3_DRAM_DQ0
MCB3_DRAM_DQ1
MCB3_DRAM_DQ2
MCB3_DRAM_DQ3
B2B_B3_L59_P
B2B_B3_L59_N
B2B_B3_L60_P
B2B_B3_L60_N
/PFO
XC6SLX45-2FGG484C
C107 100nF
C108 100nF
C109 100nF
MCB3_DRAM_A[0..15]
MCB3_DRAM_BA[0..2]
MCB3_DRAM_ODT
MCB3_DRAM_CKE
MCB3_DRAM_WE
MCB3_DRAM_DQ[0..15]
MCB3_DRAM_UDM
MCB3_DRAM_DM
MCB3_DRAM_DQS_P
MCB3_DRAM_DQS_N
MCB3_DRAM_UDQ_P
MCB3_DRAM_UDQ_N
MCB3_DRAM_CK_P
MCB3_DRAM_CK_N
S60-15
MCB3
Clear_10mil
MatchLendht150Mil
MatchLendht300Mil
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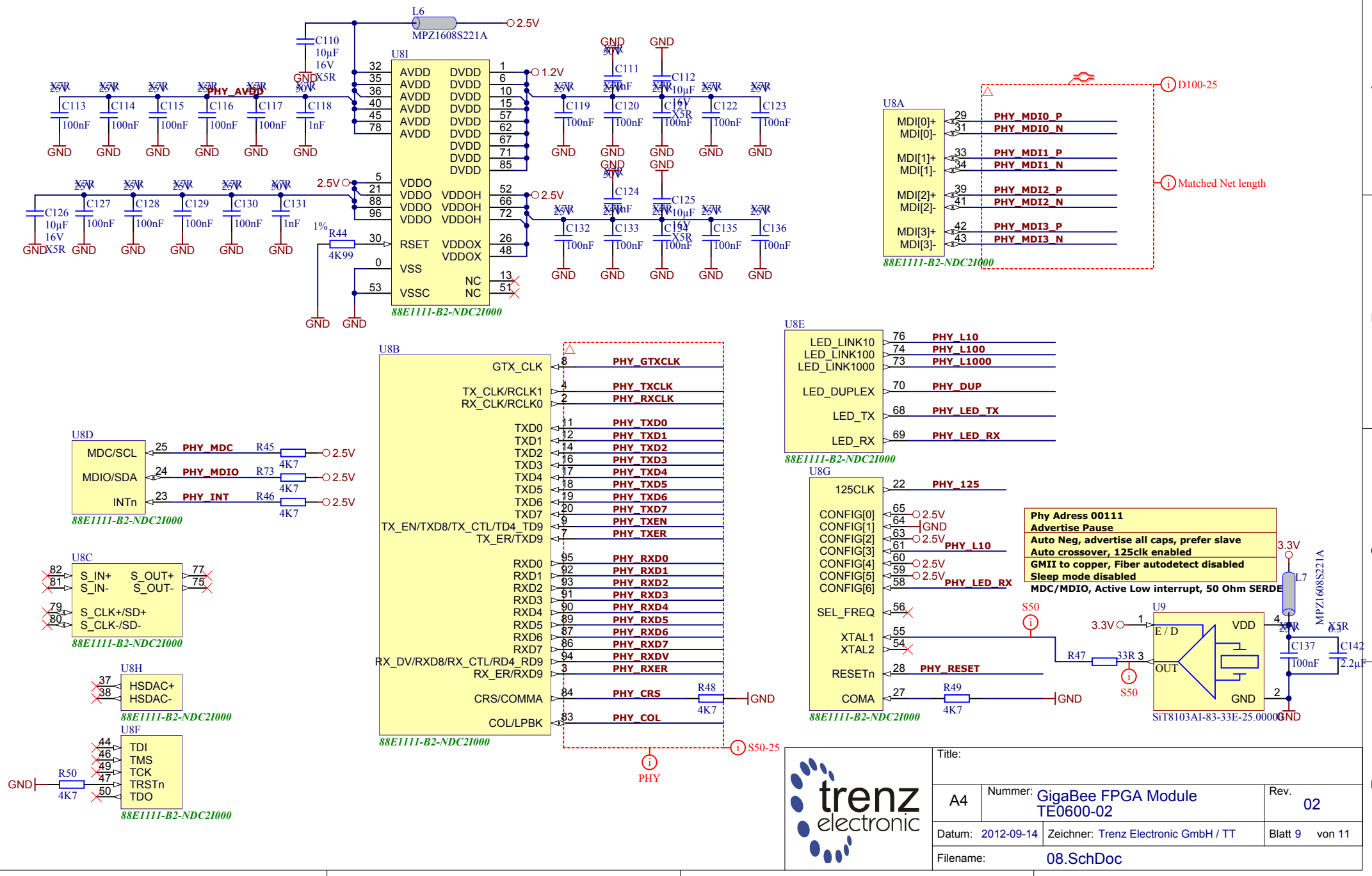
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 8 von 11
Filename: 07.SchDoc


L6
MPZ1608S221A
2.5V
U8I
AVDD
DVDD
VDDO
VDDOH
VDDOX
RSET
VSS
VSSC
NC
1.2V
PHY_AVDD
C110 10µF 16V X5R
C111 100nF
C112 10µF 16V X5R
C113 100nF
C114 100nF
C115 100nF
C116 100nF
C117 100nF
C118 1nF
C119 100nF
C120 100nF
C121 100nF
C122 100nF
C123 100nF
C124 100nF
C125 10µF 16V X5R
C126 10µF 16V X5R
C127 100nF
C128 100nF
C129 100nF
C130 100nF
C131 1nF
C132 100nF
C133 100nF
C134 100nF
C135 100nF
C136 100nF
R44 4K99 1%
GND
88E1111-B2-NDC2I000
U8A
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
PHY_MDI0_P
PHY_MDI0_N
PHY_MDI1_P
PHY_MDI1_N
PHY_MDI2_P
PHY_MDI2_N
PHY_MDI3_P
PHY_MDI3_N
D100-25
Matched Net length
U8B
GTX_CLK
TX_CLK/RCLK1
RX_CLK/RCLK0
TXD0
TXD1
TXD2
TXD3
TXD4
TXD5
TXD6
TXD7
TX_EN/TXD8/TX_CTL/TD4_TD9
TX_ER/TXD9
RXD0
RXD1
RXD2
RXD3
RXD4
RXD5
RXD6
RXD7
RX_DV/RXD8/RX_CTL/RD4_RD9
RX_ER/RXD9
CRS/COMMA
COL/LPBK
PHY_GTXCLK
PHY_TXCLK
PHY_RXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXD4
PHY_TXD5
PHY_TXD6
PHY_TXD7
PHY_TXEN
PHY_TXER
PHY_RXD0
PHY_RXD1
PHY_RXD2
PHY_RXD3
PHY_RXD4
PHY_RXD5
PHY_RXD6
PHY_RXD7
PHY_RXDV
PHY_RXER
PHY_CRS
PHY_COL
R48 4K7
S50-25
PHY
U8D
MDC/SCL
MDIO/SDA
INTn
PHY_MDC
PHY_MDIO
PHY_INT
R45 4K7
R73 4K7
R46 4K7
U8C
S_IN+
S_IN-
S_OUT+
S_OUT-
S_CLK+/SD+
S_CLK-/SD-
U8H
HSDAC+
HSDAC-
U8F
TDI
TMS
TCK
TRSTn
TDO
R50 4K7
U8E
LED_LINK10
LED_LINK100
LED_LINK1000
LED_DUPLEX
LED_TX
LED_RX
PHY_L10
PHY_L100
PHY_L1000
PHY_DUP
PHY_LED_TX
PHY_LED_RX
U8G
125CLK
CONFIG[0]
CONFIG[1]
CONFIG[2]
CONFIG[3]
CONFIG[4]
CONFIG[5]
CONFIG[6]
SEL_FREQ
XTAL1
XTAL2
RESETn
COMA
PHY_125
PHY_RESET
R49 4K7
S50
R47 33R
Phy Adress 00111
Advertise Pause
Auto Neg, advertise all caps, prefer slave
Auto crossover, 125clk enabled
GMII to copper, Fiber autodetect disabled
Sleep mode disabled
MDC/MDIO, Active Low interrupt, 50 Ohm SERDE
U9
3.3V
E / D
VDD
OUT
GND
SiT8103AI-83-33E-25.00000
C137 100nF
C142 2.2µF
L7 MPZ1608S221A
Title:
A4
Nummer: GigaBee FPGA Module TE0600-02
Rev. 02
Datum: 2012-09-14
Zeichner: Trenz Electronic GmbH / TT
Blatt 9 von 11
Filename: 08.SchDoc
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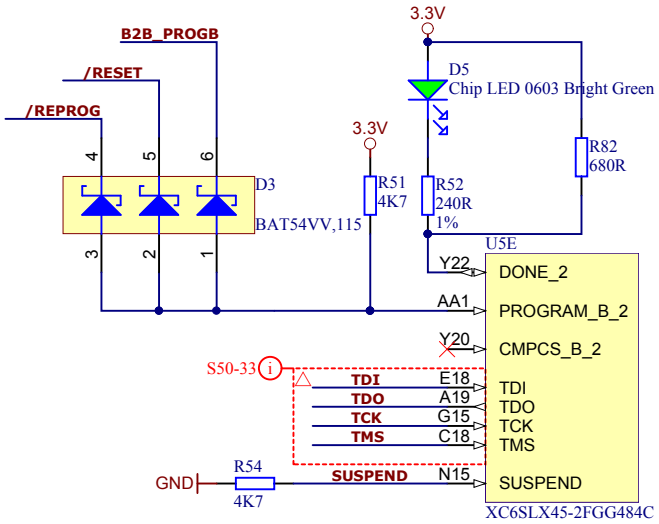
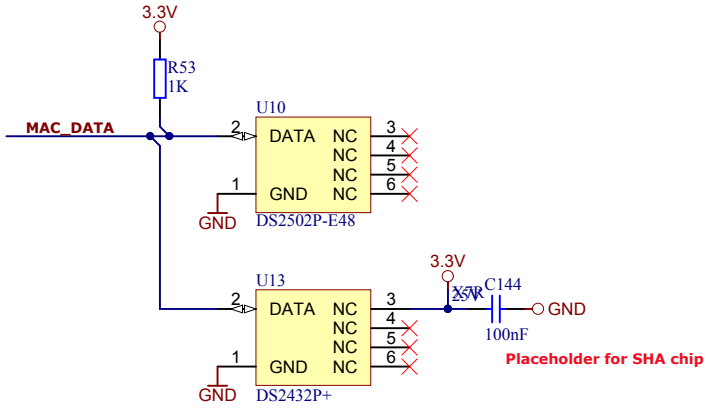
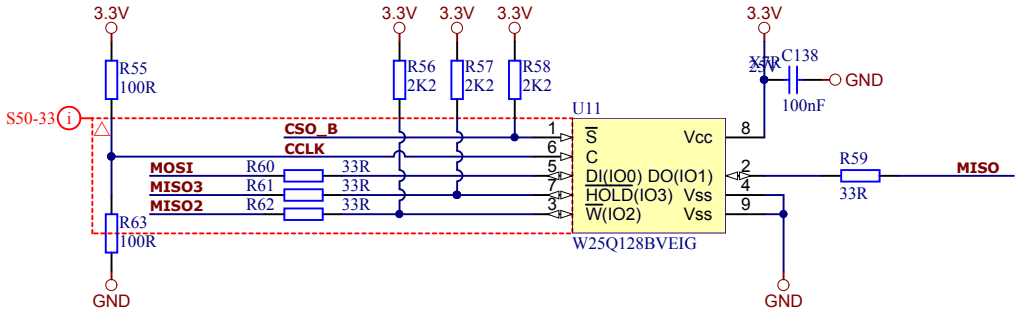
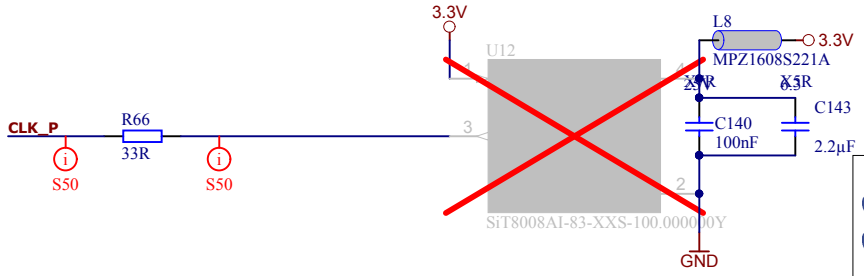


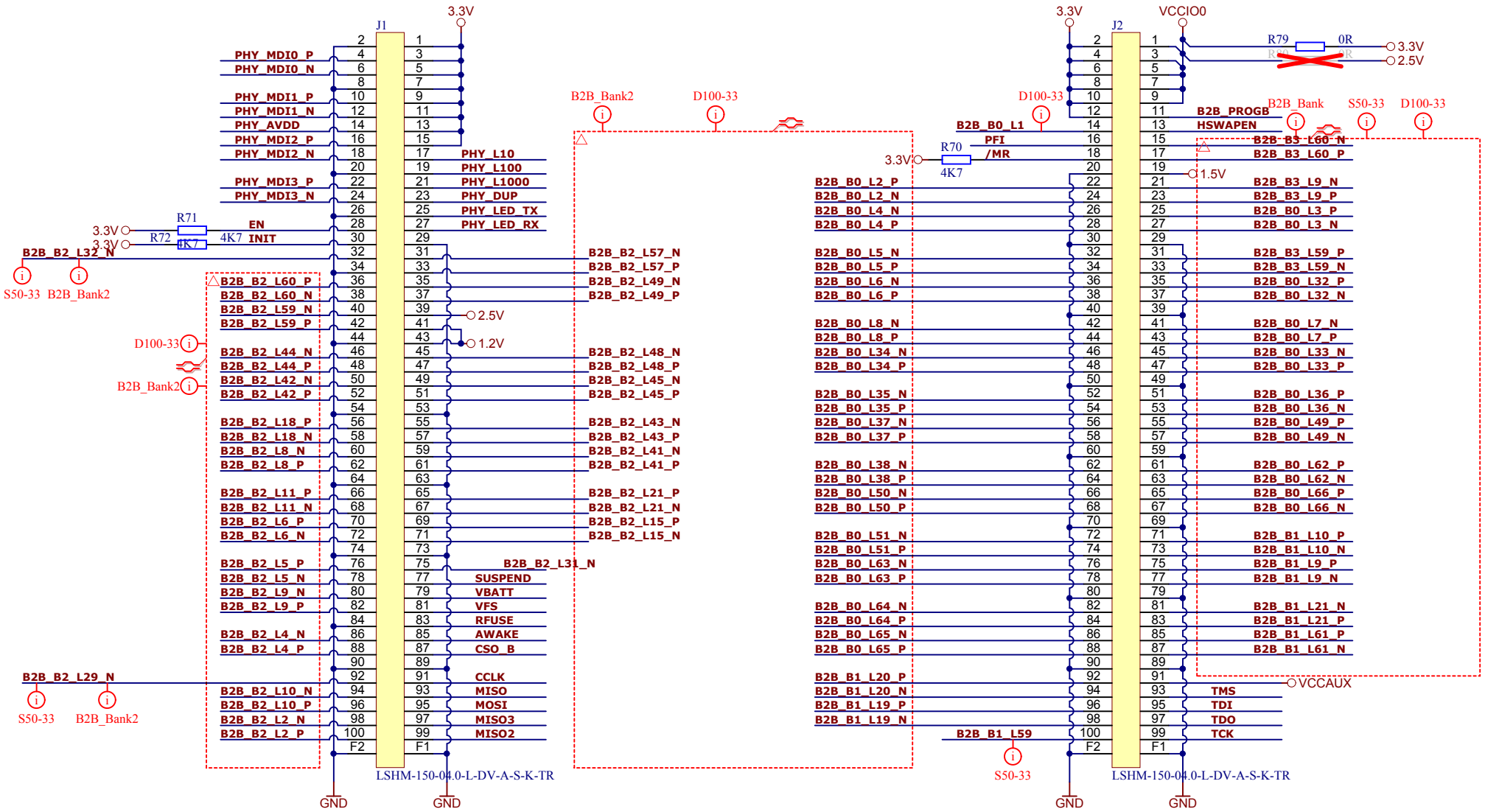




Put cclk termination close to the input pin



Title:		
A4	Nummer: GigaBee FPGA Module TE0600-02	Rev. 02
Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 10 von 11
Filename:	09.SchDoc	



trenz electronic	Title:		
	A4	Nummer: GigaBee FPGA Module TE0600-02	Rev. 02
	Datum: 2012-09-14	Zeichner: Trenz Electronic GmbH / TT	Blatt 11 von 11
	Filename:	10.SchDoc	