U_B2B-Connectors
B2B-Connectors.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_Clock
Clock.SchDoc

U_DDR3-RAM
DDR3-RAM.SchDoc

U_ETHERNET
ETHERNET.SchDoc

U_CPLD
CPLD.SchDoc

U_PWR1
PWR1.SchDoc

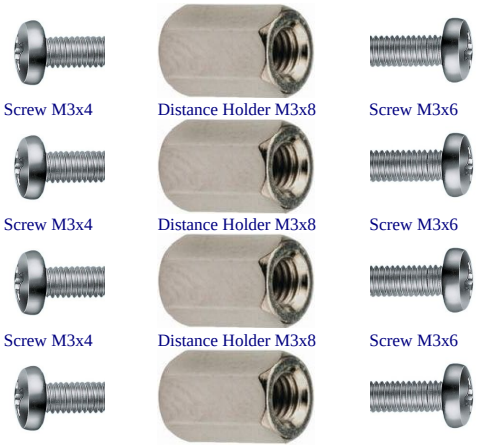
U_PWR2
PWR2.SchDoc

Serial
Serial
Serialnumber 6,3 x 6.3mm

FIDU-DOT - small FIDU-DOT - small
PM1 PM2
FIDU-DOT - small FIDU-DOT - small
PM3 PM4
FIDU-DOT - small FIDU-DOT - small
PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm
GND GND
Mount.Hole 3.2mm Mount.Hole 3.2mm
GND GND

Top of Board



Screw M3x4 Distance Holder M3x8 Screw M3x6
Screw M3x4 Distance Holder M3x8 Screw M3x6
Screw M3x4 Distance Holder M3x8 Screw M3x6
Screw M3x4 Distance Holder M3x8 Screw M3x6

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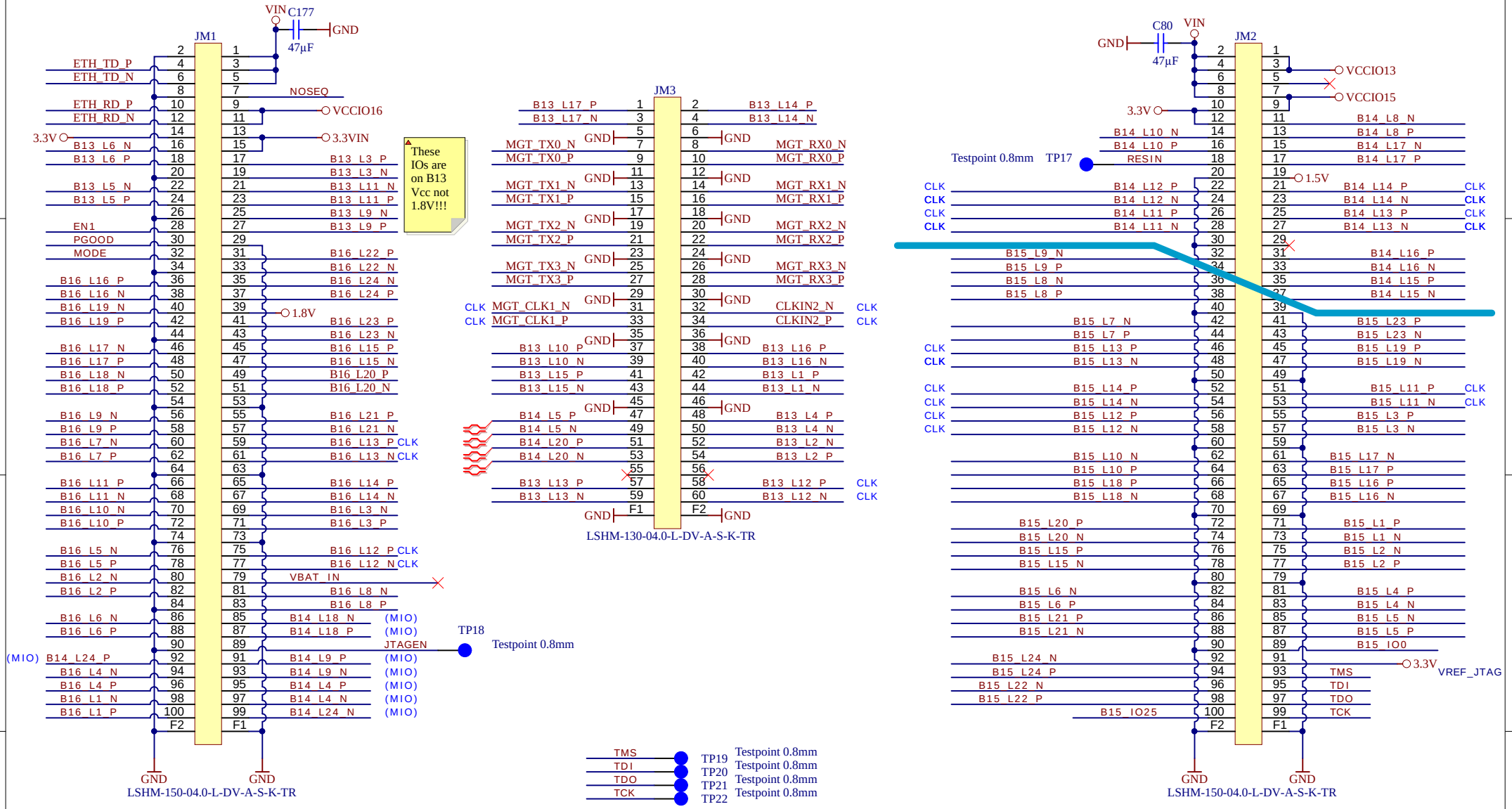
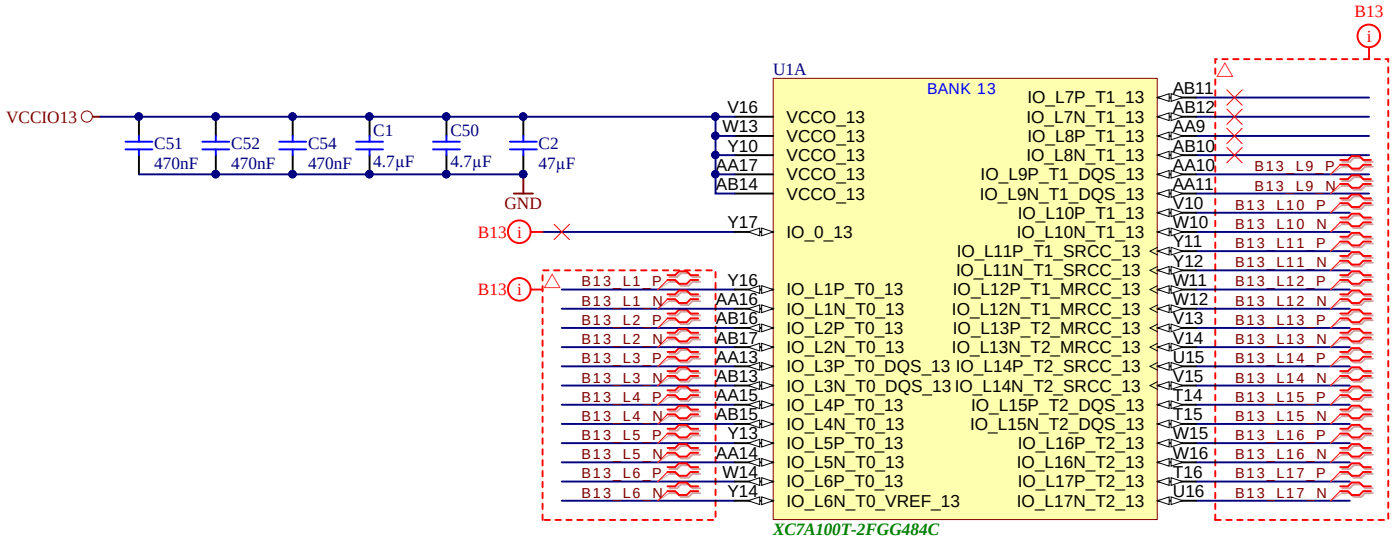
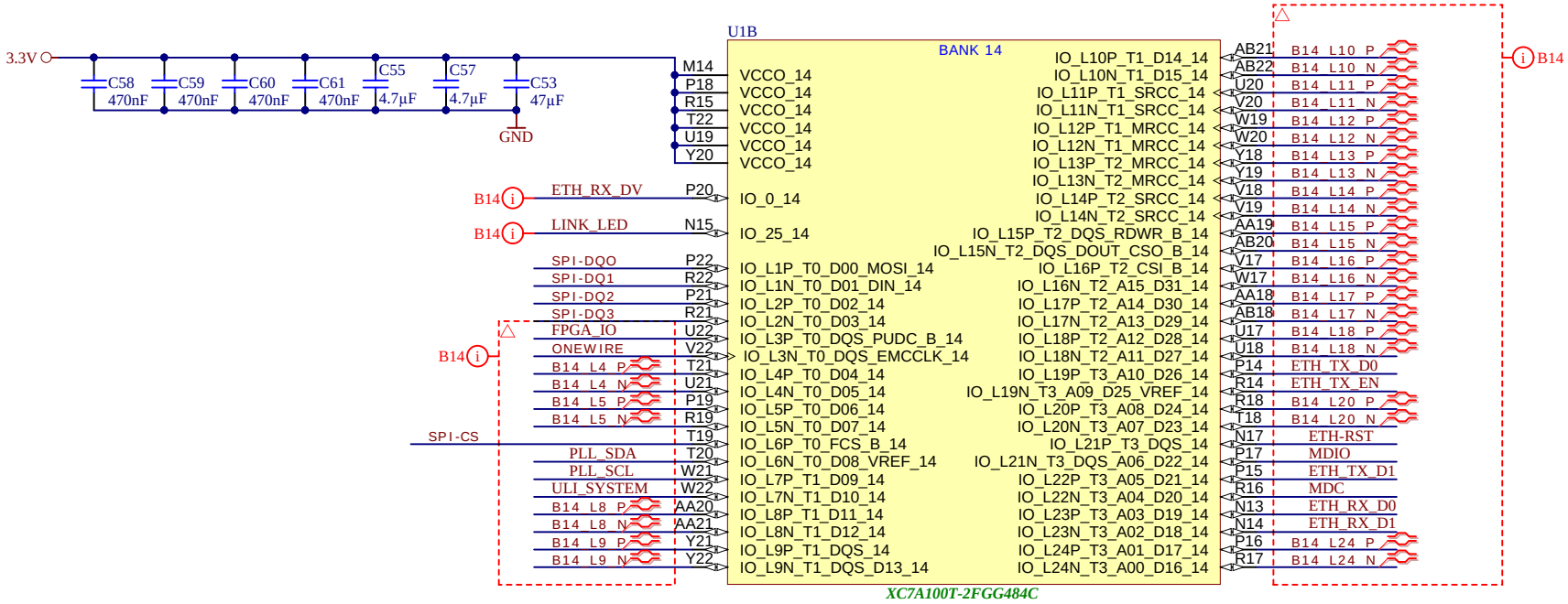
Title: TE0712		
A4	Number: TE0712 100_2CA	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page1 of 16
Filename: TE0712.SchDoc		



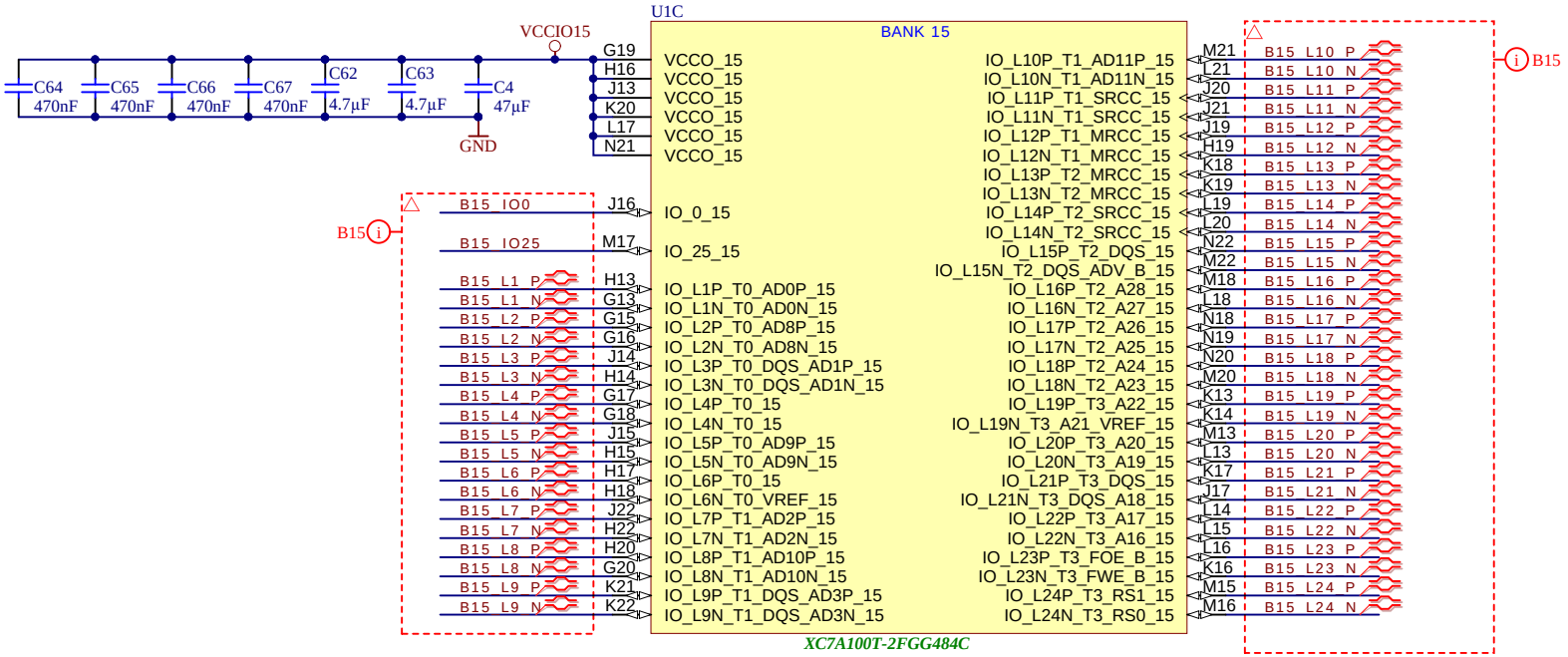
Title: B2B			
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page2 of 16
Filename: B2B-Connectors.SchDoc			



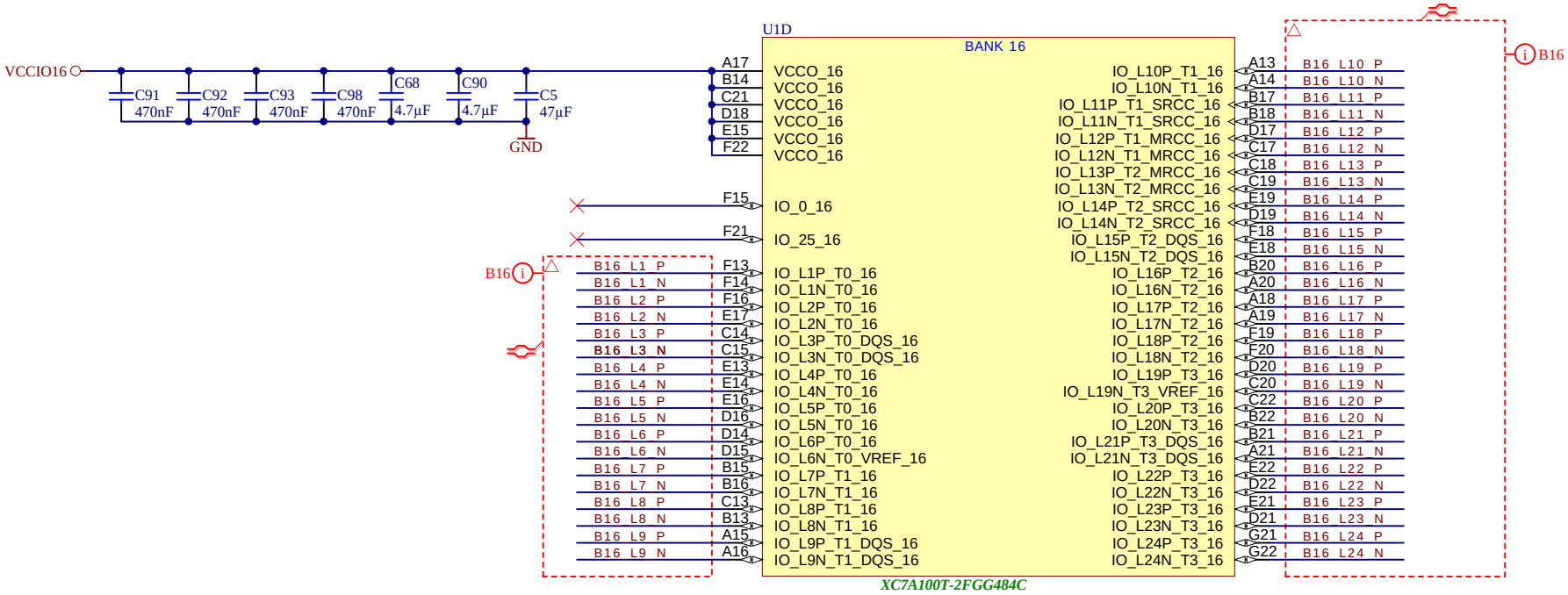
trenz electronic	Title: B13		
	A4	Number: TE0712 100_2CA	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page3 of 16
	Filename: B13.SchDoc		



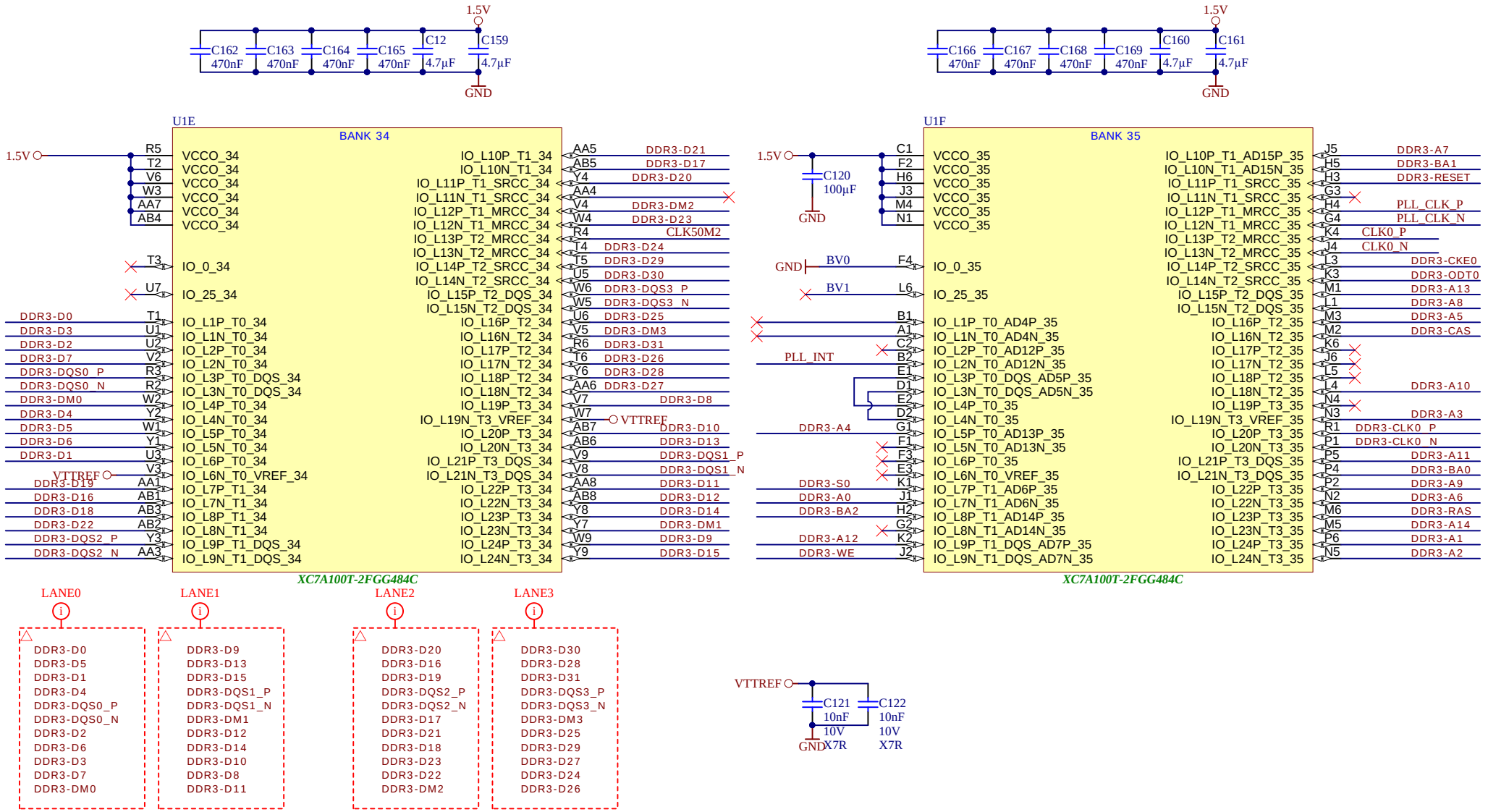
trenz electronic	Title: B14		
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page4 of 16
Filename: B14.SchDoc			



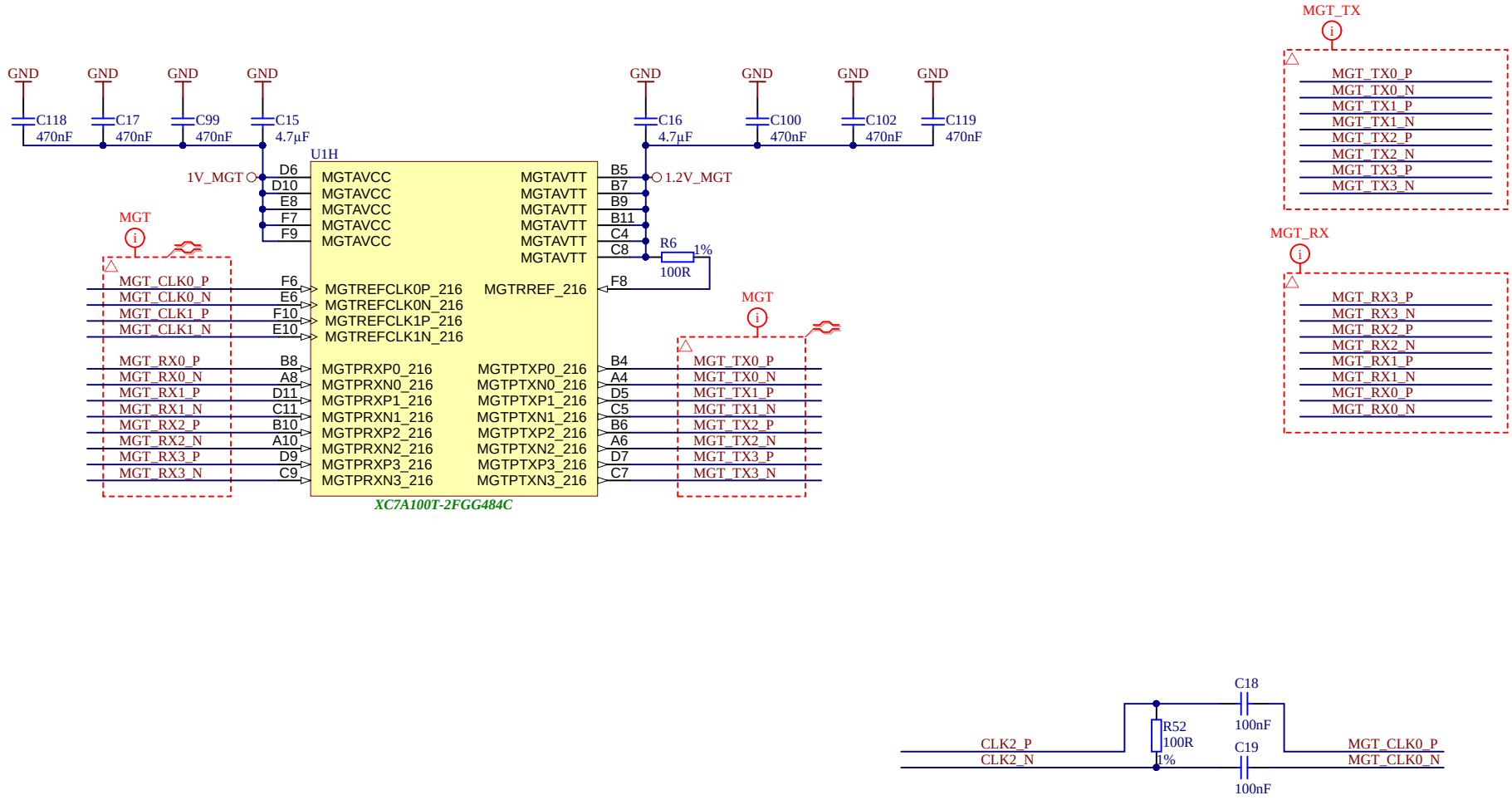
trenz electronic	Title: B15		
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page5 of 16
Filename: B15.SchDoc			



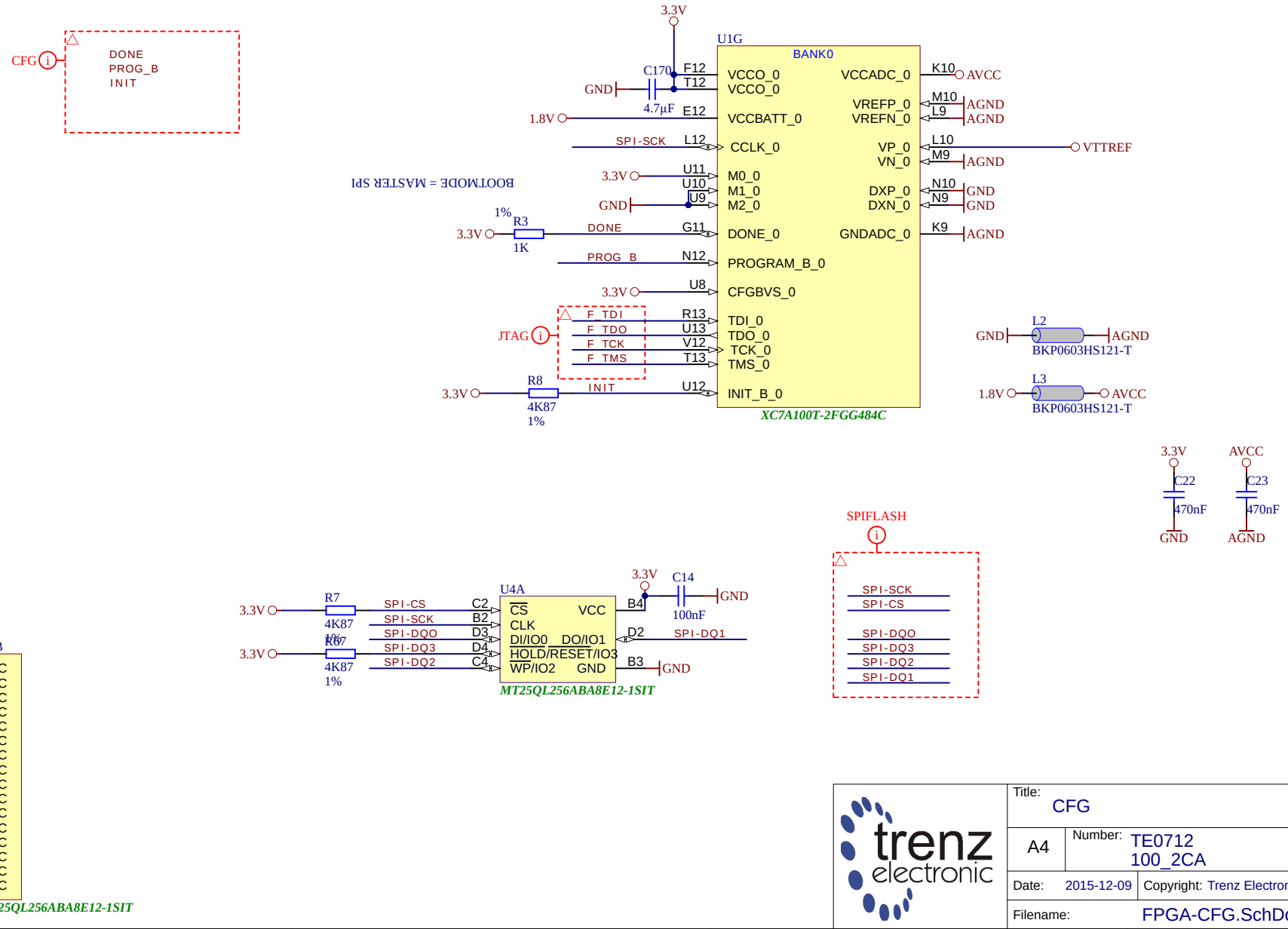
trenz electronic	Title: B16		
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page6 of 16
Filename: B16.SchDoc			



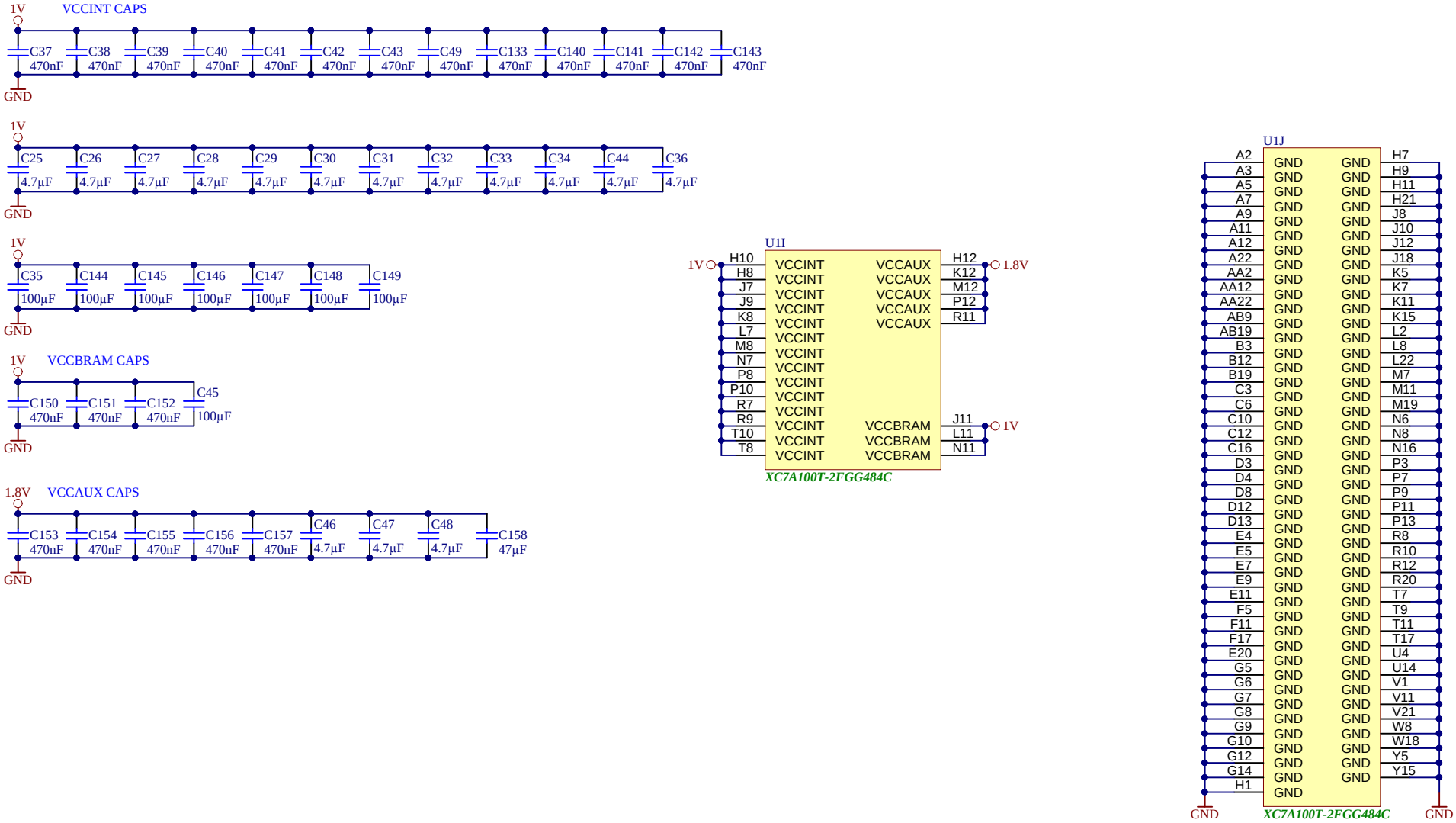
Title: B34			
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page7 of 16
Filename: B34.SchDoc			



trenz electronic	Title: MGT		
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page 8 of 16
Filename: FPGA-MGT.SchDoc			



trenz electronic	Title: CFG		
	A4	Number: TE0712 100_2CA	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page9 of 16
	Filename: FPGA-CFG.SchDoc		



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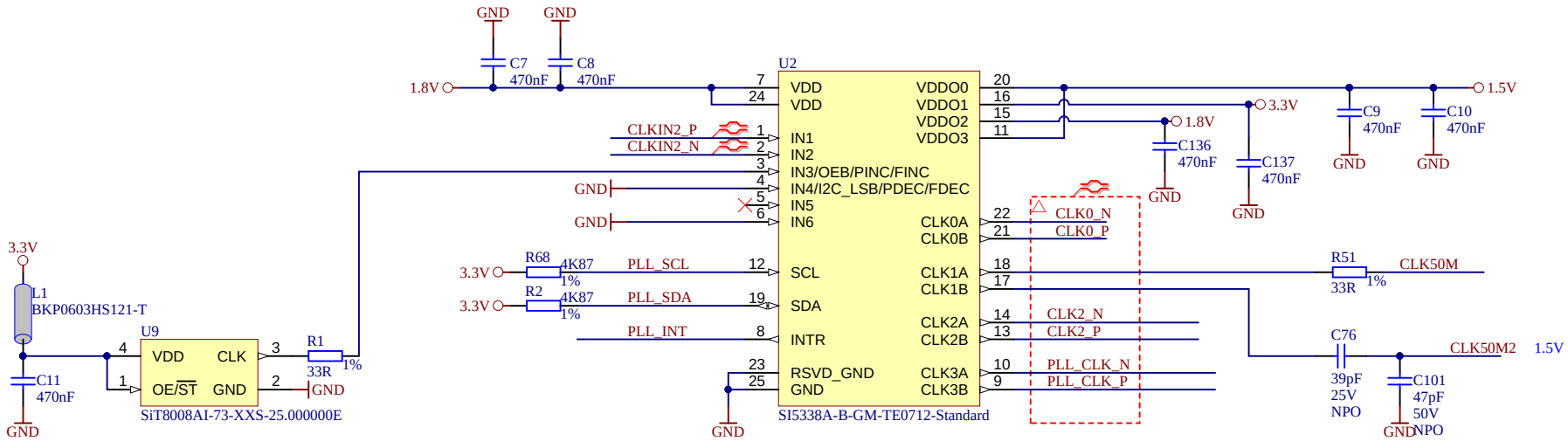
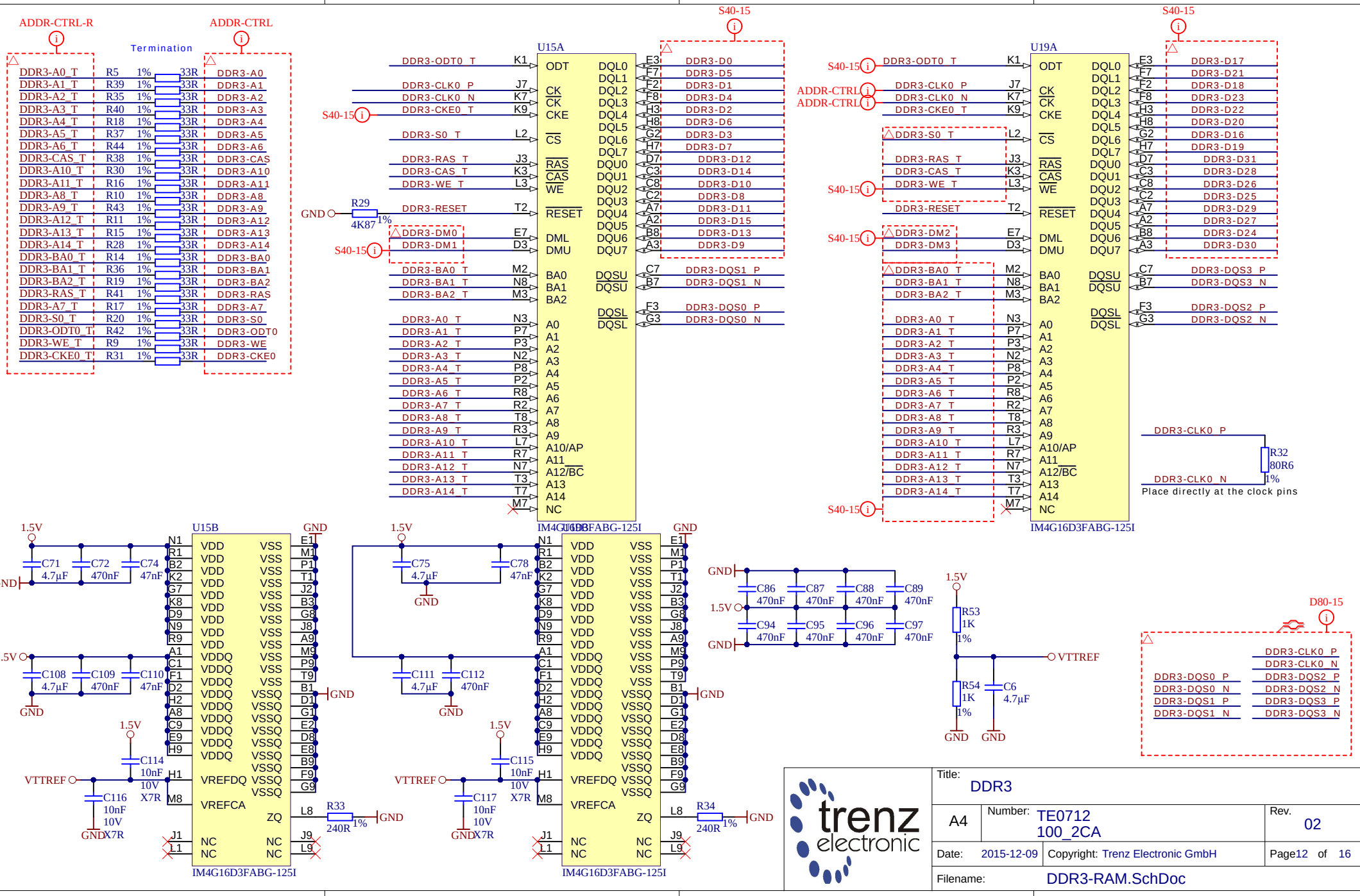
Title: PWR		
A4	Number: TE0712 100_2CA	Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page10 of 16
Filename: FPGA-PWR.SchDoc		



trenz electronic	Title: Clock		
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page11 of 16
Filename: Clock.SchDoc			


ADDR-CTRL-R
ADDR-CTRL
Termination
DDR3-A0_T R5 1% 33R DDR3-A0
DDR3-A1_T R39 1% 33R DDR3-A1
DDR3-A2_T R35 1% 33R DDR3-A2
DDR3-A3_T R40 1% 33R DDR3-A3
DDR3-A4_T R18 1% 33R DDR3-A4
DDR3-A5_T R37 1% 33R DDR3-A5
DDR3-A6_T R44 1% 33R DDR3-A6
DDR3-CAS_T R38 1% 33R DDR3-CAS
DDR3-A10_T R30 1% 33R DDR3-A10
DDR3-A11_T R16 1% 33R DDR3-A11
DDR3-A8_T R10 1% 33R DDR3-A8
DDR3-A9_T R43 1% 33R DDR3-A9
DDR3-A12_T R11 1% 33R DDR3-A12
DDR3-A13_T R15 1% 33R DDR3-A13
DDR3-A14_T R28 1% 33R DDR3-A14
DDR3-BA0_T R14 1% 33R DDR3-BA0
DDR3-BA1_T R36 1% 33R DDR3-BA1
DDR3-BA2_T R19 1% 33R DDR3-BA2
DDR3-RAS_T R41 1% 33R DDR3-RAS
DDR3-A7_T R17 1% 33R DDR3-A7
DDR3-S0_T R20 1% 33R DDR3-S0
DDR3-ODT0_T R42 1% 33R DDR3-ODT0
DDR3-WE_T R9 1% 33R DDR3-WE
DDR3-CKE0_T R31 1% 33R DDR3-CKE0
S40-15
U15A
U19A
ODT
CK
CKE
CS
RAS
CAS
WE
RESET
DML
DMU
BA0
BA1
BA2
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10/AP
A11
A12/BC
A13
A14
NC
DQSU
DQSL
DQL0
DQL1
DQL2
DQL3
DQL4
DQL5
DQL6
DQL7
DQU0
DQU1
DQU2
DQU3
DQU4
DQU5
DQU6
DQU7
R29
4K87 1%
GND
ADDR-CTRL
IM4G16D3FABG-125I
R32
80R6 1%
Place directly at the clock pins
1.5V
U15B
VDD
VSS
VDDQ
VSSQ
VREFDQ
VREFCA
ZQ
NC
C71 4.7µF
C72 470nF
C74 47nF
C75 4.7µF
C78 47nF
C86 470nF
C87 470nF
C88 470nF
C89 470nF
C94 470nF
C95 470nF
C96 470nF
C97 470nF
C108 4.7µF
C109 470nF
C110 47nF
C111 4.7µF
C112 470nF
C114 10nF 10V X7R
C115 10nF 10V X7R
C116 10nF 10V X7R
C117 10nF 10V X7R
VTTREF
R33 240R 1%
R34 240R 1%
R53 1K 1%
R54 1K 1%
C6 4.7µF
D80-15
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DQS3_P
DDR3-DQS3_N
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Title: DDR3
A4
Number: TE0712 100_2CA
Rev. 02
Date: 2015-12-09
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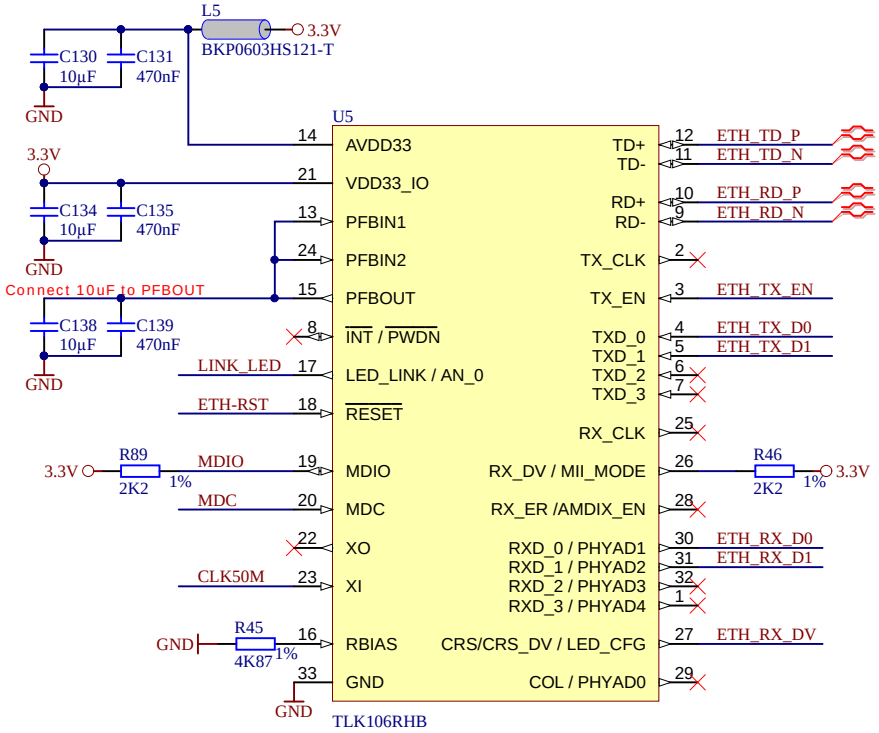
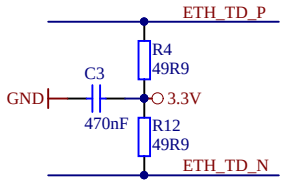
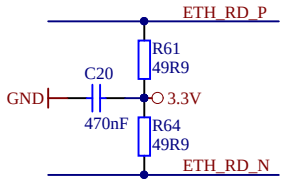
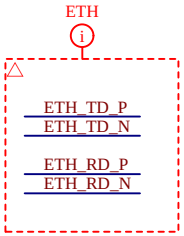
Page12 of 16
Filename: DDR3-RAM.SchDoc

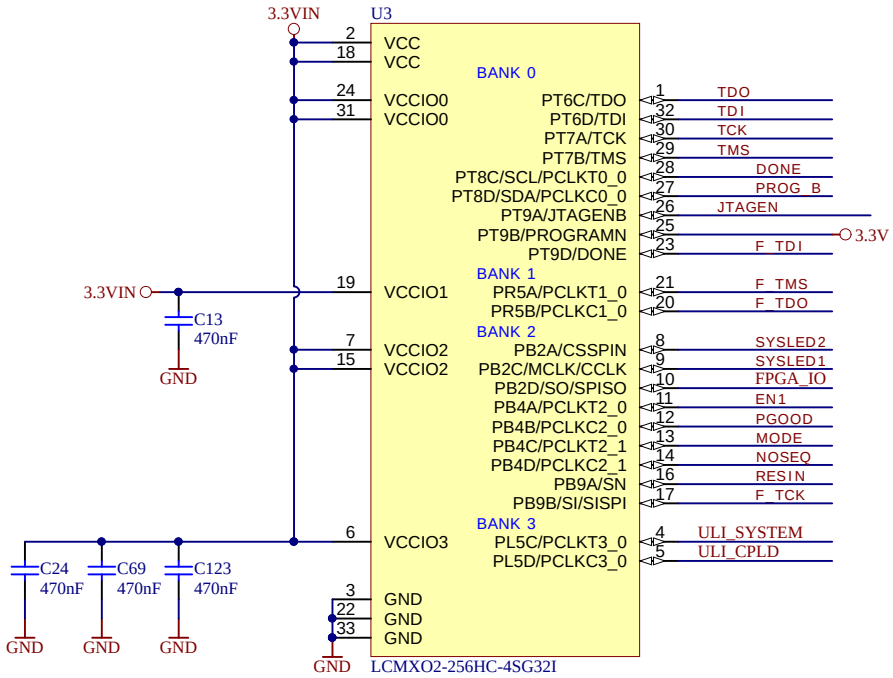


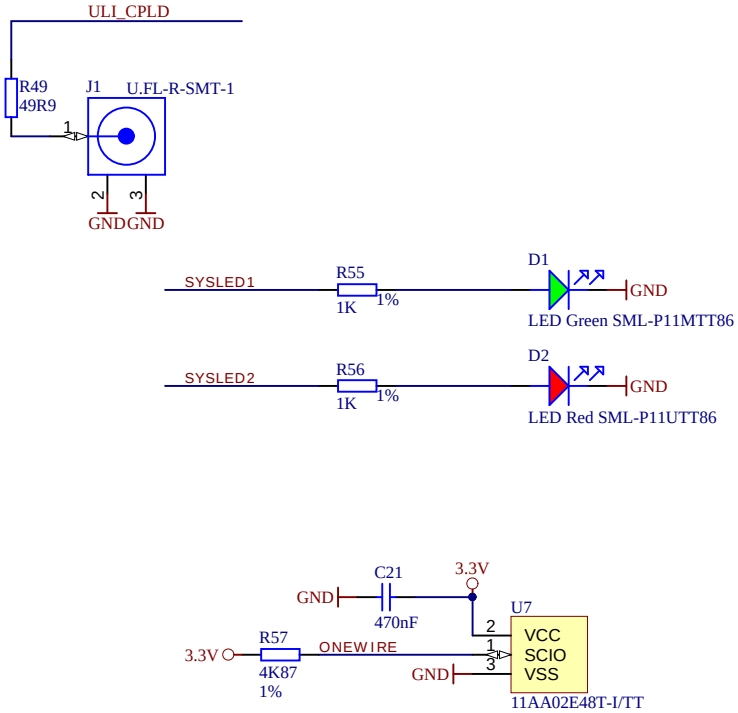




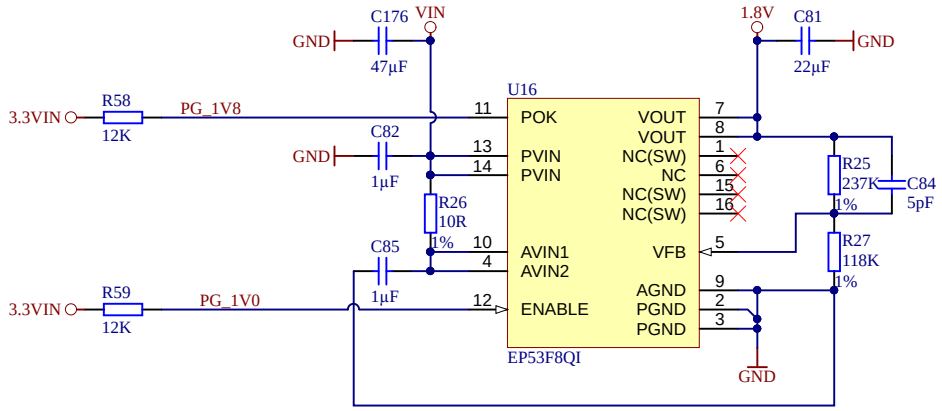


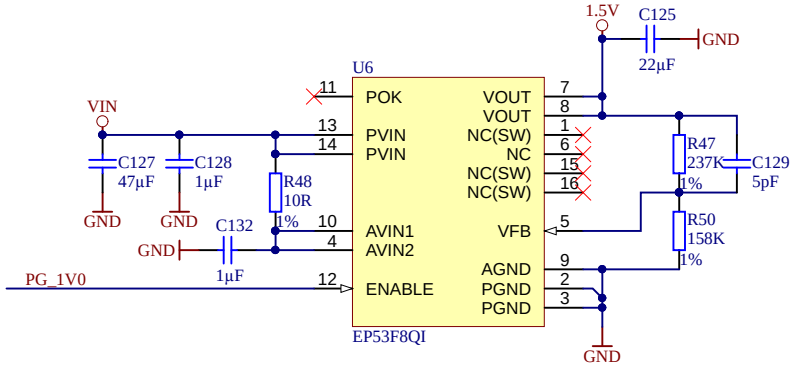
trenz electronic	Title: ETH		
	A4	Number: TE0712 100_2CA	Rev. 02
	Date: 2015-12-09	Copyright: Trenz Electronic GmbH	Page13 of 16
	Filename: ETHERNET.SchDoc		

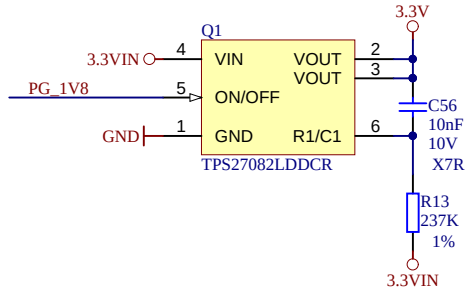


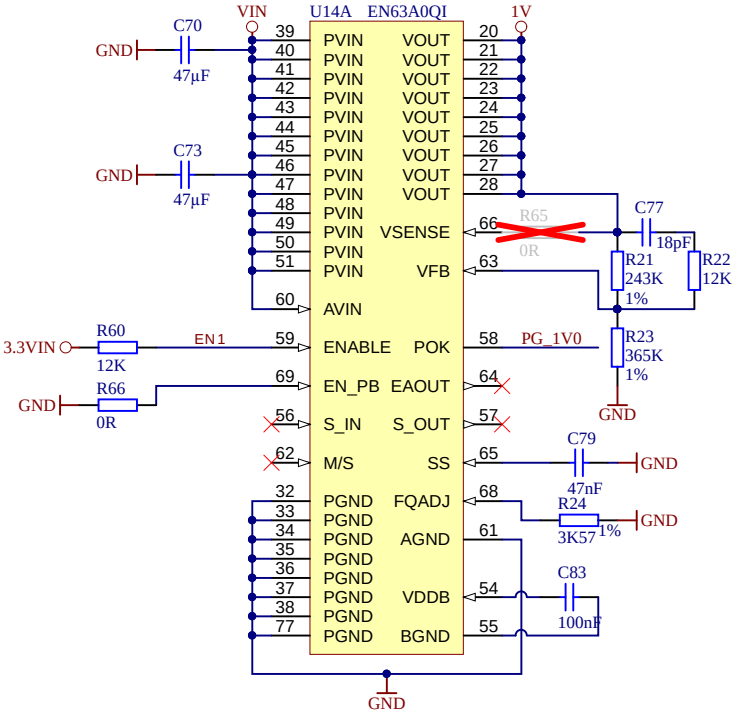


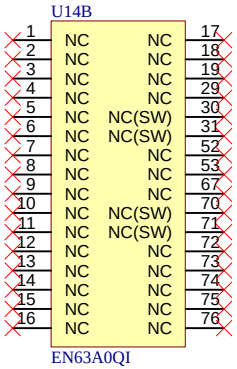
Title: CPLD			
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page14 of 16
Filename: CPLD.SchDoc			



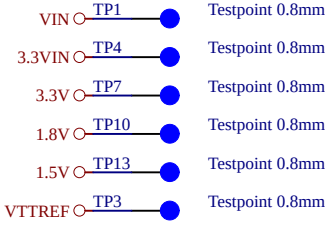


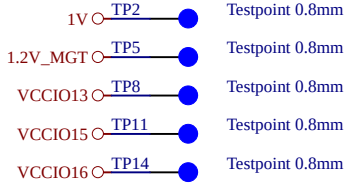


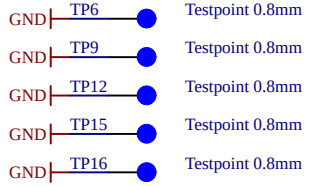




R65	R66	MODE EN63A0QI
OK	X	enable pre-bias start-up
X	OK	disable pre-bias start-up







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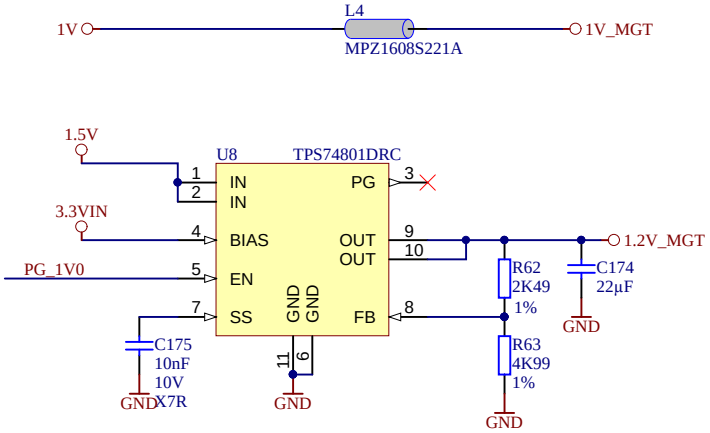
Title: PWR			
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page15 of 16
Filename: PWR1.SchDoc			



Title: PWR			
A4	Number: TE0712 100_2CA		Rev. 02
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page16 of 16
Filename: PWR2.SchDoc			