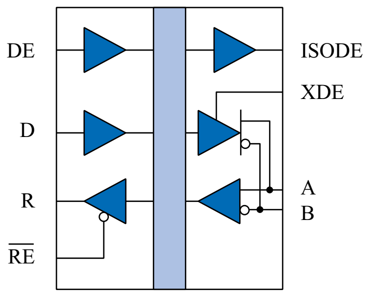
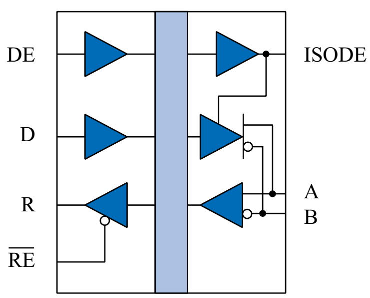
High Speed Isolated RS-485 Transceivers

Functional Diagrams



IL3585-3
(narrow-body)



IL3585
(wide-body)

V_{ID} (A-B)	DE	$\overline{RE}$	R	D	Mode	Notes
≥ 200 mV	L	L	H	X	Receive	
≤–200mV	L	L	L	X		
Open	L	L	H	X		A/B failsafe
≥ 1.5 V	H	L	H	H	Drive	R reads back D information
≤–1.5 V	H	L	L	L		
≥ 1.5 V	H	H	Z	H		R tri-state (no output)
≤–1.5 V	H	H	Z	L		
X	L	H	Z	X	Disabled	R tri-state; A/B failsafe

Features

- 40 Mbps data rate
- 6 kV_{RMS} Reinforced Isolation / 12.8 kV surge / 1.2 kV_{RMS} WV (IL3585VE)
- 3 V to 5 V power supplies
- 20 ns propagation delay
- 5 ns pulse skew
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- 44000 year barrier life
- 15 kV bus ESD protection
- Low EMC footprint
- Thermal shutdown protection
- –40 °C to +85 °C temperature range
- Meets or exceeds ANSI RS-485 and ISO 8482:1987(E)
- IEC 60747-17 (VDE 0884-17):2021-10 certified; UL 1577 recognized
- 0.15" or 0.3" True 8™ 16-pin SOIC packages

Applications

- Factory automation
- Industrial control networks
- Building environmental controls
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

The IL3585 is a galvanically isolated, high-speed differential bus transceiver, designed for bidirectional data communication on balanced transmission lines. The device uses NVE's patented* spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The part is available in an ultraminiature 0.15" 16-pin SOIC package, a JEDEC-standard 0.3"-wide package, or NVE's exclusive True 8™ 16-pin SOIC package for true 8 millimeter creepage.

The IL3585 delivers an exceptional 2.3 V differential output into a 54 Ω load over the supply range of 4.5 V to 5.5 V. This provides better data integrity over longer cable lengths, even at data rates as high as 40 Mbps. The device is also compatible with 3 V supplies, allowing interface to standard microcontrollers without additional level shifting.

Current limiting and thermal shutdown features protect against output short circuits and bus contention that may cause excessive power dissipation. Receiver inputs feature a "fail-safe if open" design, ensuring a logic high R-output if A/B are floating.

IsoLoop® is a registered trademark of NVE Corporation.
*U.S. Patent number 5,831,426; 6,300,617 and others.

REV. W

Absolute Maximum Ratings[11]

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Voltage Range at A or B Bus Pins		–7		12	V	
Supply Voltage[1]	V_{DD1}, V_{DD2}	–0.5		7	V	
Digital Input Voltage		–0.5		V_{DD} + 0.5	V	
Digital Output Voltage		–0.5		V_{DD} + 1	V	
ESD (all bus nodes)		15			kV	HBM

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Voltage	V_{DD1} V_{DD2}	3.0 4.5		5.5 5.5	V	
Ambient Operating Temperature	T_A	–40		85	°C	
Junction Temperature	T_J	–40		100	°C	
Input Voltage at any Bus Terminal (separately or common mode)	V_I V_{IC}			12 –7	V	
High-Level Digital Input Voltage	V_{IH}	2.4 3.0		V_{DD1}	V	V_{DD1} = 3.3 V V_{DD1} = 5.0 V
Low-Level Digital Input Voltage	V_{IL}	0		0.8	V	
Differential Input Voltage[2]	V_{ID}			+12 / –7	V	
High-Level Output Current (Driver)	I_{OH}			60	mA	
High-Level Digital Output Current (Receiver)	I_{OH}			8	mA	
Low-Level Output Current (Driver)	I_{OL}	–60			mA	
Low-Level Digital Output Current (Receiver)	I_{OL}	–8			mA	
Digital Input Signal Rise and Fall Times	t_{IR}, t_{IF}	DC Stable				

Safety and Approvals

IEC 60747-17 (VDE 0884-17):2021-10:

IL3585VE version (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage (V_{IORM}): 1200 V_{RMS} (1700 V_{PK}) with 20% Safety Factor; pollution degree 2
- Isolation voltage (V_{ISO}): 6000 V_{RMS}
- Surge immunity (V_{IOSM}): 12.8 kV_{PK}
- Surge rating: 8000 V
- Transient overvoltage (V_{IOTM}): 6000 V_{PK}
- Each part tested at 2387 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 V_{PK} for 60 sec.; then 2122 V_{PK} for 10 sec. with 5 pC partial discharge limit

Standard IL3585E versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit.

- Working Voltage (V_{IORM}; pollution degree 2):

Package	Part No. Suffix	Working Voltage
QSOP16	-1	600 V_{RMS}
Narrow-body SOIC16	-3	700 V_{RMS}
Wide-body SOIC16/True 8™	None	600 V_{RMS}

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180 °C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577 (Component Recognition Program File Number E207481)

Standard isolation grade

2500 V rating; each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute

V-Series isolation grade

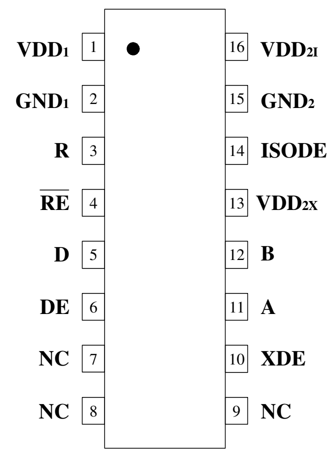
6 kV rating; each part tested at 7.2 kV_{RMS} (10.2 kV_{PK}) for 1 second; each lot sample tested at 6 kV_{RMS} (8485 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

IL3585-3 (0.15" SOIC Package) Pin Connections

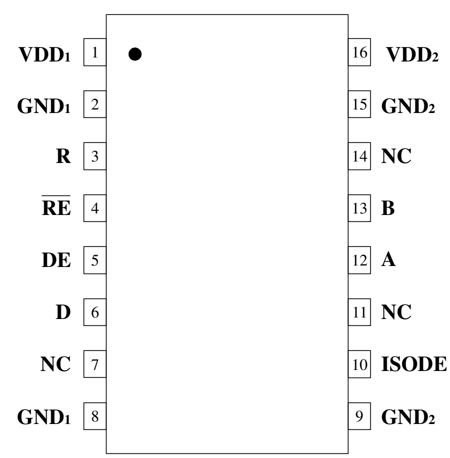
1	V_{DD1}	Input power supply
2	GND_1	Input power supply ground return
3	R	Output data from bus
4	$\overline{RE}$	Read data enable (if $\overline{RE}$ is high, R= high impedance)
5	D	Data input to bus
6	DE	Drive enable
7, 8, 9	NC	No internal connection
10	XDE	Transceiver Device Enable input enables the transceiver from the bus side, or is connected to ISODE to enable the trans-ceiver from the controller-side DE input. (this input should not be left unterminated)
11	A	Non-inverting bus line
12	B	Inverting bus line
13	V_{DD2X}	Output transceiver power supply (normally connected to pin 16)
14	ISODE	Isolated DE output (normally connected to pin 10)
15	GND_2	Output power supply ground return.
16	V_{DD2I}	Output isolation power supply (normally connected to pin 13)



IL3585-3

IL3585 (0.3" SOIC Package) Pin Connections

1	V_{DD1}	Input power supply
2	GND_1	Input power supply ground return (pin 2 is internally connected to pin 8)
3	R	Output data from bus
4	$\overline{RE}$	Read data enable (if RE is high, R= high impedance)
5	DE	Drive enable
6	D	Data input to bus
7	NC	No internal connection
8	GND_1	Input power supply ground return (pin 8 is internally connected to pin 2)
9	GND_2	Output power supply ground return (pin 9 is internally connected to pin 15)
10	ISODE	Isolated DE output for use in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored.
11	NC	No internal connection
12	A	Non-inverting bus line
13	B	Inverting bus line
14	NC	No internal connection
15	GND_2	Output power supply ground return (pin 15 is internally connected to pin 9)
16	V_{DD2}	Output power supply



IL3585

Driver Section

Electrical Specifications (T_{min} to T_{max} and V_{DD} = 4.5 V to 5.5 V unless otherwise stated)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Clamp Voltage	V_{IK}			−1.5	V	I_L = −18 mA
Output voltage	V_O			V_{DD}	V	I_O = 0
Differential Output Voltage(2)	$\|V_{OD1}\|$			V_{DD}	V	I_O = 0
Differential Output Voltage(2)	$\|V_{OD2}\|$	2.5	3	5	V	R_L = 54 Ω, V_{DD} = 5 V
Differential Output Voltage(2)	V_{OD3}	2.3		5	V	R_L = 54 Ω, V_{DD} = 4.5 V
Change in Magnitude of Differential Output Voltage(4)	$\Delta\|V_{OD}\|$			±0.2	V	R_L = 54 Ω or 100 Ω
Common Mode Output Voltage	V_{OC}			3	V	R_L = 54 Ω or 100 Ω
Change in Magnitude of Common Mode Output Voltage(4)	$\Delta\|V_{OC}\|$			±0.2	V	R_L = 54 Ω or 100 Ω
Output Current	I_O			1 −0.8	mA	Output Disabled, V_O = 12 V_O = −7
High Level Input Current	I_{IH}			10	µA	V_I = 3.5 V
Low Level Input Current	I_{IL}			−10	µA	V_I = 0.4 V
Absolute |Short-circuit Output Current|	I_{OS}			250	mA	−7 V < V_O < 12 V

Receiver Section

Electrical Specifications (T_{min} to T_{max} and V_{DD} = 4.5 V to 5.5 V unless otherwise stated)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Positive-going Input Threshold Voltage	V_{IT+}			0.2	V	−7 V < V_{CM} < 12 V
Negative-going Input Threshold Voltage	V_{IT-}	−0.2			V	−7 V < V_{CM} < 12 V
Hysteresis Voltage ($V_{IT+} - V_{IT-}$)	V_{HYS}		40		mV	V_{CM} = 0 V, T = 25°C
High Level Digital Output Voltage	V_{OH}	V_{DD} – 0.2	V_{DD}		V	V_{ID} = 200 mV I_{OH} = −20 µA
Low Level Digital Output Voltage	V_{OL}			0.2	V	V_{ID} = −200 mV I_{OH} = 20 µA
High-impedance-state output current	I_{OZ}			±1	µA	V_O = 0.4 to (V_{DD2}–0.5) V
Line Input Current	I_I			1	mA	V_I = 12 V
				−0.8	mA	V_I = −7 V
Input Resistance	R_I	20			kΩ	

Power Consumption

T_{min} to T_{max} and V_{DD2} = 5 V unless otherwise stated						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Controller-Side Quiescent Current V_{DD1} = 3.3 V V_{DD1} = 5 V	I_{DD1}		3 4	4 6	mA	f_{IN} = 0 Hz
Bus-Side Quiescent Supply Current	I_{DD2}		5	16	mA	Outputs Enabled; R_T = ∞; f_{IN} = 0 Hz ; V_{DD2X} connected to V_{DD2I} if applicable
Controller-Side Dynamic Supply Current	I_{DD1}		0.22		mA/Mbps	V_{DD1} = 3.3 V
Bus-Side Dynamic Supply Current	$\Delta I_{DD2}/\Delta f_{IN}$		1		mA/Mbps	R_T = ∞
			0.8			R_T = 60 Ω

Switching Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
V_{DD1} = 5 V, V_{DD2} = 5 V						
Data Rate		40			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay(5)	t_{PD}		27	35	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew(6)	$t_{SK}(P)$		1	6	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Skew Limit(3)	$t_{SK}(LIM)$		2	12	ns	R_L = 54 Ω, C_L = 50 pF
Output Enable Time To High Level	t_{PZH}		15	25	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		15	25	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		15	25	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		15	25	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/μs	V_{CM} = 1500 V_{DC}, $t_{TRANSIENT}$ = 25 ns
V_{DD1} = 3.3 V, V_{DD2} = 5 V						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		40			Mbps	R_L = 54 Ω, C_L = 50 pF
Propagation Delay(5)	t_{PD}		30	38	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Pulse Skew(6)	$t_{SK}(P)$		1	6	ns	V_O = −1.5 to 1.5 V, C_L = 15 pF
Skew Limit(3)	$t_{SK}(LIM)$		4	12	ns	R_L = 54 Ω, C_L = 50 pF
Output Enable Time To High Level	t_{PZH}		17	27	ns	C_L = 15 pF
Output Enable Time To Low Level	t_{PZL}		17	27	ns	C_L = 15 pF
Output Disable Time From High Level	t_{PHZ}		17	27	ns	C_L = 15 pF
Output Disable Time From Low Level	t_{PLZ}		17	27	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/μs	V_{CM} = 1500 V_{DC}, $t_{TRANSIENT}$ = 25 ns

Magnetic Field Immunity(8)

V_{DD1} = 5 V, V_{DD2} = 5 V						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8μs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			
V_{DD1} = 3.3 V, V_{DD2} = 5 V						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8μs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Insulation Specifications

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	IL3585-3E		4.0			mm	Per IEC 60601
	IL3585E		8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)			0.013	0.016		mm	
Barrier Resistance		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance		C_{IO}		3		pF	f = 1 MHz
Leakage Current				0.2		$μA_{RMS}$	240 V_{RMS}, 60 Hz
Comparative Tracking Index		CTI	≥600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC	V_{IO}	1500			V_{DC}	At maximum operating temperature
Surge Immunity ("V" Versions)		V_{IOSM}	12.8 kV			V_{PK}	Per IEC 61000-4-5
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC	θ_{JA}		100 82 67		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC	θ_{JC}		9 8 12		°C/W	Double-sided PCB in free air
Junction–Ambient Thermal Resistance	0.3" SOIC	θ_{JA}		46		°C/W	2s2p PCB in free air per JESD51
Junction–Case (Top) Thermal Resistance	0.3" SOIC	θ_{JC}		9		°C/W	2s2p PCB in free air per JESD51
Power Dissipation	QSOP 0.15" SOIC 0.3" SOIC	P_D			675 700 1500	mW	

Notes:

1. All voltages are with respect to network ground except differential I/O bus voltages.
2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3. Skew limit is the maximum propagation delay difference between any two devices at 25°C.
4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
5. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
6. Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel.
7. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section.
9. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin.”

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Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Narrow- and Wide-Body Pinout Differences

The narrow-body version (IL3585-3E) is designed for application flexibility and minimum board area in densely-populated PCAs. The wide-body version (IL3585E) has redundant ground pins for layout flexibility.

The narrow-body version provides a separate isolated DE output (ISODE) and Transceiver Device Enable (XDE) input. ISODE follows the Device Enable input (DE). XDE can be used to enable and disable the transceiver from the bus side, or connected to ISODE to enable and disable the transceiver from the DE controller-side input. The narrow-body version also provides separate bus-side power supply pins—V_{DD2X} for the transceiver module and V_{DD2I} for the isolation module. These pins should be externally connected for normal operation, but they can be used separately for testing or troubleshooting.

The wide-body version has internal connections between the isolated DE output and the Transceiver Device Enable input, and well as between the two V_{DD2} bus-side power supply pins. The two internally GND pins for each supply side provide layout flexibility. The ISODE output can be used in PROFIBUS applications where the state of the isolated drive enable node needs to be monitored, or for testing or troubleshooting.

Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on frequency and time.

Data Rate (Mbps)	I_{DD1}	I_{DD2}
1	150 µA	150 µA
10	1.5 mA	1.5 mA
20	3 mA	3 mA
40	6 mA	6 mA

Table 2. Typical Dynamic Supply Currents.

Power Supply Decoupling

V_{DD1} and V_{DD2} should be bypassed with 0.1 µF typical (47 nF minimum) capacitors as close as possible to the V_{DD} pins.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

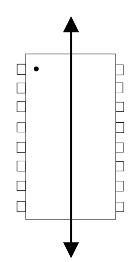
DC Correctness

The IL3585 incorporates a patented refresh circuit to maintain the correct output state with respect to data input. At power up, the bus outputs will follow the Function Table shown on Page 1. The DE input should be held low during power-up to eliminate false drive data pulses from the bus. An external power supply monitor to minimize glitches caused by slow power-up and power-down transients is not required.

Electromagnetic Compatibility

The IL3585 is fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is “end-to-end” (rather than to “pin-to-pin”) as shown in the diagram at right:



Application Information

Figures 1a and 1b show typical connections to a microcontroller for the narrow-body and wide-body versions. The schematics include typical termination and fail-safe resistors, and power supply decoupling capacitors:

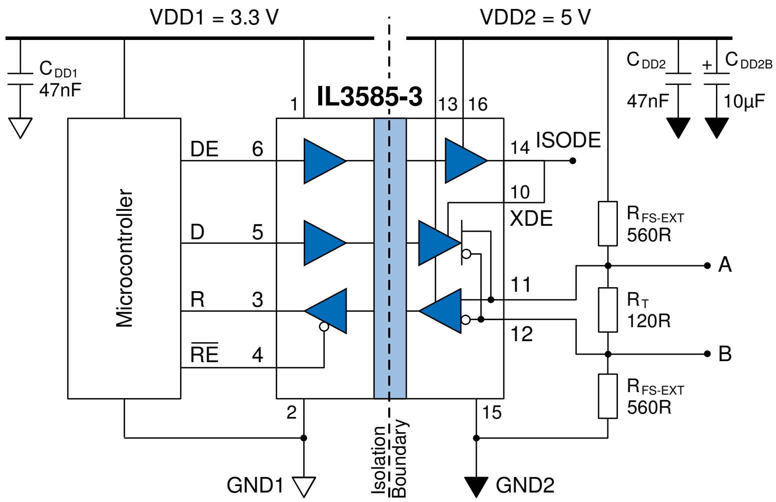


Figure 1a. Typical narrow-body connections.

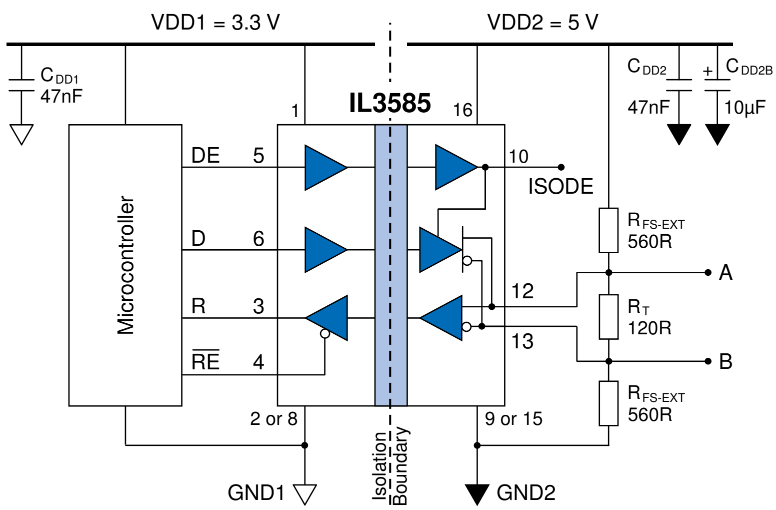


Figure 1b. Typical wide-body connections.

Receiver Features

The receiver output "R" has tri-state capability via the active low $\overline{\text{RE}}$ input.

Driver Features

The RS-485 driver has a differential output and delivers at least 2.1 V across a 54 Ω load. Drivers feature low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

Receiver Data Rate, Cables and Terminations

The IL3585 is intended for networks up to 4,000 feet (1,200 m), but the maximum data rate decreases as cable length increases. Twisted pair cable should be used in all networks since they tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receiver.

Fail-Safe Operation

"Fail-safe operation" is defined here as the forcing of a logic high state on the "R" output in response to an open-circuit condition between the "A" and "B" lines of the bus, or when no drivers are active on the bus.

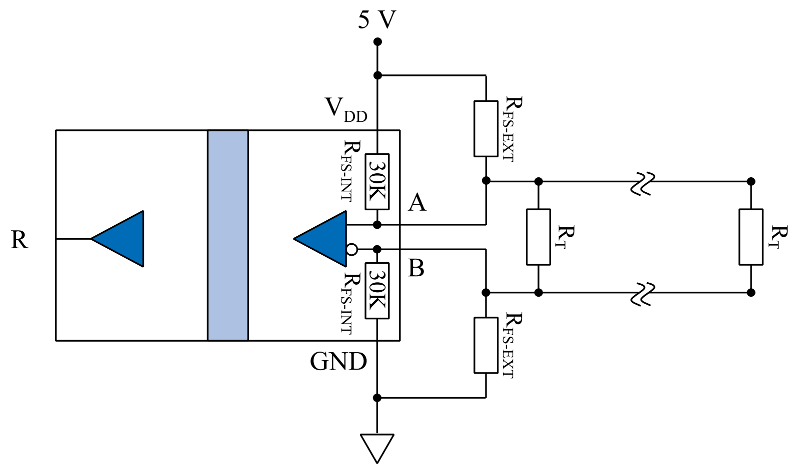
Proper biasing can ensure fail-safe operation, that is a known state when there are no active drivers on the bus. IL3000-Series Isolated Transceivers include internal pull-up and pull-down resistors of approximately 30 kΩ in the receiver section ($R_{FS\text{-}INT}$; see figure below). These internal resistors are designed to ensure failsafe operation but only if there are no termination resistors. The entire V_{DD} will appear between inputs "A" and "B" if there is no loading and no termination resistors, and there will be more than the required 200 mV with up to four RS-485 worst-case Unit Loads of 12 kΩ. Many designs operating below 1 Mbps or less than 1,000 feet are unterminated. Termination resistors may not be necessary for very low data rates and very short cable runs because reflections have time to settle before data sampling, which occurs at the middle of the bit interval.

In busses with low-impedance termination resistors however, the differential voltage across the conductor pair will be close to zero with no active drivers. In this case the state of the bus is indeterminate, and the idle bus will be susceptible to noise. For example, with 120 Ω termination resistors (R_T) on each end of the cable, and four Unit Loads (12 kΩ each), without external fail-safe biasing resistors the internal pull-up and pull-down resistors will produce a voltage between inputs "A" and "B" of only about 5 mV. This is not nearly enough to ensure a known state. External fail-safe biasing resistors ($R_{FS\text{-}EXT}$) at one end of the bus can ensure fail-safe operation with a terminated bus. Resistors should be selected so that under worst-case power supply and resistor tolerances there is at least 200 mV across the conductor pair with no active drivers to meet the input sensitivity specification of the RS-485 standard.

Using the same value for pull-up and pull-down biasing resistors maintains balance for positive- and negative going transitions. Lower-value resistors increase inactive noise immunity at the expense of quiescent power consumption. Note that each Unit Load on the bus adds a worst-case loading of 12 kΩ across the conductor pair, and 32 Unit Loads add 375 Ω worst-case loading. The more loads on the bus, the lower the required values of the biasing resistors.

In the example with two 120 Ω termination resistors and four Unit Loads, 560 Ω external biasing resistors provide more than 200 mV between "A" and "B" with adequate margin for power supply variations and resistor tolerances. This ensures a known state when there are no active drivers. Other illustrative examples are shown in the table below:

Fail-Safe Biasing



$R_{FS\text{-}EXT}$	R_T	Loading	Nominal $V_{A\text{-}B}$ (inactive)	Fail-Safe Operation?
Internal Only	None	Four unit loads (12 kΩ ea.)	238 mV	Yes
Internal Only	120 Ω	Four unit loads (12 kΩ ea.)	5 mV	No
560 Ω	120 Ω	Four unit loads (12 kΩ ea.)	254 mV	Yes
510 Ω	120 Ω	32 unit loads (12 kΩ ea.)	247 mV	Yes

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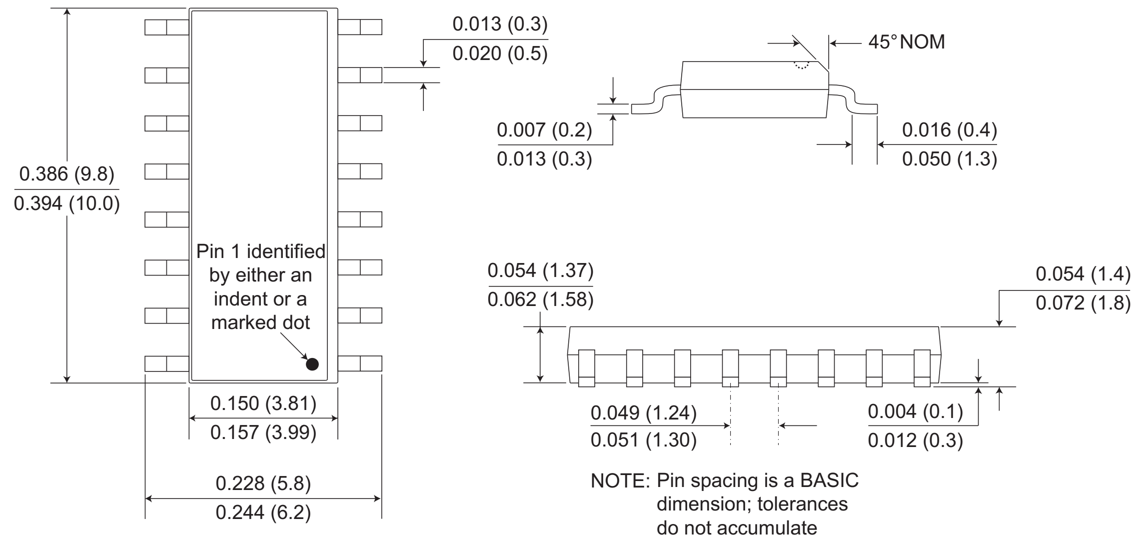
Package Drawings

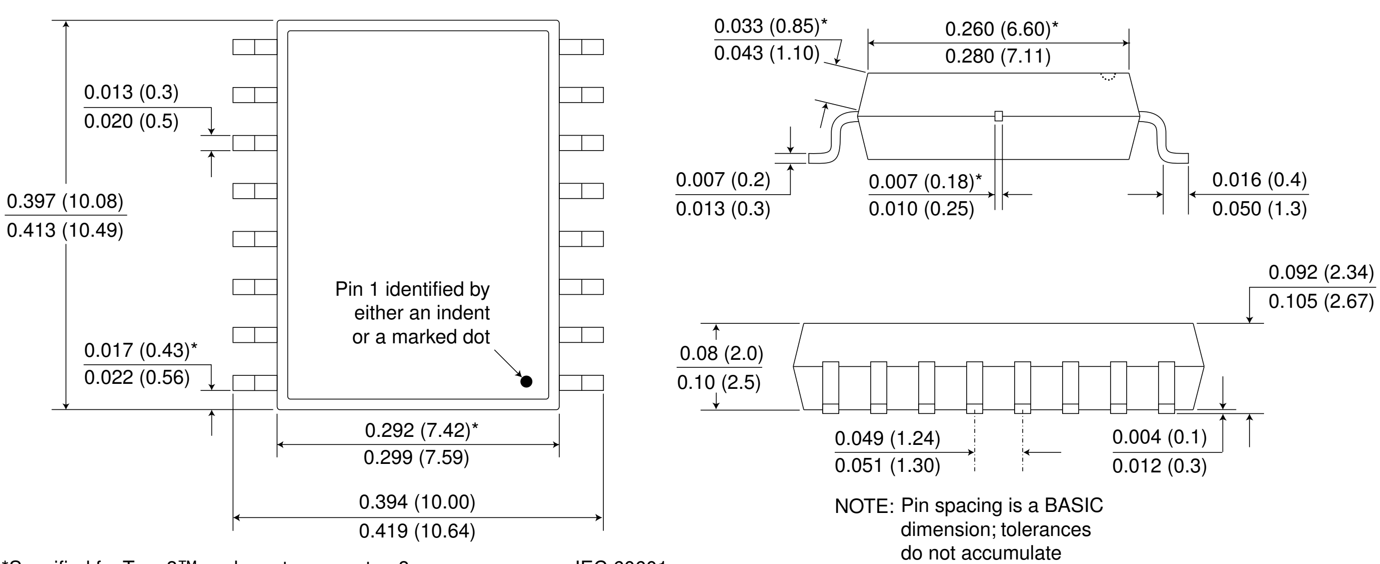
0.15" 16-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Package (no suffix)

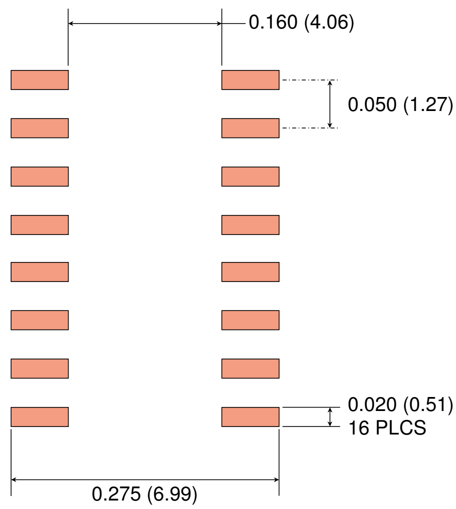
Dimensions in inches (mm); scale = approx. 5X



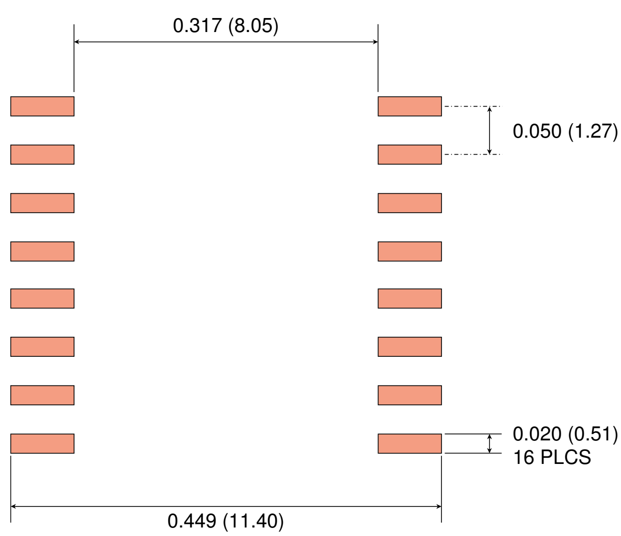
*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

0.15" 16-pin SOIC Pad Layout



0.3" 16-pin SOIC Pad Layout



Ordering Information and Valid Part Numbers

IL 35 85 -3 V E TR13

Bulk Packaging
Blank = Tube
TR13 = 13" Tape and Reel

Package
E = RoHS Compliant

Isolation Grade
Blank = 2.5 kV Isolation / 600 WV
V = 6 kV Isolation / 1 kV WV

Package Type
Blank = 0.3" SOIC
-3 = 0.15" SOIC

Channel Configuration
85 = RS-485

Base Part Number
35 = Digital-In, 40 Mbps Transceiver

Product Family
IL = Isolators

Valid Part Numbers
IL3585E
IL3585E TR13
IL3585-3E
IL3585-3E TR13

IL3585VE
IL3585VE TR13

RoHS COMPLIANT

Revision History

ISB-DS-001-IL3585-W
August 2022

Changes

- Clarified truth table (p. 1).
- Upgraded to IEC 60747-17 (VDE 0884-17):2021-10 (p. 3).
- Increased Working Voltage ratings based on latest VDE testing (p. 3).
- Separate power consumption specifications section; added dynamic power consumption (p. 5).
- Revised thermal characteristics (p. 7).
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications (p. 6) since it is not 100% tested.

ISB-DS-001-IL3585-V

Change

- Updated VDE Reinforced Isolation file number and description.

ISB-DS-001-IL3585-U

Changes

- Updated VDE certification standard to VDE V 0884-10.
- Upgraded "V" Version Surge Immunity specification to 12.8 kV.
- Upgraded "V" Version VDE 0884-10 rating to reinforced insulation.

ISB-DS-001-IL3585-T

Changes

- Increased V-Series isolation voltage to 6 kV_{RMS}.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to ≥600 V_{RMS}.

ISB-DS-001-IL3585-S

Changes

- Increase V-Series surge voltage specification to 10 kV.
- Upgraded V-Series safety and approval from IEC 60747-5-5 (VDE 0884) to VDE 0884-10.

ISB-DS-001-IL3585-R

Change

- Added V-Series versions (5 kVrms isolation / 1000 Vrms working voltage)

ISB-DS-001-IL3585-Q

Changes

- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.

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ISB-DS-001-IL3585-W

August 2022