

MSHM30N46

N-Channel 30-V (D-S) MOSFET

Description

The device is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The device meets the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- $R_{DS(ON)} = 9m\Omega @ V_{GS} = 10V$
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Typical Applications

- MB / VGA / Vcore
- POL Applications
- SMPS 2nd SR

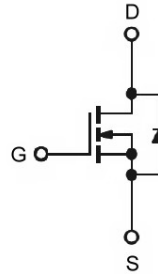
Package type : PDFN 3.3X3.3

Packing & Order Information

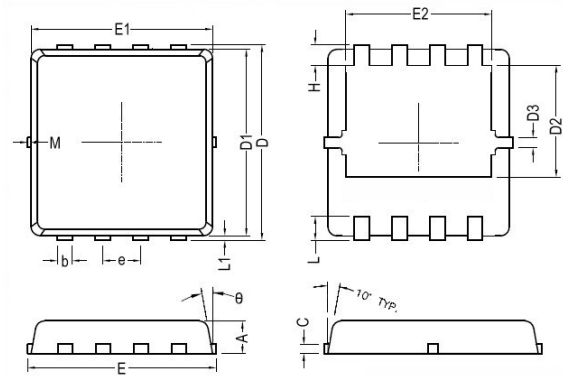
3,000/Reel



Graphic Symbol

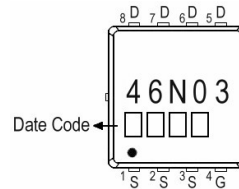


Package Dimension



REF.	Millimeter			REF.	Millimeter		
	Min.	Nom.	Max.		Min.	Nom.	Max.
A	0.70	0.75	0.80	E1	3.00	3.15	3.20
b	0.25	0.30	0.35	E2	2.39	2.49	2.59
C	0.10	0.15	0.25	e	0.65 BSC		
D	3.25	3.35	3.45	H	0.30	0.39	0.50
D1	3.00	3.10	3.20	L	0.30	0.40	0.50
D2	1.78	1.88	1.98	L1	-	0.13	0.20
D3	-	0.13	-	θ	-	10°	12°
E	3.20	3.30	3.40	M	-	-	0.15

Marking



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MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ¹ ($T_C = 25^\circ\text{C}$)	46 ⁴	A
	Continuous Drain Current ¹ ($T_C = 100^\circ\text{C}$)	29	A
I_{DM}	Pulsed Drain Current ^{1,2}	92	A
I_{AS}	Single Pulse Avalanche Current, $L = 0.1\text{mH}^3$	34	A
E_{AS}	Single Pulse Avalanche Energy, $L = 0.1\text{mH}^3$	57.8	mJ
P_D	Power Dissipation ⁴ ($T_C = 25^\circ\text{C}$)	29	W
	Power Dissipation ⁴ ($T_A = 25^\circ\text{C}$)	1.67	W
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ¹	75	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Maximum Junction-to-Case ¹	4.3	$^\circ\text{C}/\text{W}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	-	2.5	V
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30	-	-	V
g_{fs}	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 15\text{A}$	-	9.8	-	S
I_{GSS}	Gate-Source Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$	-	-	5	μA
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS} = 10\text{V}, I_D = 15\text{A}$	-	-	9	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$	-	-	15	m Ω
E_{AS}	Single Pulse Avalanche Energy ⁵	$V_{DD} = 25\text{V}, L = 0.1\text{mH}, I_{AS} = 20\text{A}$	20	-	-	mJ
V_{SD}	Diode Forward Voltage ²	$I_S = 15\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	1.2	V
I_S	Continuous Source Current ^{1,6}	$V_G = V_D = 0\text{V}, \text{Force Current}$	-	-	40	A
I_{SM}	Pulsed Source Current ^{2,6}		-	-	80	

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Dynamic						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Q _g	Total Gate Charge ²	V _{DS} = 20V	--	12.8	--	nC
Q _{gs}	Gate-Source Charge	I _D = 12A	--	3.3	--	
Q _{gd}	Gate-Drain Charge	V _{GS} = 4.5V	--	6.5	--	
t _{d(on)}	Turn-On Delay Time ²	V _{DS} = 12V	--	4.5	--	ns
t _r	Rise Time	I _D = 5A	--	10.8	--	
t _{d(off)}	Turn-Off Delay Time	V _{GS} = 10V	--	25.5	--	
t _f	Fall Time	R _G = 3.3Ω	--	9.6	--	
C _{iss}	Input Capacitance	V _{DS} = 15V	--	1317	--	pF
C _{oss}	Output Capacitance	V _{GS} = 0V	--	163	--	
C _{rss}	Reverse Transfer Capacitance	f = 1.0MHz	--	131	--	
R _g	Gate Resistance	V _{GS} = V _{DS} = 0V, f = 1.0MHz	--	1.7	--	Ω

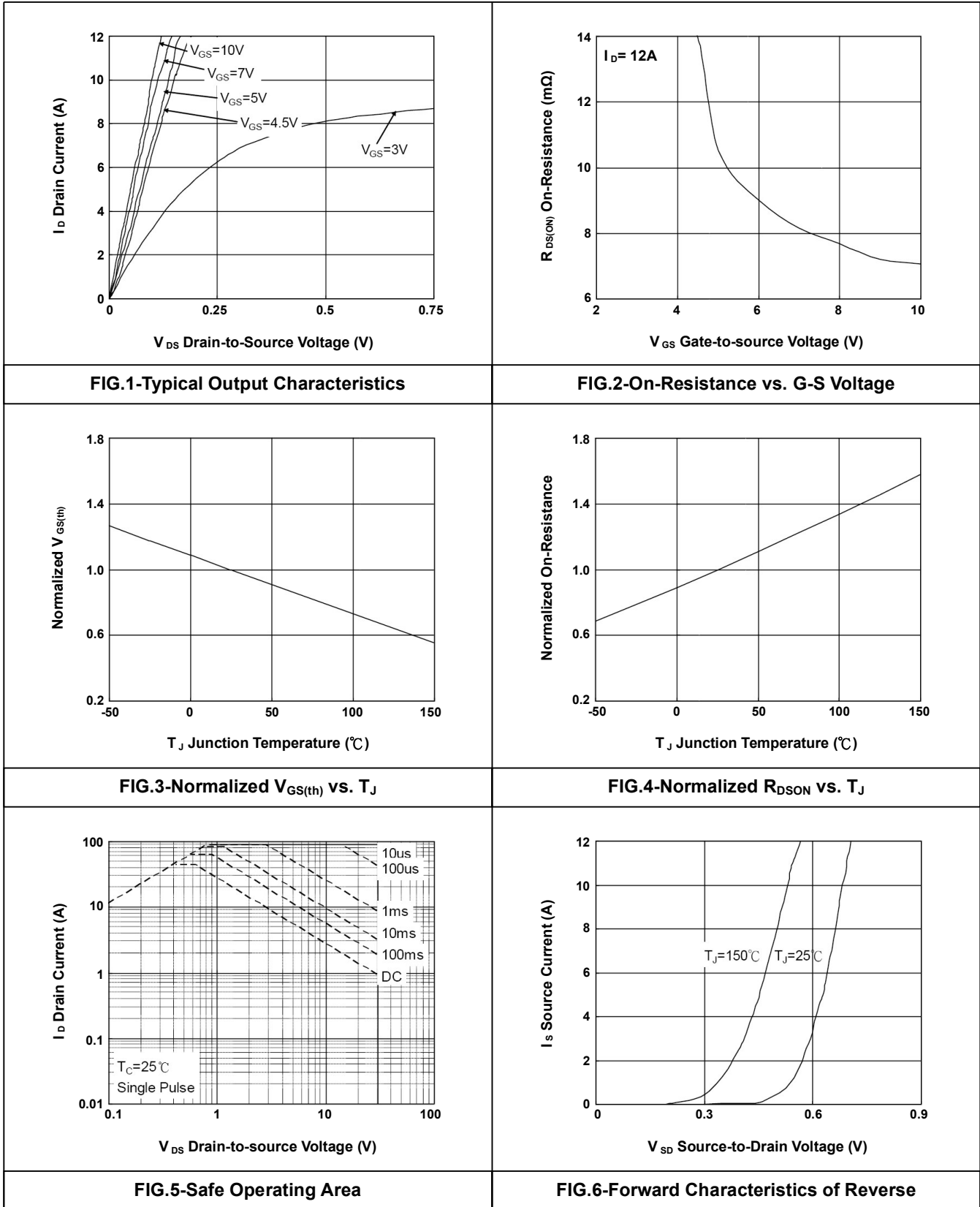
Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The EAS data shows maximum rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=34A.
4. The power dissipation is limited by 150°C junction temperature. Package Limitation current is 40A.
5. The Min. value is 100% EAS tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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- Typical Electrical Characteristics



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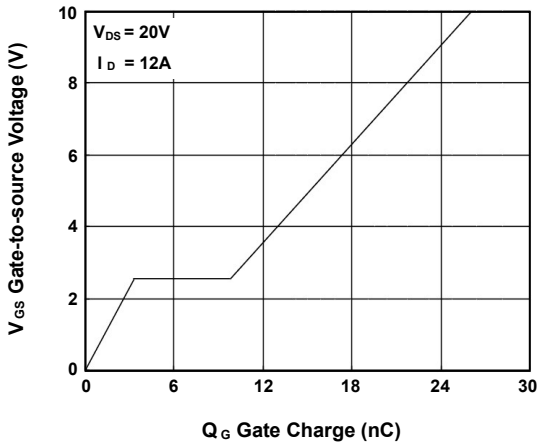


FIG.7-Gate Charge Characteristics

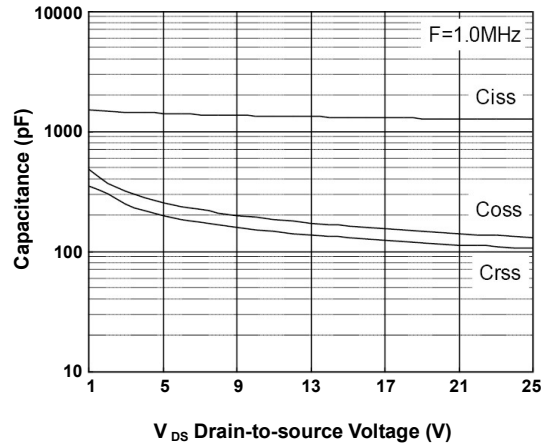


FIG.8-Capacitance Characteristics

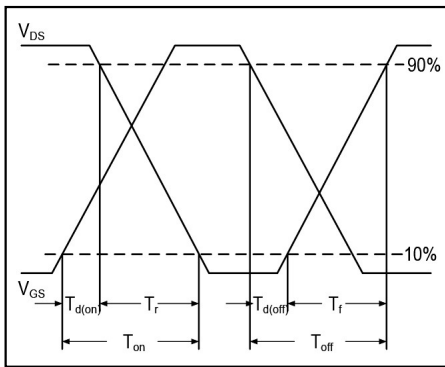


FIG.9-Switching Time Waveform

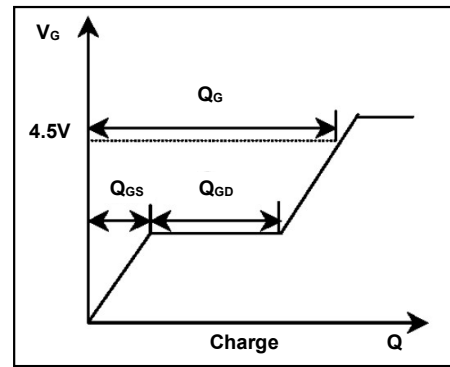


FIG.10-Gate Charge Waveform

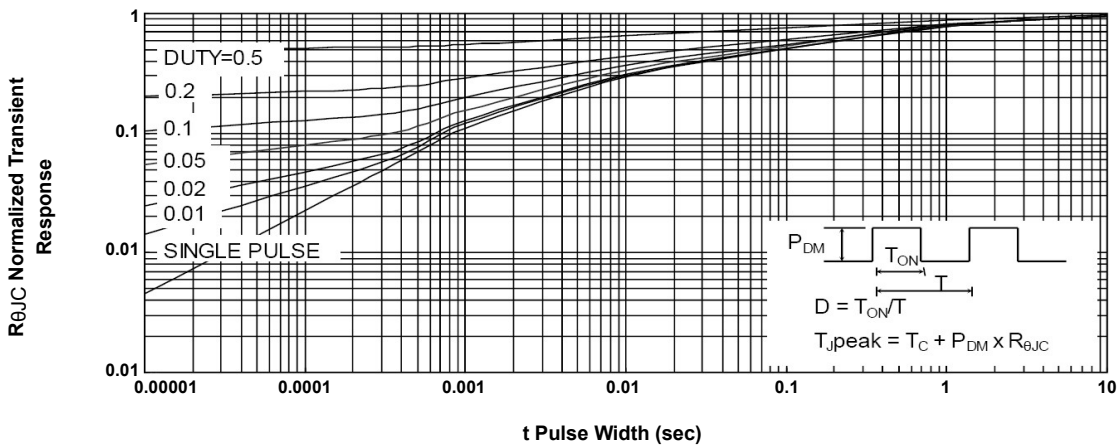


FIG.11-Normalized Maximum Transient Thermal Impedance

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