XR79120

22V, 20A Synchronous Step Down COT Power Module

General Description

The XR79120 is a 20A synchronous step-down Power Module for point-of load supplies. A wide 4.5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V, and 19.6V rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR79120 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation, hence simplifying circuit implementation and reducing overall component count. The control loop also provides 0.12% load and 0.17% line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in discontinuous mode (DCM) at light current loads, thereby significantly increasing the converter efficiency. With a 93% peak efficiency and 84% for loads as low as 100mA, the XR79120 is suitable for applications where low power losses are important.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XR79120 is available in a RoHS compliant, green / halogen free space-saving 74-pin 12 x 14 x 4mm QFN package. With integrated controller, drivers, bootstrap diode and capacitor, MOSFETs, inductor, CIN and COUT, this solution allows the smallest possible 20A POL design.

FEATURES

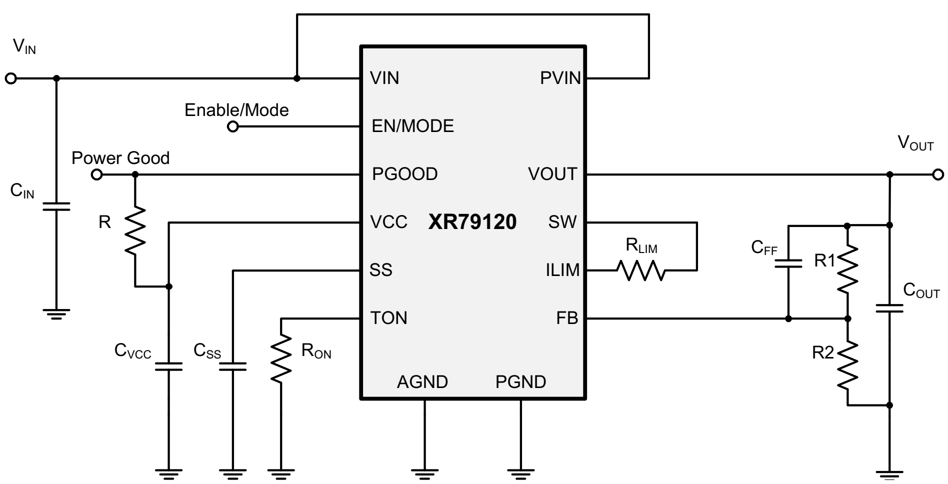
- Controller, drivers, bootstrap diode and capacitor, MOSFETs, Inductor, CIN and COUT integrated in one package
- 20A step down module
  - Wide 4.5V to 22V input voltage range
  - ≥0.6V adjustable output voltage
- Proprietary Constant On-Time control
  - No loop compensation required
  - Stable ceramic output capacitor operation
  - Programmable 200ns to 2μs on-time
  - Constant 400kHz to 600kHz frequency
- Selectable CCM or CCM / DCM
  - CCM / DCM for high efficiency at light-load
  - CCM for constant frequency at light-load
- Programmable hiccup current limit with thermal compensation
- Precision enable and Power Good flag
- Programmable soft-start
- 74-pin 12x14x4mm QFN package

APPLICATIONS

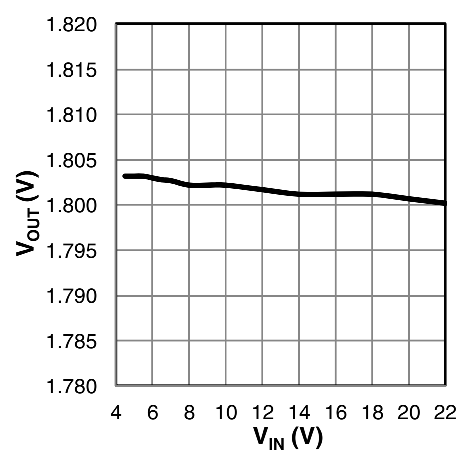
- Networking and communications
- Fast transient Point-of-Loads
- Industrial and medical equipment
- Embedded high power FPGA

Ordering Information – back page

Typical Application



Line Regulation



Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN}....................-0.3V to 25V

V_{CC}....................-0.3V to 6.0V

BST....................-0.3V to 31V(1)

BST-SW....................-0.3V to 6V

SW, ILIM....................-1V to 25V(1, 2)

ALL other pins....................-0.3V to VCC + 0.3V

Storage temperature....................-65°C to +150°C

Junction temperature....................150°C

Power dissipation....................Internally Limited

Lead temperature (Soldering, 10 sec)....................260°C MSL3

ESD Rating (HBM - Human Body Model)....................2kV

Operating Conditions

PV_{IN}....................3V to 22V

V_{IN}....................4.5V to 22V

V_{CC}....................4.5V to 5.5V

SW, ILIM....................-1V to 22V(1)

PGOOD, V_{CC}, T_{ON}, SS, EN, FB....................-0.3V to 5.5V

Switching frequency....................400kHz to 600kHz(3)

Junction temperature range....................-40°C to +125°C

JEDEC51 package thermal resistance, θ_{JA}....................14.5°C/W

Package power dissipation at 25°C....................6.9W

Note 1: No external voltage applied.

Note 2: The SW pin's minimum DC range is -1V, transient is -5V for less than 50ns.

Note 3: Recommended frequency for optimum performance

Electrical Characteristics

Unless otherwise noted: T_J = 25°C, V_{IN} = 12V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7µF. Limits applying over the full operating temperature range are denoted by a "•"

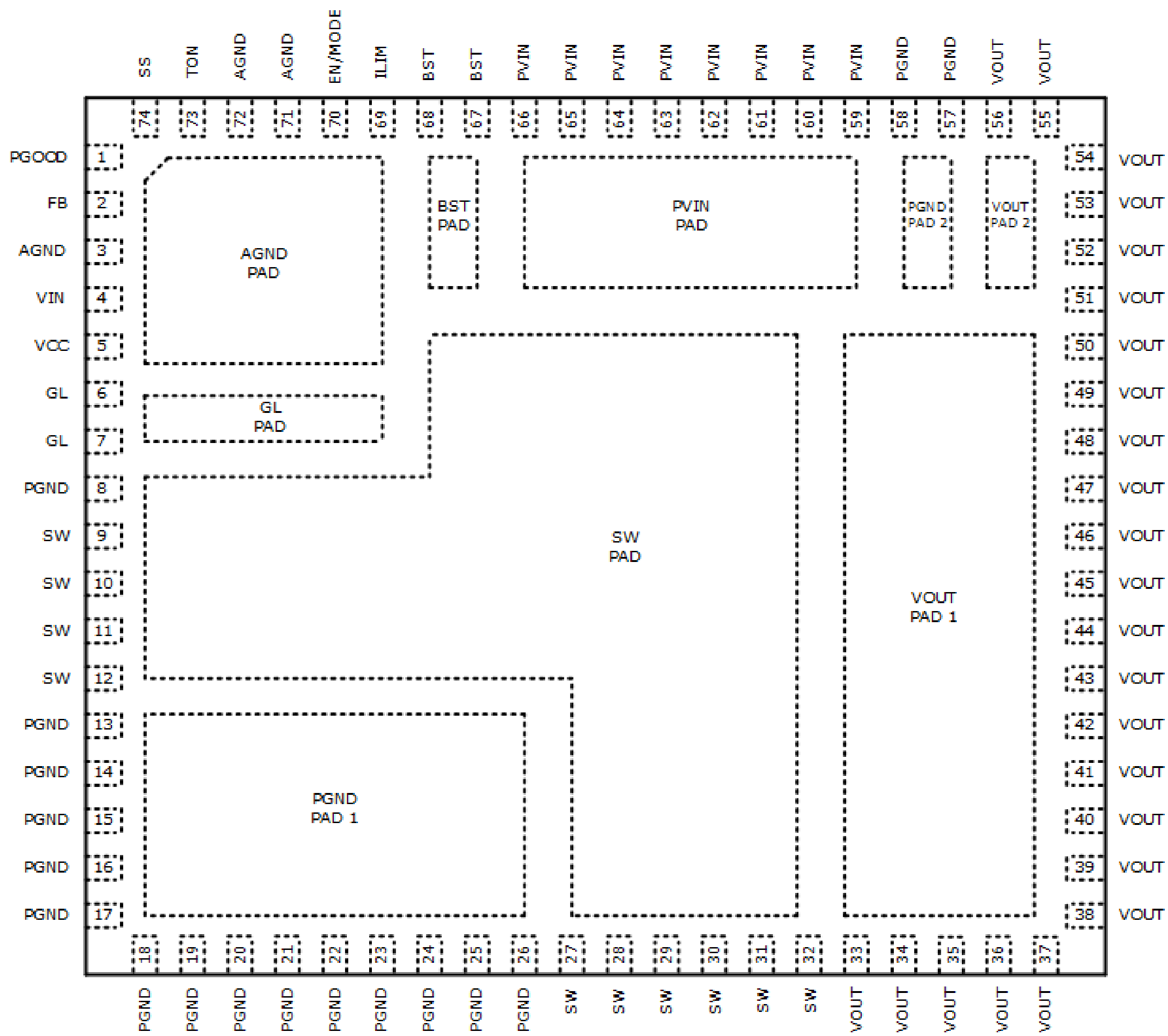
Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range	VCC regulating	•	5		22	V
		VCC tied to VIN	•	4.5		5.5	
I_{VIN}	VIN input supply current	Not switching, V_{IN} = 12V, V_{FB} = 0.7V	•		0.7	1.5	mA
I_{VCC}	VCC quiescent current	Not switching, V_{CC} = V_{IN} = 5V, V_{FB} = 0.7V	•		0.7	1.5	mA
I_{VIN}	VIN input supply current	f = 500kHz, R_{ON} = 61.9kΩ, VFB = 0.58V			21		mA
I_{OFF}	Shutdown current	Enable = 0V, V_{IN} = 12V			1		µA
Enable and Under-Voltage Lock-Out UVLO							
V_{IH_EN}	EN pin rising threshold		•	1.8	1.9	2.0	V
V_{EN_HYS}	EN pin hysteresis				50		mV
V_{IH_EN}	EN pin rising threshold for DCM/CCM operation		•	2.8	3.0	3.1	V
V_{EN_HYS}	EN pin hysteresis				100		mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	VCC UVLO start threshold, rising edge		•	4.00	4.25	4.40	V
	VCC UVLO hysteresis				200		mV
Reference Voltage							
V_{REF}	Reference voltage	V_{IN} = 5V to 22V, VCC regulating		0.597	0.600	0.603	V
		V_{IN} = 4.5V to 5.5V, VCC tied to VIN		0.596	0.600	0.604	V
		V_{IN} = 5V to 22V, VCC regulating V_{IN} = 4.5V to 5.5V, VCC tied to VIN	•	0.594	0.600	0.606	V
	DC line regulation	CCM, closed loop, V_{IN} = 4.5V - 22V, applies to any C_{OUT}			±0.17		%
	DC load regulation	CCM, closed loop, I_{OUT} = 0A - 20A, applies to any C_{OUT}			±0.12		%
Programmable Constant On-Time							
$T_{ON(MIN)}$	Minimum programmable on-time	R_{ON} = 6.98kΩ, V_{IN} = 22V			125		ns
T_{ON2}	On-time 2	R_{ON} = 6.98kΩ, V_{IN} = 12V	•	180	210	240	ns
	f corresponding to on-time 2	V_{OUT} = 1.0V		430	490	575	kHz
T_{ON3}	On-time 3	R_{ON} = 16.2kΩ, V_{IN} = 12V	•	375	445	515	ns
	Minimum off-time		•		250	350	ns
Diode Emulation Mode							
	Zero crossing threshold	DC value measured during test			-1		mV
Soft-start							
	SS charge current		•	-14	-10	-6	µA
	SS discharge current	Fault present	•	1			mA
VCC Linear Regulator							
	VCC output voltage	V_{IN} = 6V to 22V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 5V, I_{LOAD} = 0 to 20mA	•	4.6	4.8		V
Power Good Output							
	Power Good threshold			-10	-7.5	-5	%
	Power Good hysteresis				2	4	%
	Power Good sink current			1			mA
Protection: OCP, OTP, Short-Circuit							
	Hiccup timeout				110		ms
	ILIM pin source current			45	50	55	µA
	ILIM current temperature coefficient				0.4		%/°C
	OCP comparator offset		•	-8	0	+8	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	Current limit blanking	GL rising > 1V			100		ns
	Thermal shutdown threshold[1]	Rising temperature			150		°C
	Thermal hysteresis[1]				15		°C
	VSCTH feedback pin short-circuit threshold	Percent of V_{REF}, short circuit is active after PGOOD is asserted	•	50	60	70	%
Output Power Stage							
R_{DSON}	High-side MOSFET R_{DSON}	I_{DS} = 2A			8.2	10	mΩ
	Low-side MOSFET R_{DSON}				2.8	3.3	mΩ
I_{OUT}	Maximum output current		•	20			A
L	Output inductance			0.45	0.56	0.67	uH
C_{IN}	Input capacitance				1		uF
C_{OUT}	Output capacitance				2.2		uF
C_{BST}	Bootstrap capacitance				0.1		uF

Note 1: Guaranteed by design

Pin Configuration, Top View

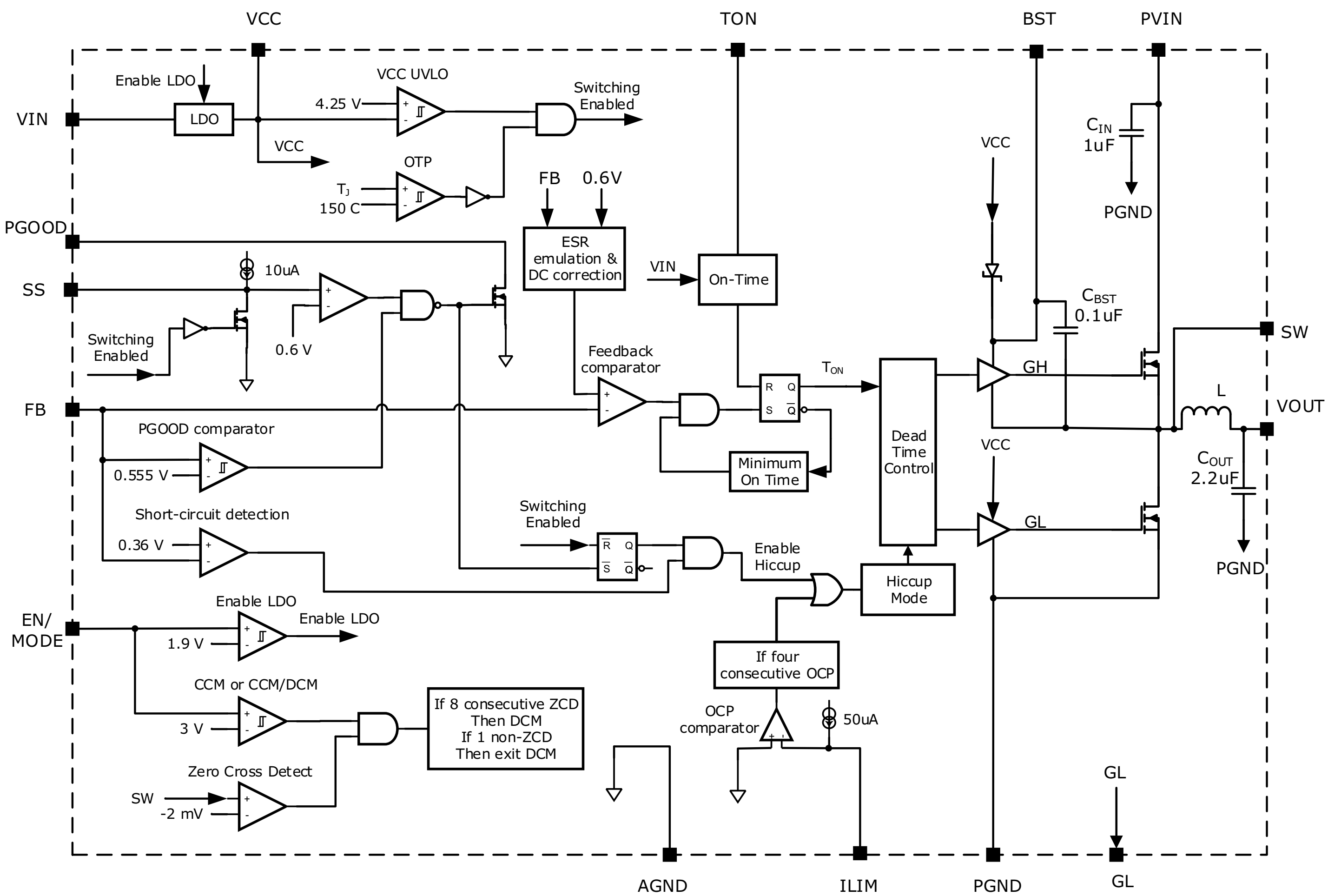


Pin Assignments

Pin No.	Pin Name	Type	Description
1	PGOOD	OD, O	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
2	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and AGND in order to program VOUT.
3, 71, 72, AGND PAD	AGND	A	Analog ground. Control circuitry of the IC is referenced to this pin. It should be connected to PVIN at a single point.
4	VIN	PWR	Controller supply input. Provides power to internal LDO. Connect to PVIN.
5	VCC	PWR	The output of the LDO. Bypass with a 4.7µF capacitor to AGND. For operation from a $5V_{IN}$ rail, VCC should be tied to VIN.
6, 7, GL PAD	GL	O	Driver output for low-side N-channel synchronous MOSFET. It is internally connected to the gate of the MOSFET. Leave these pins floating.
8	PGND	PWR	Controller low-side driver ground. Connect with a short trace to the closest PGND pins or PGND pad.
13-26, 57, 58, PGND PADS	PGND	PWR	Ground of the power stage. Should be connected to the system’s power ground plane.
9-12, 27-32, SW PAD	SW	PWR	Switching node. It is internally connected. Use thermal vias and / or sufficient PCB land area in order to heatsink the low-side FET and the inductor.
33-56, VOUT PADS	VOUT	PWR	Output of the power stage. Place the output filter capacitors as close as possible to these pins.
59-66, PVIN PAD	PVIN	PWR	Power stage input voltage. Place the input filter capacitors as close as possible to these pins.
67, 68, BST PAD	BST	A	Controller high-side driver supply pin. It is internally connected to SW via a 0.1µF bootstrap capacitor. Leave these pins floating.
69	ILIM	A	Over-current protection programming. Connect with a short trace to the SW pins.
70	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V, then the IC will operate in DCM or CCM, depending on load.
73	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
74	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10µA internal source current.

Type: A = Analog, I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram



Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 20A, f = 500kHz, T_A = 25°C. The schematic is from the application information section.

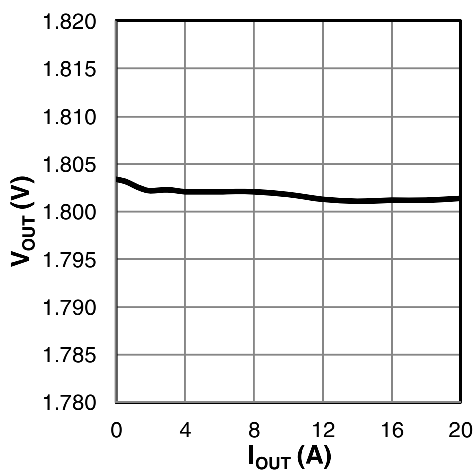


Figure 1: Load Regulation

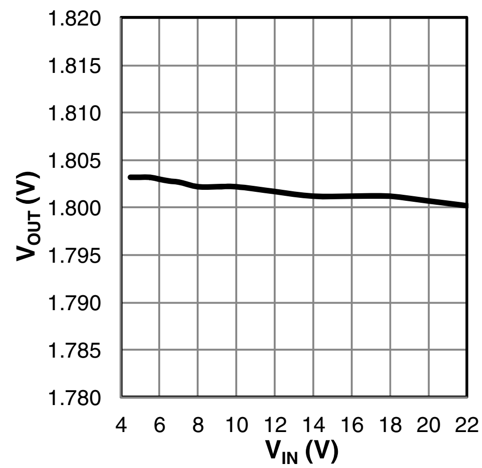


Figure 2: Line regulation

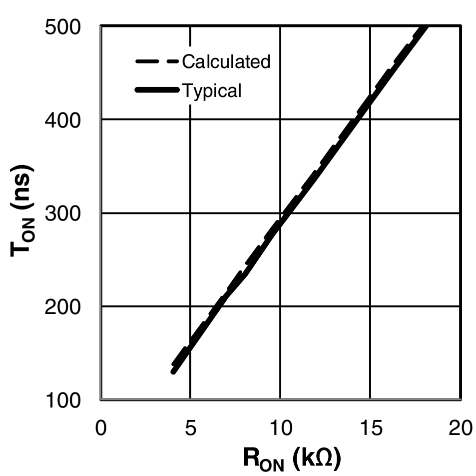


Figure 3: T_{ON} versus R_{ON}

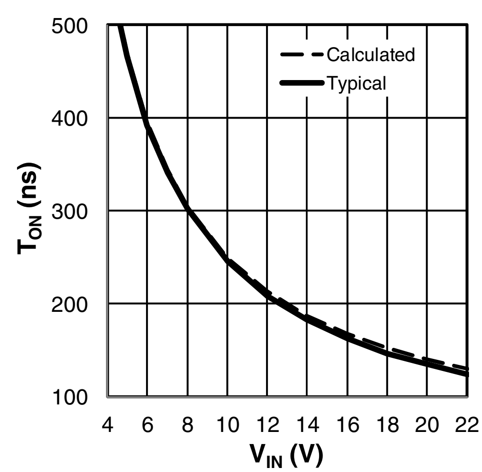


Figure 4: T_{ON} versus V_{IN}, R_{ON}=6.98k

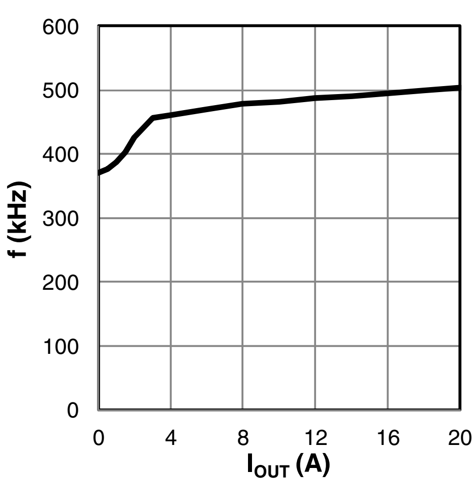


Figure 5: frequency versus I_{OUT}

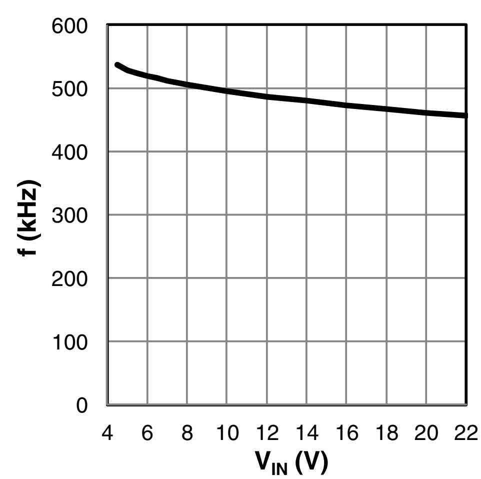


Figure 6: frequency versus V_{IN}

Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 20A, f = 500kHz, T_A = 25°C. The schematic is from the application information section.

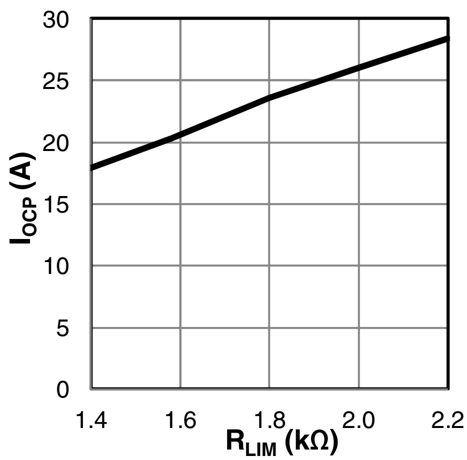


Figure 7: I_{OCP} versus R_{LIM}

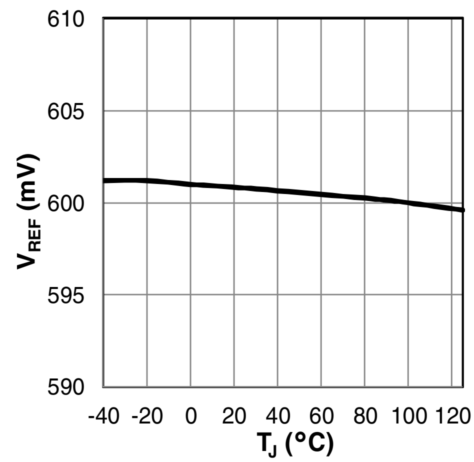


Figure 8: V_{REF} versus temperature

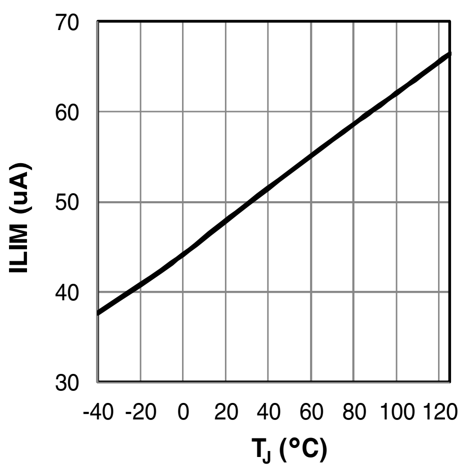


Figure 9: I_{LIM} versus temperature

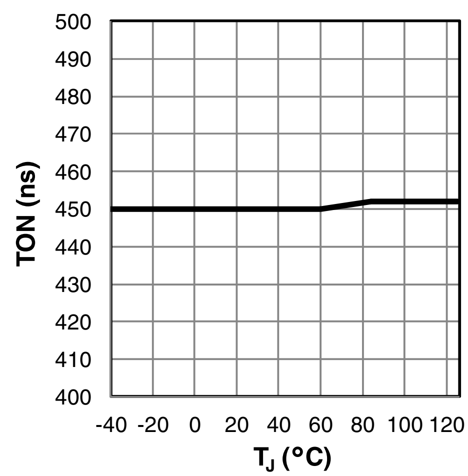


Figure 10: T_{ON} versus temperature, R_{ON}=16.2kΩ

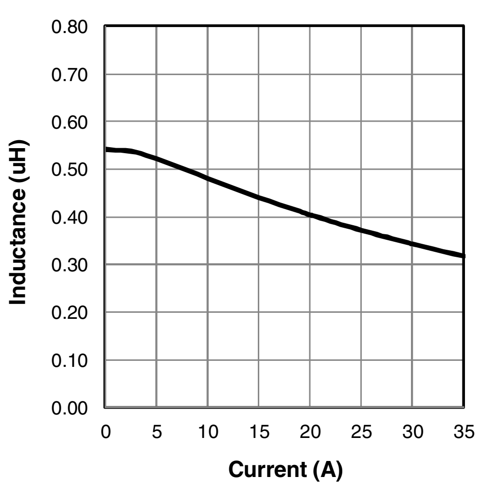


Figure 11: Inductance versus Current

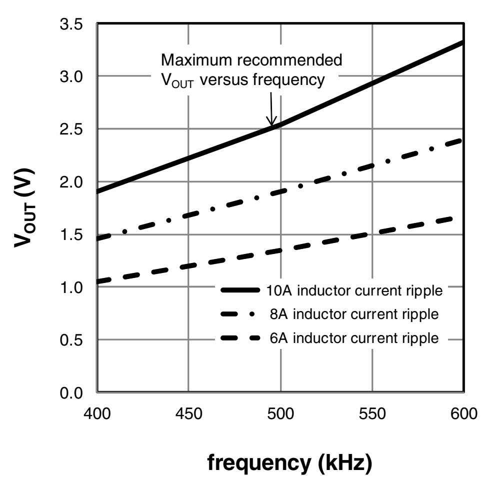


Figure 12: V_{OUT} versus f, V_{IN}=12V

Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 20A, f = 500kHz, T_A = 25°C. The schematic is from the application information section.

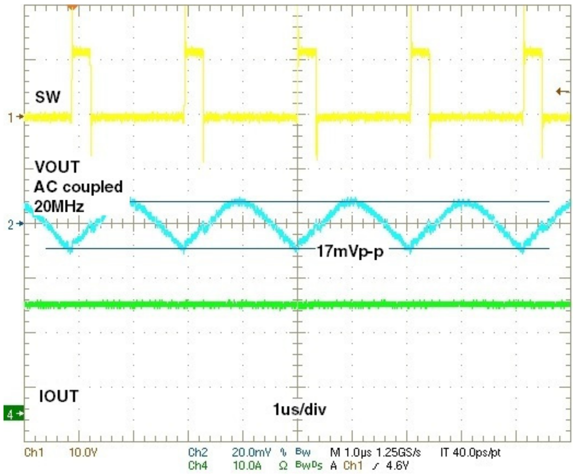


Figure 13: Steady state, CCM, I_{OUT}=20A

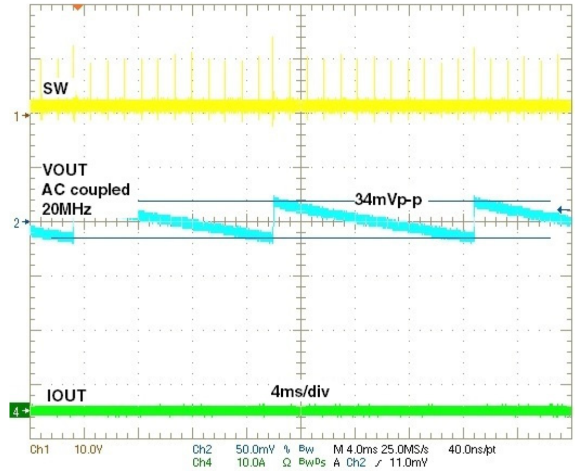


Figure 14: Steady state, DCM, I_{OUT}=0A

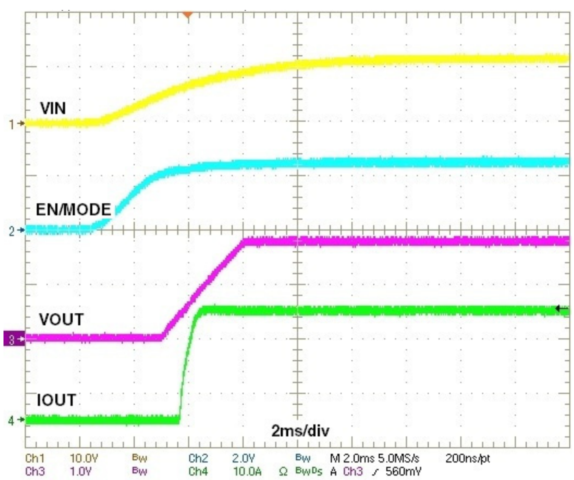


Figure 15: Power up, Forced CCM

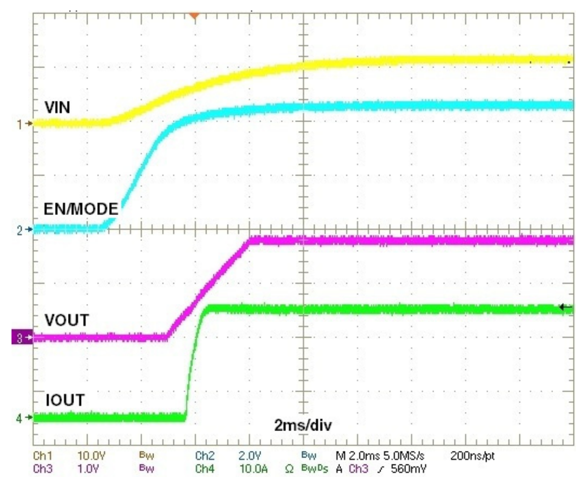


Figure 16: Power up, DCM/CCM

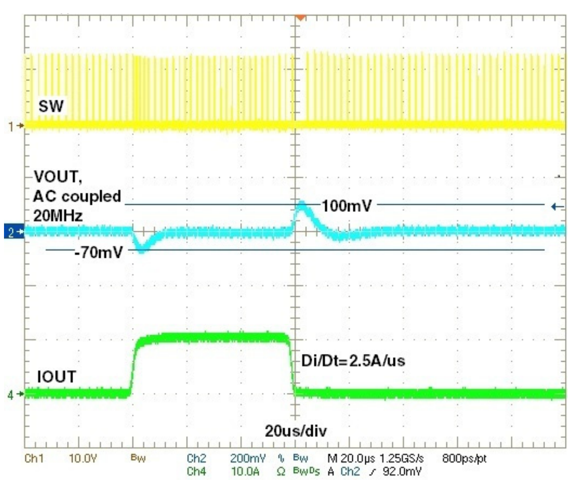


Figure 17: Load step, Forced CCM, 0A-10A-0A

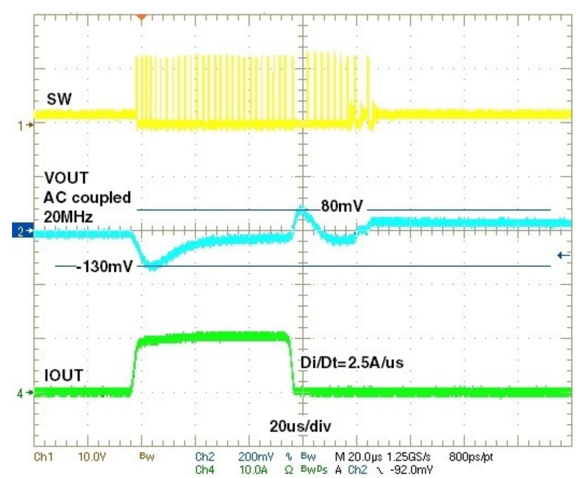


Figure 18: Load step, DCM/CCM, 0A-10A-0A

Efficiency and Package Thermal Derating

Unless otherwise noted: $T_{AMBIENT}$ = 25°C, no air flow, f = 500kHz, the schematic is from the application information section.

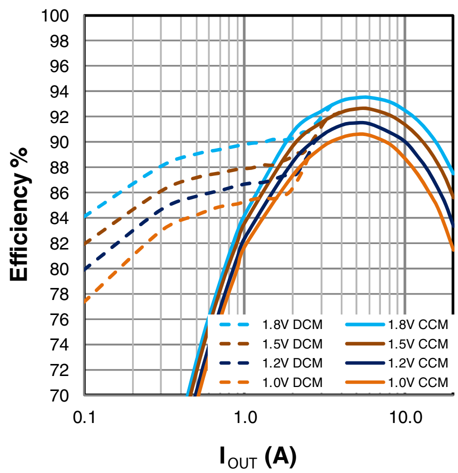


Figure 19: Efficiency, V_{IN}=5V

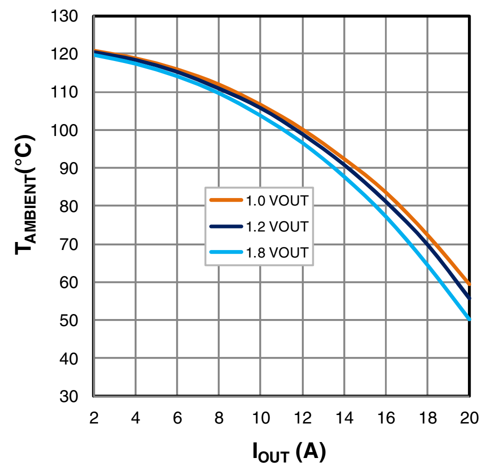


Figure 20: Maximum $T_{AMBIENT}$ vs I_{OUT}, V_{IN}=5V

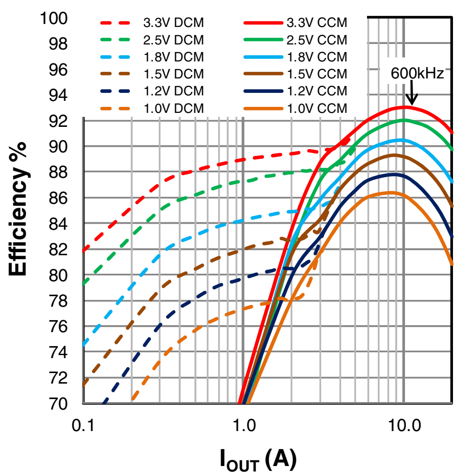


Figure 21: Efficiency, V_{IN}=12V

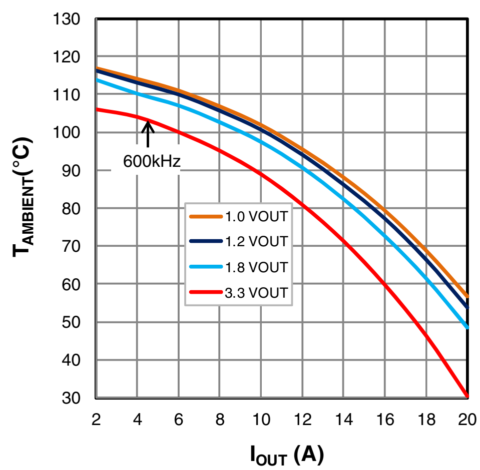


Figure 22: Maximum $T_{AMBIENT}$ vs I_{OUT}, V_{IN}=12V

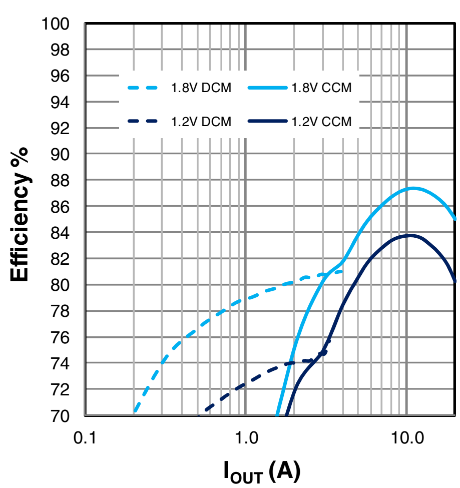


Figure 23: Efficiency, V_{IN}=19.6V

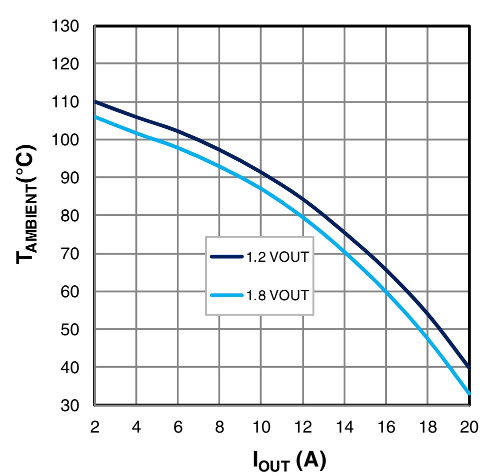


Figure 24: Maximum $T_{AMBIENT}$ vs I_{OUT}, V_{IN}=19.6V

Functional Description

XR79120 is a synchronous step-down, proprietary emulated current-mode Constant On-Time (COT) module. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with the GH signal turning on the high-side (switching) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When V_{FB} drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable / Mode Input (EN/MODE)

The EN/MODE pin accepts a tri-level signal that is used to control turn on and turn off. It also selects between two modes of operation: 'Forced CCM' and 'DCM / CCM'. If EN/MODE is pulled below 1.8V, the module shuts down. A voltage between 2.0V and 2.8V selects the Forced CCM Mode, which will run the module in continuous conduction at all times. A voltage higher than 3.1V selects the DCM / CCM mode, which will run the module in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the module to operate in Forced CCM, a voltage between 2.0V and 2.8V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in Figure 25 can be used to generate the required voltage. Note that at V_{IN} of 5V and 22V, the nominal Zener voltage is 3.8V and 4.7V, respectively. Therefore for V_{IN} in the range of 4.5V to 22V, the circuit shown in Figure 25 will generate the V_{EN} required for Forced CCM.

Selecting the DCM / CCM Mode

In order to set the module operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to EN/MODE. In applications where an external control is not available, the EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4V. If V_{IN} varies over a wide range, the circuit shown in Figure 26 can be used to generate the required voltage.

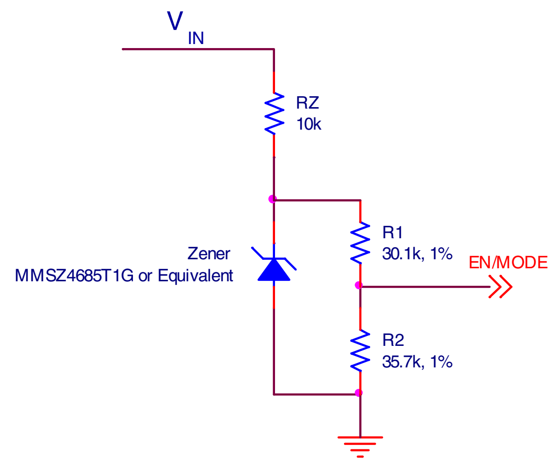


Figure 25: Selecting Forced CCM by deriving EN/MODE from V_{IN}

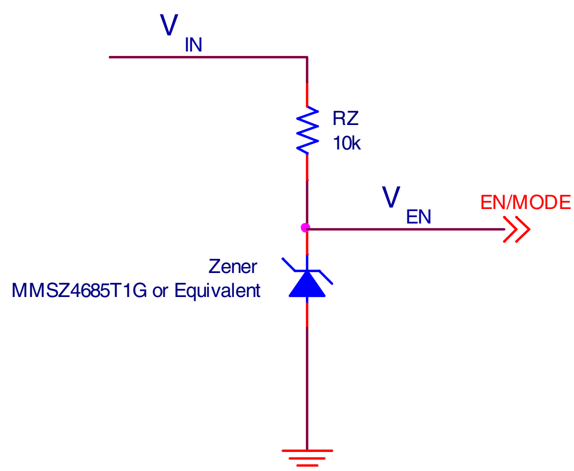


Figure 26: Selecting DCM/CCM by deriving EN/MODE from V_{IN}

Programming the On-Time

The on-time T_{ON} is programmed via resistor R_{ON} according to following equation:

$$R_{ON} = \frac{V_{IN} \times [T_{ON} - (30 \times 10^{-9})]}{3.1 \times 10^{-10}}$$

where T_{ON} is calculated from:

$$T_{ON} = \frac{V_{OUT}}{V_{IN} \times f \times Eff}$$

Where:

f is the desired switching frequency at nominal I_{OUT}

Eff is the module efficiency corresponding to nominal I_{OUT} shown in Figures 19, 21, and 23

Substituting for T_{ON} in the first equation we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{f \times Eff}\right) - [(25 \times 10^{-9}) \times V_{IN}]}{2.85 \times 10^{-10}}$$

Over-Current Protection (OCP)

If load current exceeds the programmed over-current I_{OCP} for four consecutive switching cycles, then the module enters the hiccup mode of operation. In hiccup mode, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The module will remain in hiccup mode until load current is reduced below the programmed I_{OCP} . In order to program the over-current protection, use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

RLIM is resistor value for programming I_{OCP}

I_{OCP} is the over-current threshold to be programmed

RDS is the MOSFET rated on resistance (3.3mΩ)

8mV is the OCP comparator maximum offset

ILIM is the internal current that generates the necessary OCP comparator threshold (use 45µA).

Note that ILIM has a positive temperature coefficient of 0.4%/°C (Figure 9). This is meant to roughly match and compensate for the positive temperature coefficient of the synchronous FET. A graph of typical I_{OCP} versus RLIM is shown in Figure 7.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the module will enter hiccup mode. Hiccup will persist until the short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

Over-Temperature (OTP)

OTP triggers at a nominal die temperature of 150°C. The gates of the switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in the Application Circuit to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1\right)$$

where R2 has a nominal value of 2kΩ.

Programming the Soft-start

Place a capacitor CSS between the SS and AGND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance CSS from the following equation:

$$CSS = TSS \times \left(\frac{10\mu A}{0.6V}\right)$$

Feed-Forward Capacitor (CFF)

A feed-forward capacitor (C_{FF}) may be necessary depending on the Equivalent Series Resistance (ESR) of C_{OUT}. If only ceramic output capacitors are used for C_{OUT}, then a C_{FF} is necessary. Calculate C_{FF} from:

$$C_{FF} = \frac{1}{2 \times \pi \times R1 \times 7 \times f_{LC}}$$

Where:

R1 is the resistor that C_{FF} is placed in parallel with

f_{LC} is the frequency of output filter double-pole

f_{LC} must be less than 13kHz when using ceramic C_{OUT}. If necessary, increase C_{OUT} in order to meet this constraint.

When using capacitors with higher ESR, such as the PANASONIC TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of output filter LC double-pole f_{LC} should be less than 10kHz.

2. The frequency of ESR Zero $f_{Zero,ESR}$ should be at least three times larger than f_{LC}.

Note that if $f_{Zero,ESR}$ is less than $5xf_{LC}$, then it is recommended to set the f_{LC} at less than 2kHz. C_{FF} is still not required.

Maximum Allowable Voltage Ripple at FB Pin

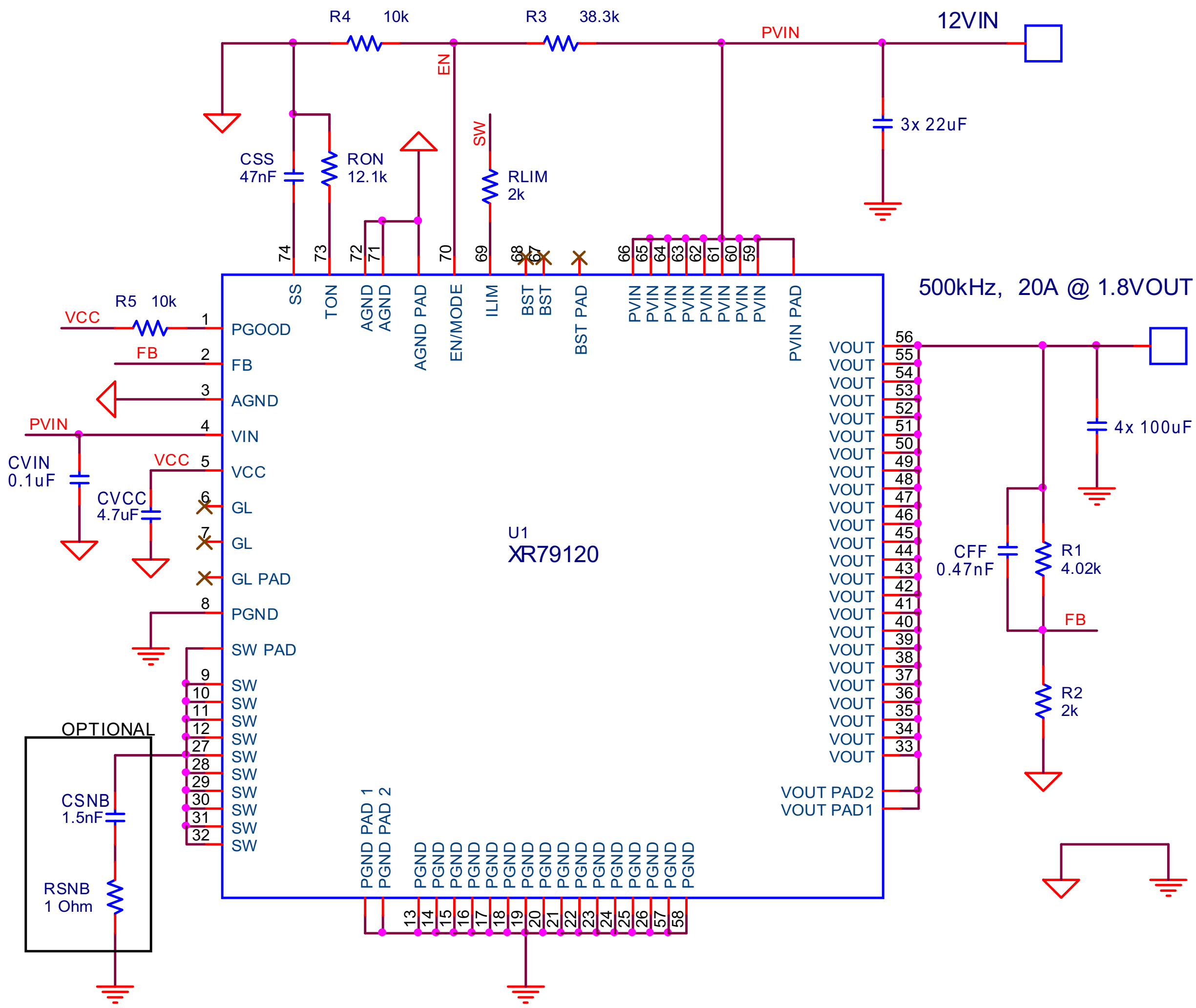
Note that the steady-state voltage ripple at feedback pin FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the module to function correctly. If $V_{FB, RIPPLE}$ is larger than 50mV, the C_{OUT} should be increased as necessary in order to keep the $V_{FB, RIPPLE}$ below 50mV.

Poor PCB layout can cause FET switching noise at the output and may couple to the FB pin via C_{FF}. Excessive noise at FB will cause poor load regulation. To solve this problem, place a resistor R_{FF} in series with C_{FF}. An R_{FF} value up to 2% of R1 is acceptable.

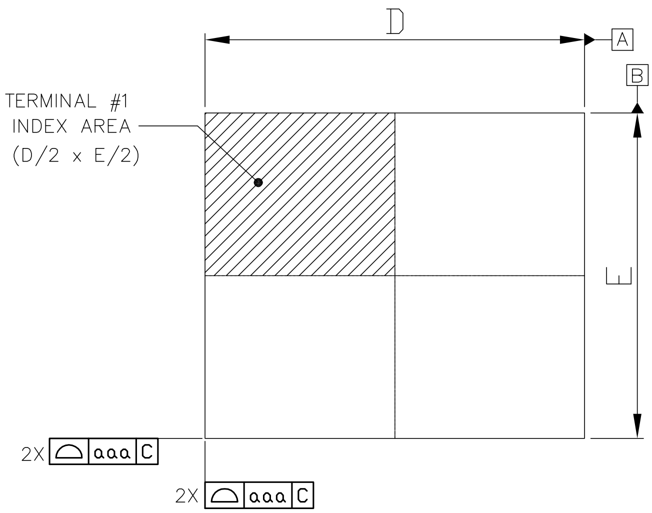
Maximum Recommended VOUT versus Frequency

V_{OUT} versus frequency curves corresponding to inductor current ripple ΔIL of 10A, 8A and 6A are plotted in Figure 12. These curves show the relationship between V_{OUT}, f and ΔIL for V_{IN} = 12V. As an example, for operating conditions of V_{IN} = 12V, V_{OUT} = 1.5V and f = 500kHz, the current ripple is about 6.5A. Note that maximum recommended peak-to-peak ΔIL is 10A. Therefore the maximum permissible V_{OUT} versus f corresponds to the top curve in Figure 12. For example, with V_{IN} = 12V and f = 500kHz maximum, V_{OUT} is 2.5V.

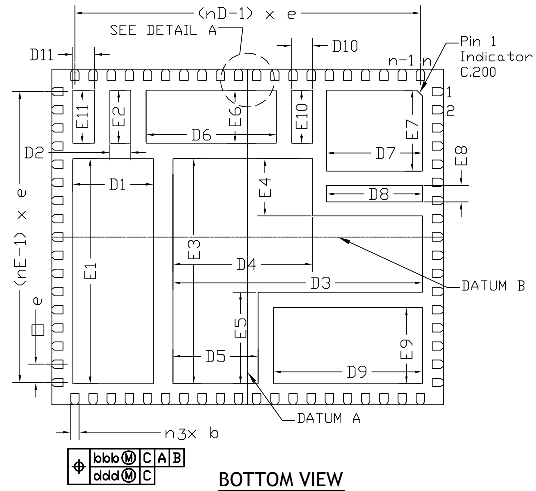
Application Circuit



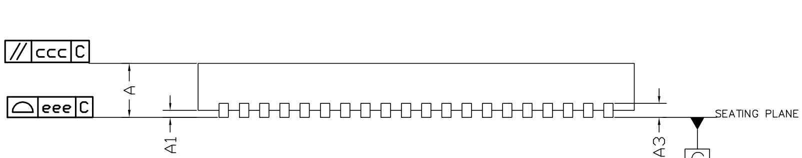
Mechanical Dimensions



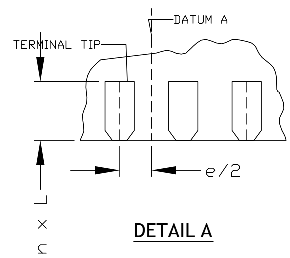
TOP VIEW



BOTTOM VIEW



SIDE VIEW

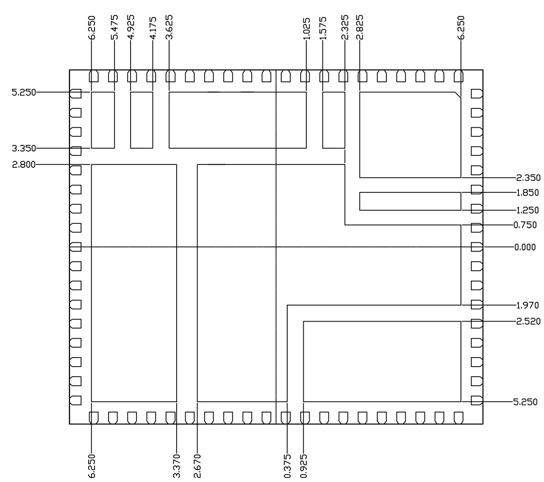


DETAIL A

PACKAGE	74L 14x12 SIP-QFN		
REF.	MIN.	NOM.	MAX.
A	3.90	4.00	4.10
b	0.25	0.30	0.35
L	0.30	0.40	0.50
D	14.00 BSC		
D1	2.78	2.88	2.98
D2	0.65	0.75	0.85
D3	8.82	8.92	9.02
D4	4.895	4.995	5.005
D5	2.945	3.045	3.145
D6	4.55	4.65	4.75
D7	3.325	3.425	3.525
D8	3.325	3.425	3.525
D9	5.225	5.325	5.425
D10	0.65	0.75	0.85
D11	0.675	0.775	0.875
E	12.00 BSC		
E1	7.95	8.05	8.15
E2	1.80	1.90	2.00
E3	7.95	8.05	8.15
E4	1.95	2.05	2.15
E5	3.18	3.28	3.38
E6	1.80	1.90	2.00
E7	2.80	2.90	3.00
E8	0.50	0.60	0.70
E9	2.63	2.73	2.83
E10	1.80	1.90	2.00
E11	1.80	1.90	2.00
e	0.65 BSC		
n	74		
nD	20		
nE	17		

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A1	0	0.02	0.05	
A3	0.20 REF.			
TOLERANCES OF FORM AND POSITION				
aaa	0.10			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			

TERMINAL DETAILS



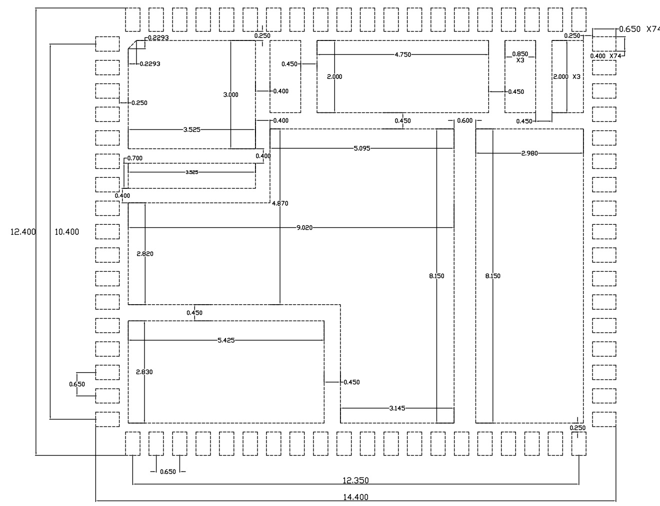
TERMINAL AND PAD EDGE DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

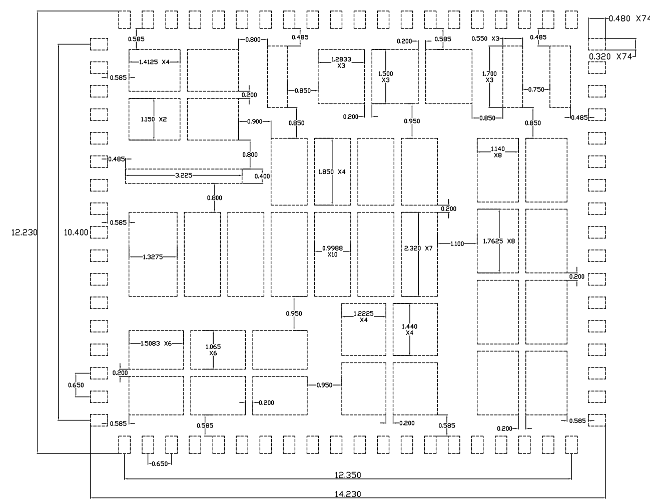
Drawing No.: POD-00000059

Revision: B

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD-00000059

Revision: B

Ordering Information[1]

Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free
XR79120EL-F	-40°C to +125°C	12 x14mm QFN	Tray	Yes[2]
XR79120EVB	XR79120 Evaluation Board			

NOTES:
1. Refer to www.maxlinear.com/XR79120 for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	March 2015	ECN 1512-02
1B	June 2018	Update to MaxLinear logo. Update format and Ordering Information.
1C	November 2019	Correct block diagram by changing the input gate that connects to the Hiccup Mode block from an AND gate to an OR gate.

Corporate Headquarters:
5966 La Place Court
Suite 100
Carlsbad, CA 92008
Tel.:+1 (760) 692-0711
Fax: +1 (760) 444-8598
www.maxlinear.com