



## M2058/M2059 Series SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT OSCILLATOR

### FEATURES

LVPECL/LVDS Differential Output  
RMS Phase Jitter < 100 fs, 12 kHz to 20 MHz  
(156.25 MHz, PECL output)  
Low Phase Noise  
3<sup>rd</sup> Overtone crystal technology  
Compliant to RoHS directive

### APPLICATIONS

10 Gigabit Ethernet switches/routers  
Network Interface

### Ordering Information:

Product Family (Supply Voltage Option)	Temperature Range		Stability *		Enable/Disable		Logic Type		Package/Lead Configuration		Frequency
	Code	Value	Code	Value	Code	Value	Code	Value	Code	Value	
<b>M2058</b> (3.3V)	<b>2</b>	-40 °C to +85 °C	<b>3</b>	±100 ppm	<b>B</b>	Enable High (pad 1)	<b>P</b>	LVPECL	<b>N</b>	Leadless	XXX.XXXX MHz
<b>M2059</b> (2.5V)	<b>6</b>	-20 °C to +70 °C	<b>4</b>	±50 ppm	<b>U</b>	No Enable/Disable	<b>L</b>	LVDS			
			<b>6</b>	±25 ppm	<b>G</b>	Enable High (pad 2)					
			<b>8</b>	±20 ppm							

Example: M205824BPN 156.2500 MHz

<b>M2058</b>	<b>2</b>	<b>4</b>	<b>B</b>	<b>P</b>	<b>N</b>	<b>156.2500 MHz</b>
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\* Stability includes initial tolerance @ +25°C, deviation over operating temperature, variations to supply voltage, load, vibration and shock.

### LVPECL Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F <sub>O</sub>	25		220	MHz	
<b>Frequency Stability</b>						
Frequency Stability	ΔF/F	See ordering information				
Aging		-5		+5	ppm	1 <sup>st</sup> year
<b>RF Output</b>						
Output Type		LVPECL Compatible				
Output Load		50 Ω to (V <sub>CC</sub> -2.0) V <sub>DC</sub>				
Symmetry (duty cycle)	V <sub>OH</sub>	45		55	%	Ref. to 50% of waveform
Logic Level "1"	V <sub>OH</sub>	V <sub>CC</sub> -1.025		V <sub>CC</sub> -0.880	V	
Logic Level "0"	T <sub>DC</sub>	V <sub>CC</sub> -1.810		V <sub>CC</sub> -1.620	V	
Rise/Fall Time	T <sub>R</sub> /T <sub>F</sub>		0.2	0.4	ns	20% to 80% of waveform
Start-up Time	T <sub>SU</sub>			10	ms	T <sub>ambient</sub> = +25°C
Enable Logic		70% V <sub>CC</sub> or N/C			V	Pad 1 or Pad 2: Output Enabled
Disable Logic				30% V <sub>CC</sub>	V	Pad 1 or Pad 2: Output Disabled to high-Z
<b>Supply Voltage &amp; Power Consumption</b>						
Operating Voltage	V <sub>CC</sub>	3.135	3.300	3.465	V	
Supply Current	I <sub>CC</sub>			75	mA	
<b>Other Parameters</b>						
Phase Jitter (RMS)	Φ <sub>J</sub>			0.100	ps	12 KHz to 20 MHz 156.25 MHz



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### LVDS Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Frequency of Operation	$F_O$	25		220	MHz		
<b>Frequency Stability</b>							
Frequency Stability	$\Delta F/F$	See ordering information					
Aging		-5		+5	ppm	1 <sup>st</sup> year	
<b>RF Output</b>							
Output Type		LVDS Compatible					
Output Load		100 $\Omega$ Differential			V		
Symmetry (duty cycle)	$V_{OH}$	45		55	%	Ref. to 50% of waveform	
Differential Output Voltage	$V_{DIFF}$	250	350	450	mV	peak-to-peak differential output voltage	
Output Offset Voltage	$V_{OS}$	1.125	1.250	1.375	V		
Rise/Fall Time	$T_R/T_F$		0.2	0.4	ns	20% to 80% of waveform	
Start-up Time	$T_{SU}$			10	ms	$T_{ambient} = +25^\circ C$	
Enable Logic		70% $V_{CC}$ or N/C			V	Pad 1 or Pad 2: Output Enabled	
Disable Logic				30% $V_{CC}$	V	Pad 1 or Pad 2: Output Disabled to high-Z	
<b>Supply Voltage &amp; Power Consumption</b>							
Operating Voltage	$V_{CC}$	3.135	3.300	3.465	V		
Supply Current	$I_{CC}$			40	mA		
<b>Other Parameters</b>							
Phase Jitter (RMS)	$\Phi_J$			0.150	ps	12 KHz to 20 MHz 156.25 MHz	

### Environmental & Packaging Requirements:

Storage Temperature	-55°C to 125°C
Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Vibration	Per MIL-STD-202, Method 204D, Condition D
Aging	+85°C $\pm 3^\circ C$ , 720H (No BIAS)
Humidity	+40°C $\pm 2^\circ C$ X90~95%, 96H (NO BIAS)
Thermal Cycle	Per MIL-STD-883, Method 1011, Condition A
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 <sup>-8</sup> atm cc/s of Helium)
Moisture Sensitivity Level	MSL1
Solderability	Per EIAJ-STD-002, Method 208
Max. Soldering Conditions	See solder profile, Figure 1
Pad Termination	Gold, 1 $\mu m$ maximum thickness
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.

### Marking, Pin Out:



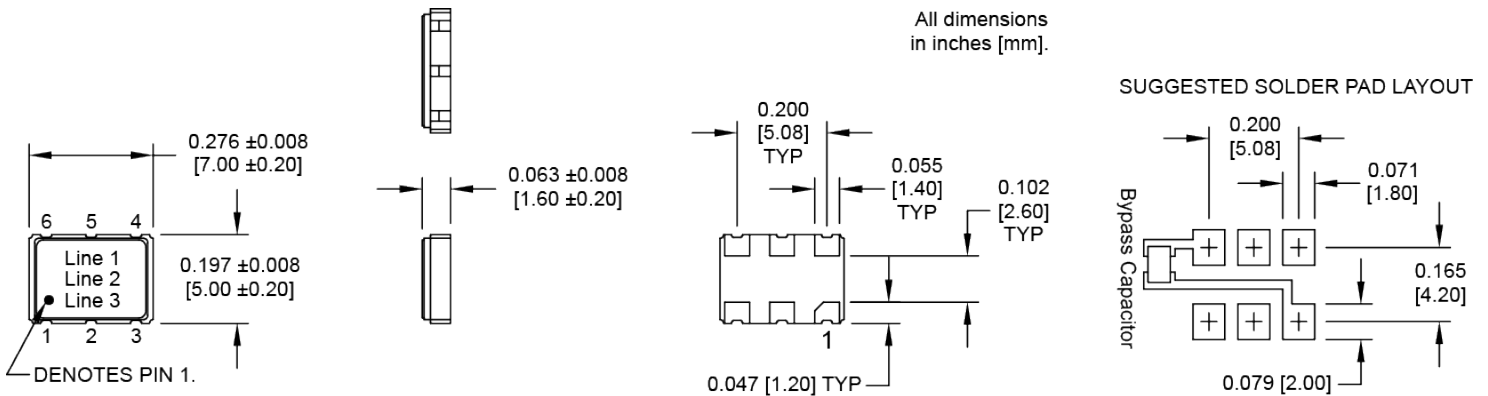
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Pad	Function
1	Enable/Disable or N/C
2	Enable/Disable or N/C
3	Ground
4	Output
5	Complementary Output
6	+V <sub>CC</sub>

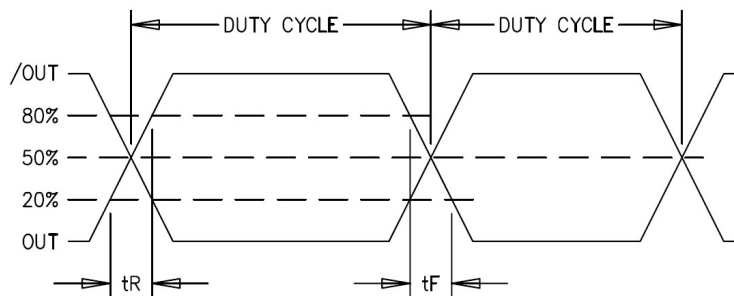
Part Marking	
Line 1	M2058/M2059
Line 2	FFFMMMM
Line 3	M yy ww vv

Legend	
M	MtronPTI
F	Frequency
yy	Year
ww	Work Week
vv	Factory code

### Dimensions:



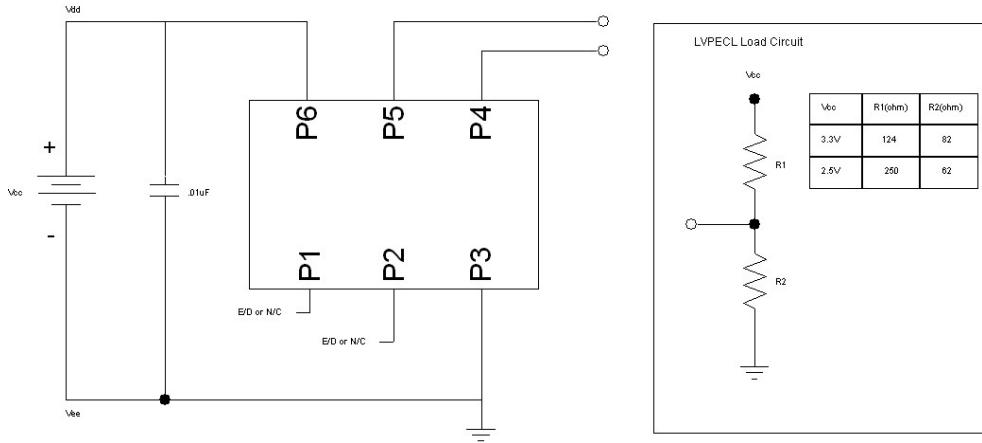
### Output Waveform:



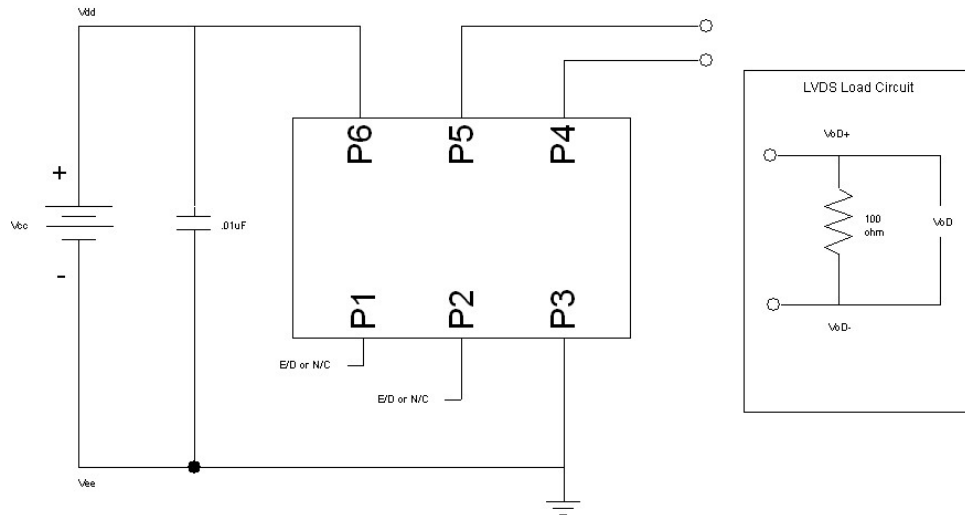


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**Typical LVPECL Test Circuit & Load Circuit Diagrams:**



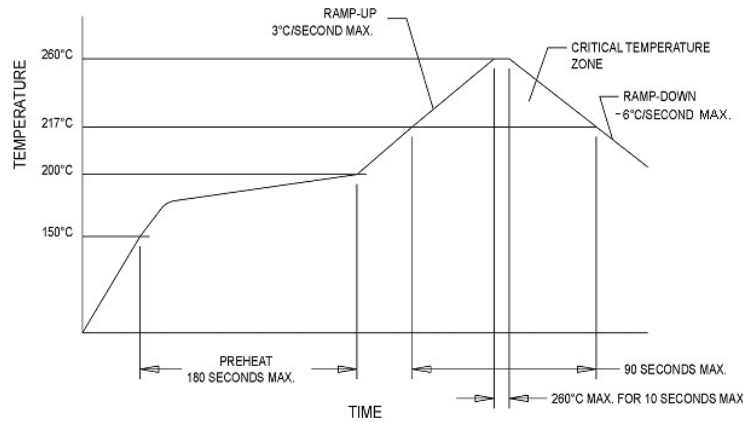
**Typical LVDS Test Circuit & Load Circuit Diagrams:**





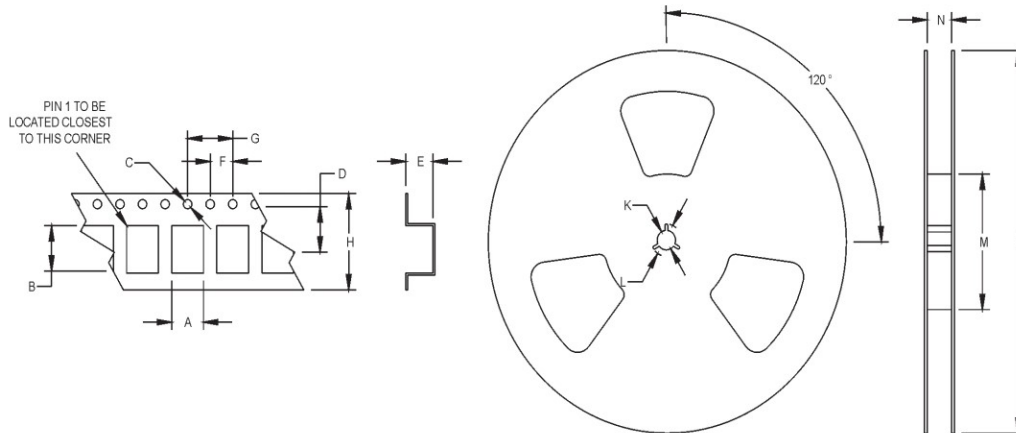
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### Soldering Conditions:



### Tape and Reel Specifications:

All units in mm

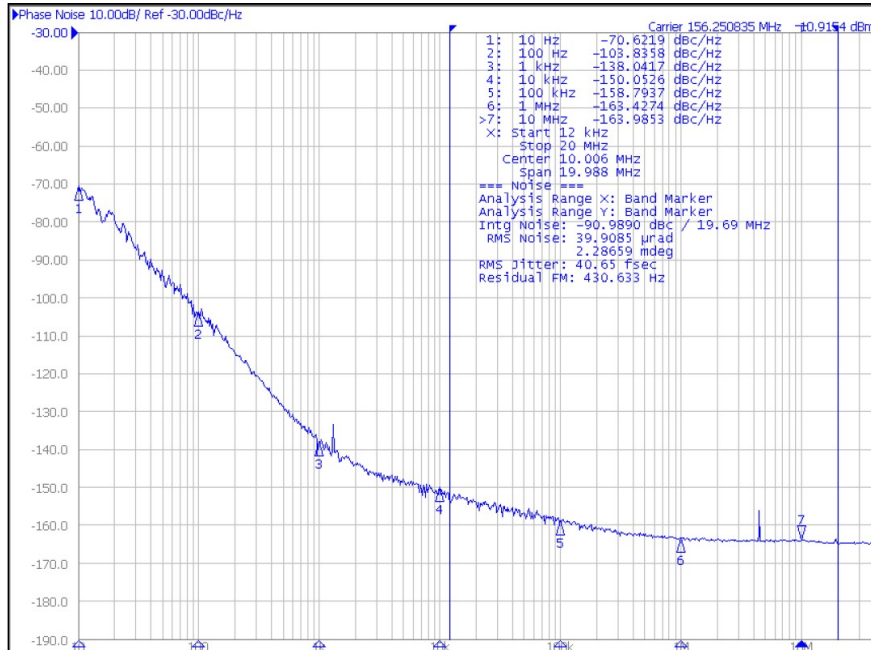


Tape and Reel Specifications											
A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80

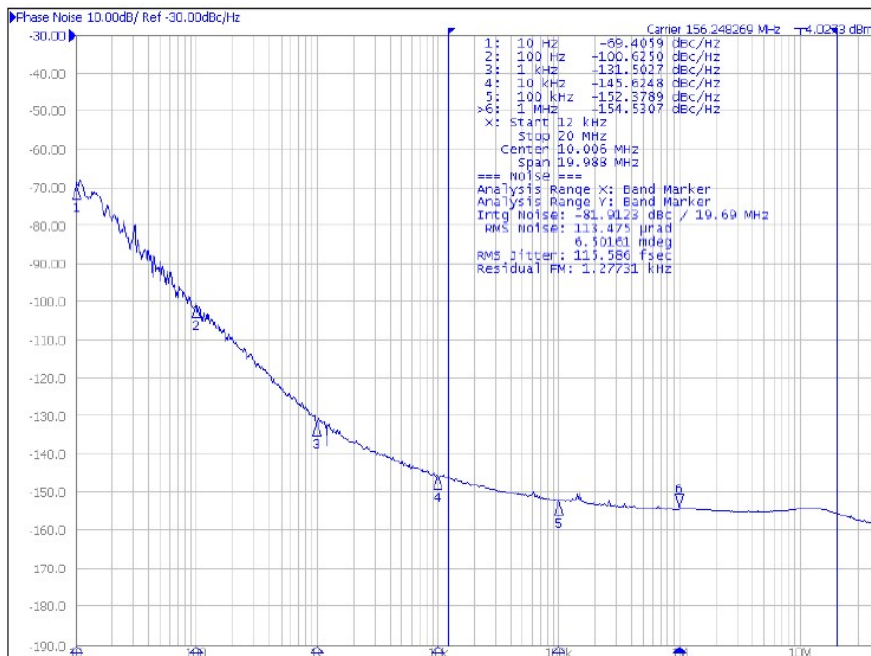


## M2058/M2059 Series SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT OSCILLATOR

### LVPECL Phase Noise Plot:



### LVDS Phase Noise Plot:



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