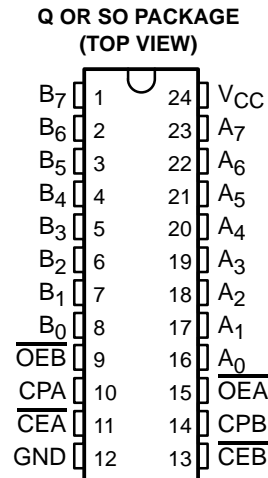


- **Function, Pinout, and Drive Compatible With FCT, F Logic, and AM2952**
- **Reduced  $V_{OH}$  (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **64-mA Output Sink Current**  
**32-mA Output Source Current**



### description

The CY29FCT52T has two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Separate clock, clock enable, and 3-state output-enable signals are provided for each register. Both A outputs and B outputs are specified to sink 64 mA.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### PIN DESCRIPTION

NAME	DESCRIPTION
A	A register inputs or B register outputs
B	B register inputs or A register outputs
CPA	Clock for the A register. When $\overline{CEA}$ is low, data enters the A register on the low-to-high transition of the CPA signal.
$\overline{CEA}$	Clock enable for the A register. When $\overline{CEA}$ is low, data enters the A register on the low-to-high transition of the CPA signal. When $\overline{CEA}$ is high, the A register holds its contents, regardless of CPA signal transitions.
$\overline{OEA}$	Output enable for the A register. When $\overline{OEA}$ is low, the A register outputs are enabled onto the B lines. When $\overline{OEA}$ is high, the A outputs are in the high-impedance state.
CPB	Clock for the B register. When $\overline{CEB}$ is low, data enters the B register on the low-to-high transition of the CPB signal.
$\overline{CEB}$	Clock enable for the B register. When $\overline{CEB}$ is low, data enters the B register on the low-to-high transition of the CPB signal. When $\overline{CEB}$ is high, the B register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	Output enable for the B register. When $\overline{OEB}$ is low, the B register outputs are enabled onto the A lines. When $\overline{OEB}$ is high, the B outputs are in the high-impedance state.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# CY29FCT52T

## 8-BIT REGISTERED TRANSCEIVER

SCCS010A – MAY 1994 – REVISED OCTOBER 2001

### ORDERING INFORMATION

TA	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	6.3	CY29FCT52CTQCT	29FCT52C
	SOIC – SO	Tube	6.3	CY29FCT52CTSOC	29FCT52C
		Tape and reel	6.3	CY29FCT52CTSOCT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### Function Tables

FUNCTION TABLE

INPUTS			INTERNAL Q	FUNCTION
D	CP	CE		
X	X	H	NC	Hold data
L		L	L	Load data
H		L	H	

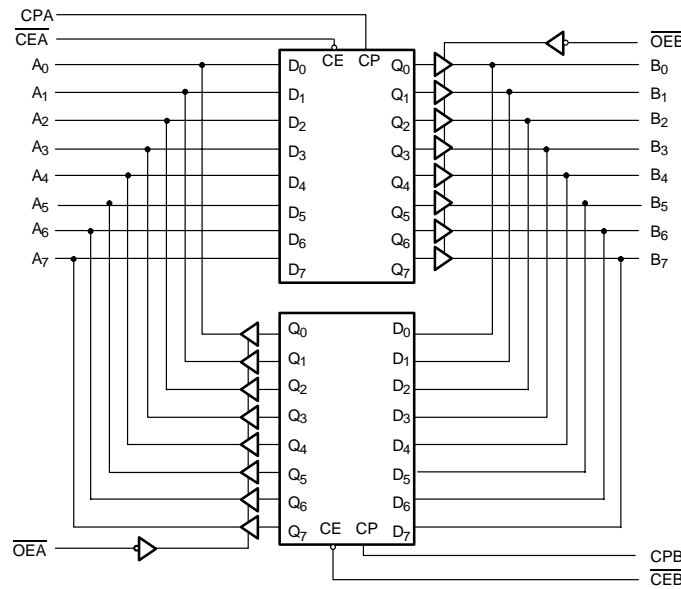
H = High logic level, L = Low logic level, X = Don't care, NC = No change

OUTPUT CONTROL

$\overline{OE}$	INTERNAL Q	Y OUTPUTS	FUNCTION
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H = High logic level, L = Low logic level, X = Don't care, Z = High impedance (off) state.

### logic diagram



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**absolute maximum rating over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	61°C/W
SO package .....	46°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to 135°C
Storage temperature range, $T_{Stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–32	mA
$I_{OL}$ Low-level output current			64	mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

# CY29FCT52T

## 8-BIT REGISTERED TRANSCEIVER

SCCS010A – MAY 1994 – REVISED OCTOBER 2001

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT		
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{IN} = -18\text{ mA}$	-0.7	-1.2		V		
$V_{OH}$	$V_{CC} = 4.75\text{ V}$	$I_{OH} = -32\text{ mA}$	2			V		
		$I_{OH} = -15\text{ mA}$	2.4	3.3				
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 64\text{ mA}$	0.3	0.55		V		
$V_H$	All inputs		0.2			V		
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = V_{CC}$			5	$\mu\text{A}$		
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 2.7\text{ V}$			$\pm 1$	$\mu\text{A}$		
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 0.5\text{ V}$			$\pm 1$	$\mu\text{A}$		
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0\text{ V}$	-60	-120	-225	mA		
$I_{off}$	$V_{CC} = 0\text{ V}$ ,	$V_{OUT} = 4.5\text{ V}$			$\pm 1$	$\mu\text{A}$		
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ , $V_{IN} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.1	0.2		mA		
$\Delta I_{CC}$	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 3.4\text{ V}^\S$ , $f_1 = 0$ , Outputs open		0.5	2		mA		
$I_{CCD}^\parallel$	$V_{CC} = 5.25\text{ V}$ , One input switching at 50% duty cycle, Outputs open, OEA or OEB = GND, $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.06	0.12		mA/MHz		
$I_C^\#$	$V_{CC} = 5.25\text{ V}$ , $f_0 = 10\text{ MHz}$ , Outputs open, OEA or OEB = GND	One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.7	1.4	mA	
			$V_{IN} = 3.4\text{ V}$ or GND		1.2	3.4		
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$		1.6	3.2		
			$V_{IN} = 3.4\text{ V}$ or GND		3.9	12.2		
$C_i$			5	10		pF		
$C_o$			9	12		pF		

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_C$  formula.



**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER		MIN	MAX	UNIT
$t_w$	Pulse duration, clock	3		ns
$t_{su}$	Setup time, before CPA $\uparrow$ or CPB $\uparrow$	Data	2.5	ns
		$\overline{CEA}$ or $\overline{CEB}$	3	
$t_h$	Hold time, after CPA $\uparrow$ or CPB $\uparrow$	Data	1.5	ns
		$\overline{CEA}$ or $\overline{CEB}$	2	

**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{PLH}$	CPA, CPB	A, B	2	6.3	ns
$t_{PHL}$			2	6.3	
$t_{PZH}$	$\overline{OEA}$ or $\overline{OEB}$	A or B	1.5	7	ns
$t_{PZL}$			1.5	7	
$t_{PHZ}$	$\overline{OEA}$ or $\overline{OEB}$	A or B	1.5	6.5	ns
$t_{PLZ}$			1.5	6.5	

# CY29FCT52T

## 8-BIT REGISTERED TRANSCEIVER

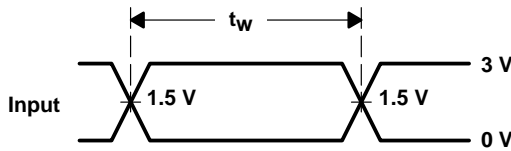
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### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY29FCT52CTQCT	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	29FCT52C	<a href="#">Samples</a>
CY29FCT52CTSOC	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	29FCT52C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY29FCT52CTQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY29FCT52CTQCT	SSOP	DBQ	24	2500	853.0	449.0	35.0

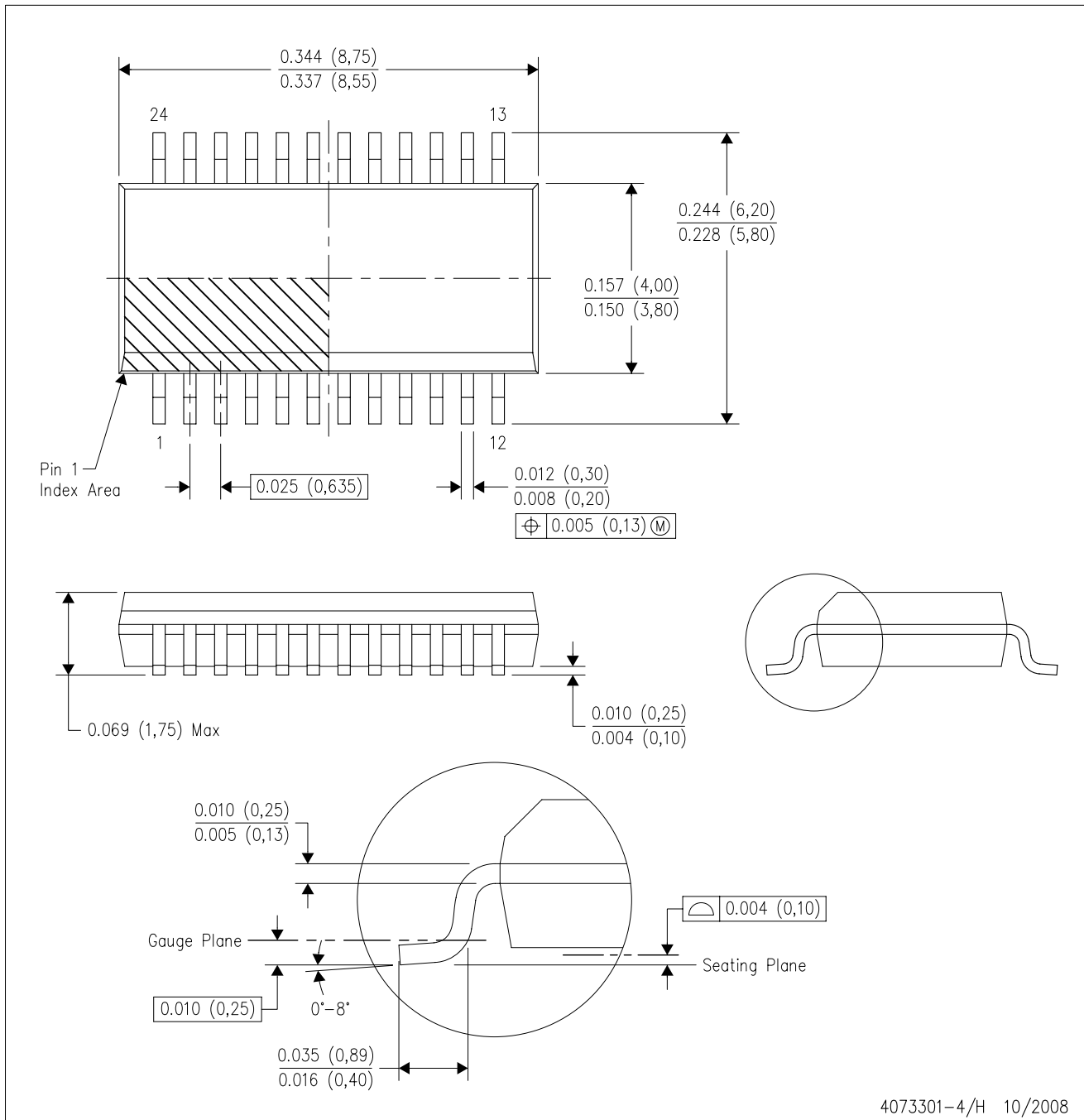
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY29FCT52CTSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AE.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

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