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MAX22000

Industrial Configurable Analog I/O

General Description

The MAX22000 is an industrial-grade configurable analog input/output device that can be configured on-the-fly in software as a voltage input or output, or current input or output. Additional inputs are available to measure other analog signals.

The device offers an 18-bit DAC with fast settling time, as well as a 24-bit delta-sigma ADC. The ADC and DAC can individually choose between an internal or an external reference.

The MAX22000 supports the ADC with a low-noise programmable gain amplifier (PGA), with high-voltage and low-voltage input ranges to support RTD and thermocouple measurements. Additional auxiliary inputs are provided to measure cold junction temperatures on-board.

The MAX22000 communicates through a high speed 20MHz SPI bus for all configuration and management information, as well as for conversion results. An optional 8-bit CRC enhances the reliability of the SPI interface, protecting against all 8-bit bursts and double-bit errors.

The MAX22000 operates from 2.7V to 3.6V analog and digital supplies and up to ±24V high-voltage supplies. The device is available in a 64-pin LGA package and operates over the -40°C to +125°C industrial temperature range.

Applications

- Distributed Control Systems
- Process Control
- Programmable Logic Controllers (PLC)
- Programmable Automation Controllers (PAC)

Benefits and Features

- Accuracy
  - Analog Output Voltage or Current Mode:
    - 0.02% FSR Accuracy, Room Temp
    - 0.1% FSR Accuracy, ±50°C Temp Variation
  - 5ppm/°C Internal Reference
- Flexibility
  - 6 Analog Inputs/1 Analog Output, Software Configurable for Voltage and Current Mode
  - Two Auxiliary ADC Inputs for Cold Junction Measurements
  - RTD Input Mode in 2, 3, or 4-Wire Configurations
  - Thermocouple Input Mode
  - ±12.5V Input/Output Voltage Range
  - ±25mA or ±2.5mA Output Current Range
  - ±25V, ±2.5V, ±500mV, ±250mV, and ±125mV PGA Input Voltage Ranges
  - +24V Field Supply for Current Loop
  - Optional External Reference for ADC and/or DAC
  - Six GPIOs
  - 20MHz SPI Interface
- Robustness
  - ±36V Protection on All Analog I/O Ports
  - Overcurrrent Protection
  - Thermal Shutdown
  - Undervoltage Interrupt on All High Voltage Supplies
  - CRC Detection
  - Open Detection on All Analog Inputs
  - 1kV HBM Protection on All Pins
- -40°C to +125°C Operating Temperature Range
- 9mm x 9.5mm 64-Pin LGA Package

Ordering Information and Application Block Diagram appear at end of datasheet.

19-100526; Rev 3; 3/22

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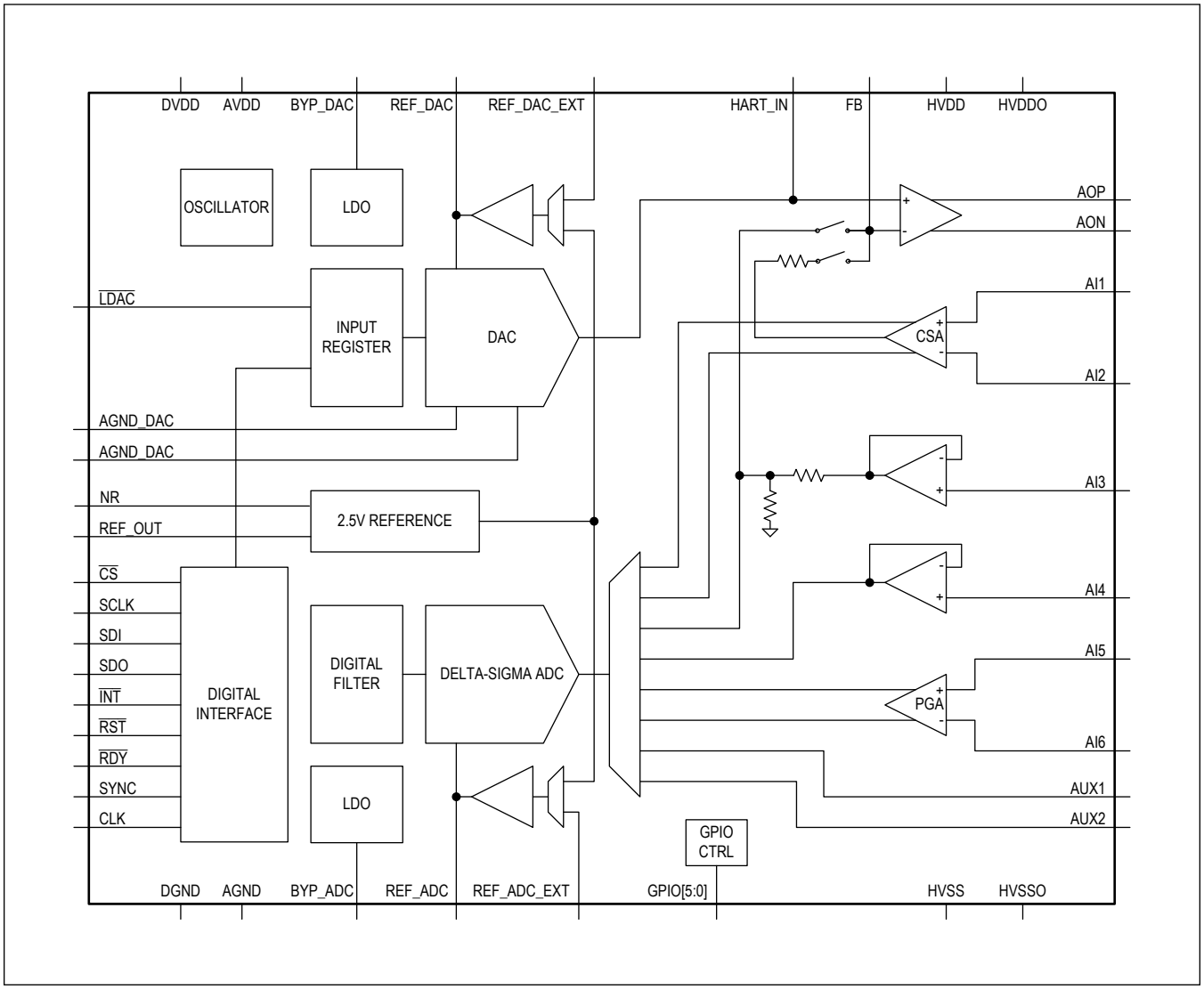
Functional Block Diagram



Absolute Maximum Ratings

AVDD to AGND ..... -0.3V to +3.9V
DVDD to DGND ..... -0.3V to +3.9V
AGND to DGND ..... -0.3V to +0.3V
AGND_DAC to AGND ..... -0.3V to +0.3V
AGND_DAC to DGND ..... -0.3V to +0.3V
AVDD to REF_DAC_EXT ..... -0.3V to +3.9V
BYP_ADC to DGND ..... -0.3V to +2.1V
HVDD to HVSS ..... -0.3V to +52V
HVDDO to HVSSO ..... -0.3V to +52V
HVDD to AGND ..... -0.3V to +40V
HVDDO to AGND ..... -0.3V to +40V
AGND to HVSS ..... -0.3V to +40V
AGND to HVSSO ..... -0.3V to +40V
HVSSO to HVSS ..... -0.3V to +40V
AI_ to HVSS ..... -0.3V to the lower of +52V or $((V_{HVDD}-V_{HVSS})+0.3V)$
HART_IN, FB to HVSSO ..... -0.3 to the lower of +52V or $((V_{HVDDO}-V_{HVSSO})+0.3V)$
$\overline{INT}$ to DGND ..... -0.3V to +6V
$\overline{CS}$, SCLK, SDI, SDO, $\overline{RDY}$, $\overline{RST}$, SYNC, CLK, $\overline{LDAC}$, GPIO_ to DGND ..... -0.3 to the lower of +3.9V or $(V_{DVDD}+0.3V)$
REF_ADC, REF_DAC, AUX1, AUX2, REF_ADC_EXT, REF_DAC_EXT, NR, REF_OUT, BYP_DAC to AGND ..... -0.3 to the lower of +3.9V or $(V_{AVDD}+0.3V)$
AON to HVSS ..... -0.3V to +80V
AOP to HVDDO ..... -70V to +0.3V
AON to HVSSO ..... -0.3V to +70V
Maximum Current into AOP, AON ..... ±100mA
Maximum Current into Any Other Pin ..... ± 50mA
Continuous Power Dissipation (T_A = +70°C)
64-Pin LGA (derate 42.8mW/°C over T_A = +70°C) ..3418.8mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

64 LGA

Package Code	L649A9M+1
Outline Number	21-100274
Land Pattern Number	90-100096
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	23.4°C/W
Junction to Case (θ_{JC})	7.0°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG OUTPUT VOLTAGE MODE						
Output Voltage Range	V_{OUT}	12.5V setting, DAC full-scale range (Note 2)		±12.5		V
		12.5V setting, linear range (Note 2, Note 3)	-10.5		+10.5	
		25V setting (Note 2)		+25		
Dropout Voltage		V_{HVDDO} = +13V, sourcing 25mA, measured between HVDDO and AOP, gain compression <1%			0.85	V
		V_{HVDDO} = -13V, sinking 25mA, measured between AON and HVSSO, gain compression <1%			0.85	
Output Current Protection		Output shorted to HVDDO or HVSSO, threshold current (Note 4)		50		mA
		Output shorted to HVDDO or HVSSO, average current (Note 4)		13		
AOP, AON High Impedance Leakage Current		Measured at the combined output after the external diodes			±0.5	µA
Offset Error	V_{OFF}	T_A = +25°C before calibration			±150	mV
Offset Calibration Range				±12.5		V
Offset Calibration Resolution				95		µV
Offset Drift		T_A = +50°C ± 50°C with internal reference (Note 5)		±18		µV/°C
Gain Error		T_A = +25°C before calibration	0		4	%
Gain Calibration Range				0 to 100		%
Gain Calibration Resolution				4		ppm
Gain Drift		T_A = +50°C ± 50°C with internal reference (Note 5)		±3.3		ppm/°C
INL Error	INL	T_A = +25°C			±300	µV
INL Drift		T_A = +50°C ± 50°C (Note 5)		±3		µV/°C
Output Noise	V_N	10kHz bandwidth		85		$µV_{RMS}$
Supply Rejection Ratio	PSRR	DC, 12.5V setting, V_{OUT} = 0V, V_{HVDD} = V_{HVDDO} = +5V to +24V		120		dB
		DC, 12.5V setting, V_{OUT} = 0V, V_{HVSS} = V_{HVSSO} = -24V to -5V		115		
Load Regulation		-10mA ≤ I_{LOAD} ≤ +10mA, measured at V_{OUT} = -10.5V and V_{OUT} = +10.5V, output change due to self-heating excluded		±0.1		mV
AI3 Headroom		From V_{HVSS} (Note 3)	2.5			V
		From V_{HVDD} (Note 3)	2.5			

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AI3 Input Current		(Note 5)			±20	nA
Settling Time		12.5V setting, resistive load from 1kΩ to 10MΩ; settling to 1% for V_{OUT} = 0V to +10.5V or 0V to -10.5V		0.2		ms
		12.5V setting, capacitive load up to 1µF; settling to 1% for V_{OUT} = 0V to +10.5V or 0V to -10.5V		1		
Bandwidth of 25V Setting		-3dB bandwidth from HART_IN to output, 25V setting, load as depicted in Figure 3		10		kHz
ANALOG OUTPUT CURRENT MODE						
Output Current Range	I_{OUT}	25mA setting, R_{SENSE} = 50Ω, DAC full-scale range (Note 6)		±25		mA
		25mA setting, R_{SENSE} = 50Ω, linear range (Note 3, Note 6)	-21		+21	
		2.5mA setting, R_{SENSE} = 50Ω, DAC full-scale range (Note 6)		±2.5		
		2.5mA setting, R_{SENSE} = 50Ω, linear range (Note 3, Note 6)	-2.1		+2.1	
Dropout Voltage		Sourcing 25mA, measured between HVDDO and AOP, gain compression <1%			0.85	V
		Sinking 25mA, measured between AON and HVSSO, gain compression <1%			0.85	
Offset Error	I_{OFF}	25mA setting, T_A = +25°C before calibration			±300	µA
		2.5mA setting, T_A = +25°C before calibration			±30	
Offset Calibration Range		25mA setting		±25		mA
		2.5mA setting		±2.5		
Offset Calibration Resolution		25mA setting		200		nA
		2.5mA setting		20		
Offset Drift		25mA setting, T_A = +50°C ± 50°C with internal reference (Note 5)		±36		nA/°C
		2.5mA setting, T_A = +50°C ± 50°C, with internal reference (Note 5)		±4		
Gain Error		25mA setting, T_A = +25°C before calibration	0		4	%
Gain Calibration Range		All settings		0 to 100		%
Gain Calibration Resolution		All settings		4		ppm
Gain Drift		25mA setting, T_A = +50°C ± 50°C, with internal reference (Note 5)		±3.2		ppm/°C
INL Error	INL	25mA setting, T_A = +25°C			±600	nA

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INL Drift		25mA setting, T_A = +50°C ± 50°C (Note 5)		±6		nA/°C
Output Noise	I_N	25mA setting, 10kHz bandwidth		270		nA_{RMS}
		2.5mA setting, 10Hz bandwidth		25		nA_{p-p}
Supply Rejection	PSR	DC, 25mA setting, V_{HVDD} = V_{HVDDO} = +5V to +24V		10		nA/V
		DC, 25mA setting, V_{HVSS} = V_{HVSSO} = -24V to -5V		10		
AI1, AI2 Headroom		From V_{HVSS} (Note 3)	2.5			V
		From V_{HVDD} (Note 3)	2.5			
AI1, AI2 Input Current		(Note 5)			±20	nA
Common-Mode Rejection	CMR	AI1, AI2 in CSA mode, V_{AI1} = V_{AI2} = V_{CM}, V_{CM} = -16V to +16V			0.5	µA/V
AI1 and AI2 Differential Input Range		AI1, AI2 in CSA mode		±1.25		V
AI1 and AI2 Differential Input Impedance		AI1, AI2 in CSA mode		100		MΩ
Settling Time		Resistive load up to 250Ω; settling to 1% for I_{OUT} = 0mA to +21mA or 0mA to -21mA		0.5		ms
		Resistive load up to 750Ω; settling to 1% for I_{OUT} = 0mA to +21mA or 0mA to -21mA		1.0		
		Inductive load up to 1mH; settling to 1% for I_{OUT} = 0mA to +21mA or 0mA to -21mA		0.5		
ANALOG INPUT VOLTAGE MODE (AI1 TO AI4)						
Headroom		From V_{HVSS} (Note 3)	2.5			V
		From V_{HVDD} (Note 3)	2.5			
Input Voltage Range	V_{IN}	ADC full-scale range		±12.5		V
		Linear range (Note 3)	-10.5		+10.5	
Offset Error	V_{OFF}	T_A = +25°C before calibration			±25	mV
Offset Calibration Range				±12.5		V
Offset Calibration Resolution				3		µV
Offset Drift		T_A = +50°C ± 50°C with internal reference (Note 5)		±12		µV/°C
Gain Error		T_A = +25°C before calibration			±4	%
Gain Calibration Range				0 to 200		%
Gain Calibration Resolution				0.1		ppm
Gain Drift		T_A = +50°C ± 50°C with internal reference (Note 5)		±2.2		ppm/°C

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INL Error	INL	T_A = +25°C			±600	µV
INL Drift		T_A = +50°C ± 50°C (Note 5)		±2.4		µV/°C
Input Voltage Noise	V_N	ADC sample rate is 57.6ksps, ADC mode is Continuous		85		$µV_{RMS}$
Input Current		(Note 5)			±20	nA
Supply Rejection Ratio	PSRR	DC, V_{HVDD} = +5V to +24V		100		dB
		DC, V_{HVSS} = -24V to -5V		100		
50/60Hz Normal Mode Rejection		DCHNL_RATE[3:0] = 0b0010, 0b0011, 0b0100, 0b0101	87			dB
		DCHNL_RATE[3:0] = 0b0000, 0b0001	75			
Open/Short Detector Resistance		From any AI1 through AI6 to HVDD		2		MΩ
		From any AI1 through AI6 to AGND		2		
Settling Time		V_{IN} changes from 0V to +10.5V or 0V to -10.5V, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		µs
ANALOG INPUT VOLTAGE MODE – PGA (AI5, AI6)						
Headroom		From V_{HVSS} (Note 3)	2.5			V
		From V_{HVDD} (Note 3)	2.5			
Input Voltage Range	V_{IN}	25V setting, ADC full-scale range		±25		V
		25V setting, linear range (Note 3)	-21		21	
		2.5V setting, ADC full-scale range		±2.5		
		2.5V setting, linear range (Note 3)	-2.1		+2.1	
		500mV setting, ADC full-scale range		±500		mV
		500mV setting, linear range (Note 3)	-420		+420	
		250mV setting, ADC full-scale range		±250		
		250mV setting, linear range (Note 3)	-210		+210	
		125mV setting, ADC full-scale range		±125		
		125mV setting, linear range (Note 3)	-105		+105	
Offset Error	V_{OFF}	25V setting, T_A = +25°C before calibration			±25	mV
		2.5V setting, T_A = +25°C before calibration		±300		µV
		500mV setting, T_A = +25°C before calibration			±500	
		250mV setting, T_A = +25°C before calibration		±30		
		125mV setting, T_A = +25°C before calibration		±15		

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Calibration Range		25V setting		±25		V
		2.5V setting		±2500		mV
		500mV setting		±500		
		250mV setting		±250		
		125mV setting		±125		
Offset Calibration Resolution		25V setting		6		µV
		2.5V setting		0.6		
		500mV setting		0.12		
		250mV setting		0.06		
		125mV setting		0.03		
Offset Drift		25V setting, T_A = +50°C ± 50°C with internal reference (Note 5)		±12		µV/°C
		500mV setting, T_A = +50°C ± 50°C with internal reference (Note 5)		±600		nV/°C
Gain Error		All voltage settings, T_A = +25°C before calibration			±4	%
Gain Calibration Range				0 to 200		%
Gain Calibration Resolution				0.1		ppm
Gain Drift		25V setting, T_A = +50°C ± 50°C with internal reference (Note 5)		±2.2		ppm/°C
		All other voltage settings, T_A = +50°C ± 50°C with internal reference (Note 5)		±1.1		
INL Error	INL	25V setting, T_A = +25°C			±600	µV
		500mV setting, T_A = +25°C			±170	µV
INL Drift		25V setting, T_A = 25°C ± 50°C (Note 5)		±35		µV/°C
		500mV setting, T_A = +50°C ± 50°C (Note 5)		±3.5		µV/°C
Input Voltage Noise	V_N	25V setting, ADC sample rate is 57.6ksps, ADC mode is Continuous		85		μV_{RMS}
		500mV setting, ADC sample rate is 900sps, ADC mode is Continuous		4		μV_{P-P}
Input Common Mode Range		25V setting, guaranteed by CMRR (Note 7)	-6.25		+6.25	V
		All other voltage settings, guaranteed by CMRR (Note 7)	-1.25		+1.25	
Common Mode Rejection Ratio	CMRR	25V setting, V_{CM} = -6.25V to +6.25V	60			dB
		2.5V setting, V_{CM} = -1.25V to +1.25V	80			
		All other voltage settings, V_{CM} = -1.25V to +1.25V	92			
Supply Rejection Ratio	PSRR	DC, V_{HVDD} = +5V to +24V		100		dB
		DC, V_{HVSS} = -24V to -5V		100		

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
50/60Hz Normal Mode Rejection		DCHNL_RATE[3:0] = 0b0010, 0b0011, 0b0100, 0b0101	87			dB
		DCHNL_RATE[3:0] = 0b0000, 0b0001	75			
Input Current		(Note 5)			±20	nA
Settling Time		25V setting, V_{IN} changes from 0V to +21V or 0V to -21V, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		µs
		500mV setting, V_{IN} changes from 0V to +420mV or 0V to -420mV, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		
AMPLIFIER INPUTS (HART_IN, FB)						
Input Bias Voltage				±2.5		V
AUX INPUTS (AUX1, AUX2)						
Headroom		From V_{HVSS} (Note 3)	2.5			V
		From V_{HVDD} (Note 3)	2.5			
Input Voltage Range	V_{IN}	ADC linear range, single-ended (Note 3)		+0.1 to +2.4		V
		ADC linear range, differential (Note 3)		-2.3 to +2.3		
Offset Error	V_{OFF}	T_A = +25°C before calibration		±0.5	±2.5	mV
Offset Calibration Range		Single-ended		0 to 2.5		V
		Differential		±2.5		
Offset Calibration Resolution				0.3		µV
Offset Drift		T_A = +50°C ± 50°C with internal reference (Note 5)		±1		µV/°C
Gain Error		T_A = +25°C before calibration			±4	%
Gain Calibration Range				0 to 200		%
Gain Calibration Resolution				0.1		ppm
Gain Drift		T_A = +50°C ± 50°C, with internal reference (Note 5)		±1		ppm/°C
INL Error	INL	T_A = +25°C		±15	±60	µV
INL Drift		T_A = +50°C ± 50°C (Note 5)		±50		nV/°C
Input Voltage Noise	V_N	ADC sample rate is 57.6ksps, ADC mode is Continuous		8		$µV_{RMS}$
Supply Rejection Ratio	PSRR	DC, V_{HVDD} = +5V to +24V		100		dB
		DC, V_{HVSS} = -24V to -5V		100		

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
50/60Hz Normal Mode Rejection		DCHNL_RATE[3:0] = 0b0010, 0b0011, 0b0100, 0b0101	87			dB
		DCHNL_RATE[3:0] = 0b0000, 0b0001	75			
Input Current	I_{IN}	(Note 5)			±20	nA
Settling Time		V_{IN} changes from 0.1V to +2.4V, digital output reaches 1% of final value, ADC sample rate is 57.6ksps, ADC mode is Continuous		100		µs
DAC REFERENCE (REF_DAC)						
REF_DAC Output Voltage	V_{REF_DAC}	Internal reference		2.5		V
Output Voltage Accuracy		Referred to V_{REF_DAC}, T_A = +25°C	-0.2		+0.2	%
Output Voltage Temperature Coefficient		T_A = -40°C to +125°C (Note 5)		5		ppm/°C
Line Regulation		2.7V ≤ V_{AVDD} ≤ 3.6V			50	µV/V
REF_DAC Bypass Capacitor				100		pF
REF_DAC_EXT Input Range		External reference		2.5		V
ADC REFERENCE (REF_ADC)						
REF_ADC Output Voltage	V_{REF_ADC}	Internal reference		2.5		V
Output Voltage Accuracy		Referred to V_{REF_ADC}, T_A = +25°C	-0.2		+0.2	%
Output Voltage Temperature Coefficient		T_A = -40°C to +125°C (Note 5)		5		ppm/°C
Line Regulation		2.7V ≤ V_{AVDD} ≤ 3.6V			250	µV/V
REF_ADC Bypass Capacitor				4.7		µF
REF_ADC_EXT Input Range		External reference		2.5		V
DIGITAL INPUTS ($\overline{CS}$, SCLK, SDI, $\overline{RST}$, SYNC, CLK, $\overline{LDAC}$, GPIO0 THROUGH GPIO5)						
Input Logic Low Voltage	V_{IL}				0.3×V_{DVDD}	V
Input Logic High Voltage	V_{IH}		0.7×V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}		-1		+1	µA
Input Capacitance	C_{IN}			10		pF
DIGITAL OUTPUTS (SDO, $\overline{RDY}$, $\overline{INT}$, GPIO0 THROUGH GPIO5)						
Output Logic Low Voltage	V_{OL}	I_{SINK} = 4mA			0.4	V

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic High Voltage	V_{OH}	I_{SOURCE} = 4mA, except $\overline{INT}$	0.9×V_{DVDD}			V
Three-State Leakage Current			-10		+10	µA
Three-State Output Capacitance				10		pF
POWER SUPPLIES						
Analog Supply Voltage	V_{AVDD}		2.7	3.3	3.6	V
Digital Supply Voltage	V_{DVDD}		2.7	3.3	3.6	V
Positive High Voltage Supply	V_{HVDD}		5		28	V
Negative High Voltage Supply	V_{HVSS}		-24		-5	V
High Voltage Supply	V_{HV}	V_{HVDD} - V_{HVSS}	10		48	V
Positive High Voltage Output Supply	V_{HVDDO}		5		28	V
Negative High Voltage Output Supply	V_{HVSSO}		-24		-5	V
High Voltage Output Supply	V_{HVO}	V_{HVDDO} - V_{HVSSO}	10		48	V
DVDD POR Threshold		Voltage rising		1.6		V
HVDD Undervoltage Threshold		Voltage rising		1.5		V
Analog Supply Quiescent Current	I_{AVDD_Q}	Analog output voltage mode		5.5		mA
		Analog output current mode		5.5		
		Analog inputs AI1-AI6		5.2		
		Analog inputs and output		8		
Digital Supply Quiescent Current	I_{DVDD_Q}	Analog output voltage mode		1.4		mA
		Analog output current mode		1.4		
		Analog inputs AI1-AI6		2.4		
		Analog inputs and output		2.4		
High-Voltage Quiescent Current	I_{HV_Q}	Analog output voltage mode, no load current		2.3		mA
		Analog output current mode, no load current		3.3		
		Analog inputs AI1-AI6, AI1-AI6 at AGND		2.8		
		Analog inputs and output, AI1-AI6 at AGND, no load current		3.5		

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Quiescent Power	P_Q	Analog output voltage mode, no load current, V_{HVDD} = V_{HVDDO} = +15V, V_{HVSS} = V_{HVSSO} = -15V		90		mW
		Analog output current mode, no load current, V_{HVDD} = V_{HVDDO} = +15V, V_{HVSS} = V_{HVSSO} = -15V		120		
		Analog inputs AI1-AI6, AI1-AI6 at AGND, V_{HVDD} = V_{HVDDO} = +15V, V_{HVSS} = V_{HVSSO} = -15V		110		
		Analog inputs and output, AI1-AI6 at AGND, no load current, V_{HVDD} = V_{HVDDO} = +15V, V_{HVSS} = V_{HVSSO} = -15V		140		
PROTECTION						
Thermal Shutdown Threshold	T_{SHDN}	Temperature rising until the analog I/O configuration resets		+165		°C
Thermal Warning Threshold	T_{WARN}	Temperature rising until interrupt assertion		+145		°C
Thermal Warning Hysteresis	T_{WARN_HYS}			10		°C
TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}	All SPI transactions except analog output DAC register read-back			20	MHz
		Analog output DAC register read-back, registers 0x44 through 0x47			10	
SCLK Clock Period	t_{CP}	All SPI transactions except analog output DAC register read-back	50			ns
		Analog output DAC register read-back, registers 0x44 through 0x47	100			
SCLK Pulse Width High	t_{CH}	All SPI transactions except analog output DAC register read-back	13			ns
		Analog output DAC register read-back for registers 0x44 through 0x47	40			
SCLK Pulse Width Low	t_{CL}	All SPI transactions except analog output DAC register read-back	20			ns
		Analog output DAC register read-back, registers 0x44 through 0x47	40			
$\overline{CS}$ Fall Setup Time	t_{CSS0}	$\overline{CS}$ falling edge to first SCLK rising edge setup time	7			ns
$\overline{CS}$ Rise Setup Time	t_{CSS1}	$\overline{CS}$ rising edge to SCLK rising edge setup time	5			ns
$\overline{CS}$ Fall Hold Time	t_{CSH0}	SCLK rising edge to $\overline{CS}$ falling edge hold time	0			ns
$\overline{CS}$ Rise Hold Time	t_{CSH1}	SCLK falling edge to $\overline{CS}$ rising edge hold time	3			ns

Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +2.7V to +3.6V, V_{HVDD} = V_{HVDDO} = +18.0V; V_{HVSS} = V_{HVSSO} = -18.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width High	t_{CSW}	Minimum $\overline{CS}$ pulse width high	150			ns
SDI Setup Time	t_{DS}	SDI setup time to SCLK rising edge	10			ns
SDI Hold Time	t_{DH}	SDI hold time after SCLK rising edge	5			ns
SDO Transition Time	t_{DOT}	SDO transition valid after SCLK falling edge			20	ns
SDO Hold Time	t_{DOH}	Output remains valid after falling edge of SCLK	1			ns
SDO Disable Time	t_{DOD}	$\overline{CS}$ rising edge to SDO disable, C_{LOAD} = 20pF			80	ns
ESD AND SURGE PROTECTION						
ESD		Human Body Model, all pins		±1		kV
IEC Surge	V_{SURGE}	IEC 61000-4-5, 1.2/50µs pulse, pins AI1-AI6, 4.75kΩ series MELF resistor		±1		kV

Note 1: Maximum and minimum limits are 100% tested with typical supply voltage levels at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and device characterization.

Note 2: The output voltage is measured at the sense voltage input (AI3). The supply voltage must fulfill the input headroom requirements, as well as the output amplifier requirements. Assuming that AI1, AI2, and AI3 are connected to the output, AI1 dictates the headroom requirement. Assuming a 25mA load current, a ±12.5V output, and a 50Ω sense resistor, the minimum supply voltage to fulfill the AI1 headroom requirement is the output voltage (V_{OUT}) plus the voltage drop across the sense resistor plus 2.5V, resulting in a supply voltage requirement of ±16.25V. The minimum supply voltage required for the output amplifier is the sum of the V_{OUT}, the voltage across the sense resistor, the diode forward voltage, and the dropout voltage. For a 25mA load current, a ±12.5V output, a 50Ω sense resistor, and a diode forward voltage of 750mV, the minimum supply voltage required by the output amplifier is ±15.35V. Overall, the minimum supply voltage is ±16.25V.

Note 3: Offset error, gain error, INL error, and settling times are only guaranteed in the linear range. The minimum and maximum specification of the linear range and input headroom are guaranteed through offset, gain, and INL error.

Note 4: The threshold current specifies the typical current that triggers the short circuit protection. The average current that accounts for self heating of the device is significantly smaller due to the duty cycle when OVC_CTRL is set to logic low.

Note 5: Not production tested. Guaranteed by design and device characterization.

Note 6: The supply voltage must fulfill the AI1 and AI2 headroom requirements, as well as the output amplifier requirements. The minimum supply voltage required to fulfill the AI1 and AI2 headroom is 2.5V plus the output current times the sum of the load and cable resistances, and the voltage across the sense resistor. The minimum supply voltage required for the output amplifier is the output current times the sum of the load and cable resistances, the voltage across the sense resistor, the diode forward voltage, and the dropout voltage. For a 25mA output current, a load resistor of 500Ω, a cable resistance of 250Ω, a 50Ω sense resistor, and a diode forward voltage of 750mV, the minimum headroom for AI1 and AI2 requires a supply voltage of ±22.5V, while the supply voltage required by the output amplifier is ±21.6V. Overall, the minimum supply voltage is ±22.5V.

Note 7: The maximum allowed input common-mode range depends on the signal amplitude. The minimum and maximum values given in the *Electrical Characteristics* table apply to the maximum signal amplitude allowed for a given setting. Refer to the *PGA Input Common-Mode Range* section for the allowed input common-mode range for smaller signal amplitudes.

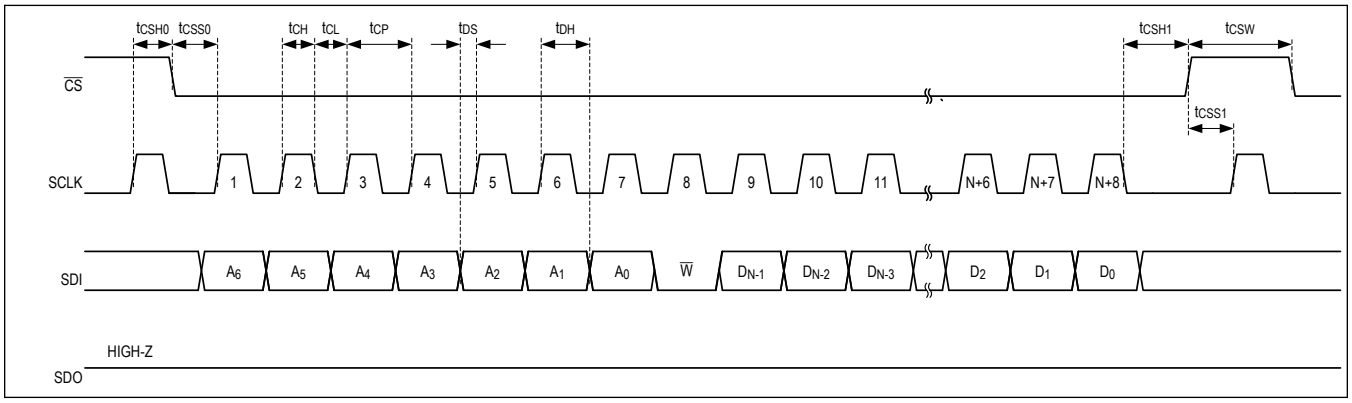


Figure 1. SPI Write Timing (N=24 when CRC is Disabled, N=32 when CRC is Enabled)

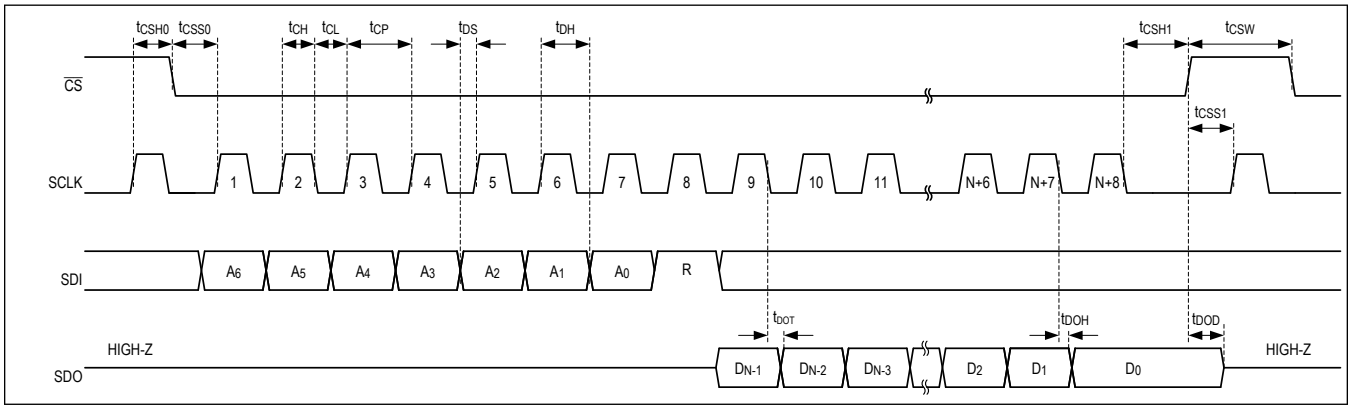
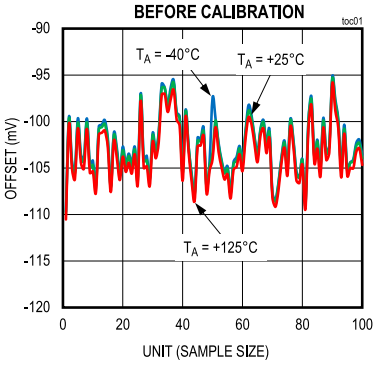


Figure 2. SPI Read Timing (N = 24 when CRC is Disabled, N = 32 when CRC is Enabled)

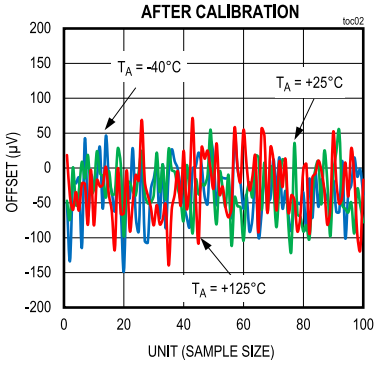
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C unless specified otherwise)

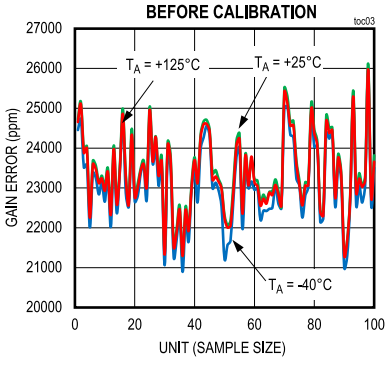
VOLTAGE OUTPUT MODE
OFFSET VOLTAGE DISTRIBUTION
BEFORE CALIBRATION



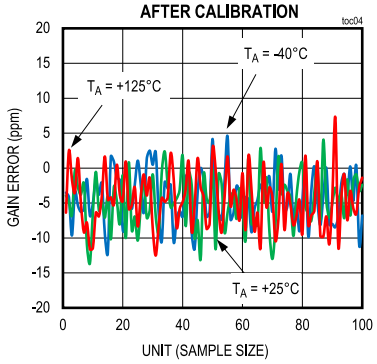
VOLTAGE OUTPUT MODE
OFFSET VOLTAGE DISTRIBUTION
AFTER CALIBRATION



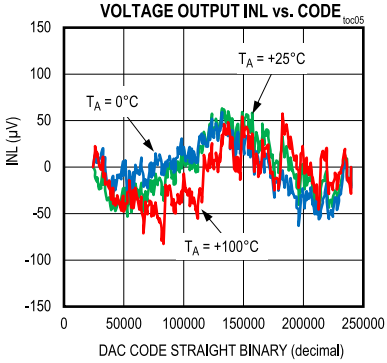
VOLTAGE OUTPUT MODE
GAIN ERROR DISTRIBUTION
BEFORE CALIBRATION



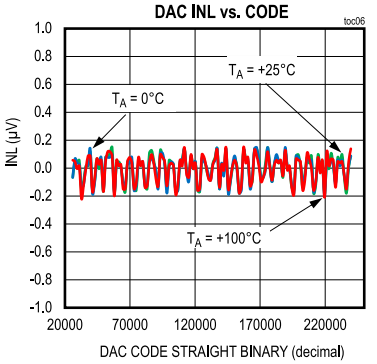
VOLTAGE OUTPUT MODE
GAIN ERROR DISTRIBUTION
AFTER CALIBRATION



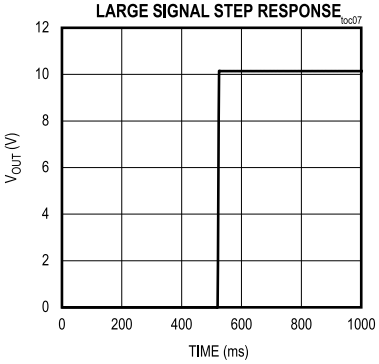
VOLTAGE OUTPUT INL vs. CODE



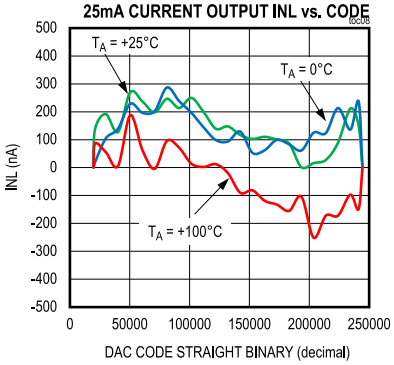
DAC INL vs. CODE



LARGE SIGNAL STEP RESPONSE



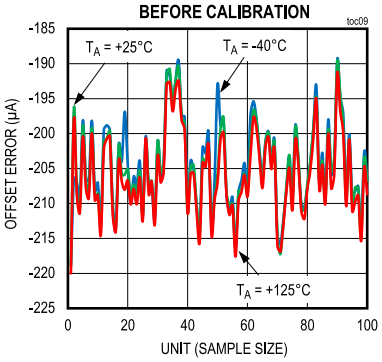
25mA CURRENT OUTPUT INL vs. CODE



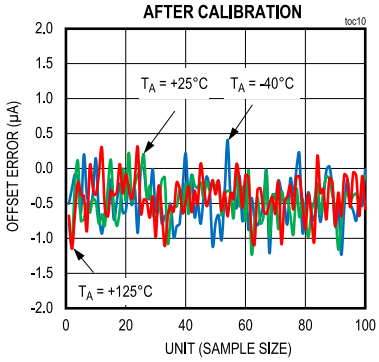
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C unless specified otherwise)

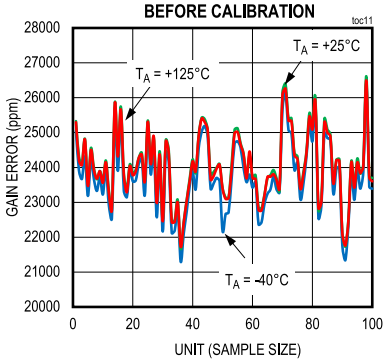
CURRENT OUTPUT MODE
OFFSET ERROR DISTRIBUTION
BEFORE CALIBRATION



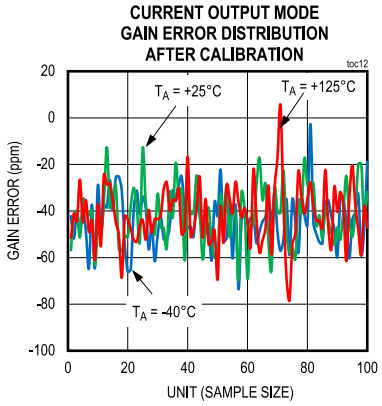
CURRENT OUTPUT MODE
OFFSET ERROR DISTRIBUTION
AFTER CALIBRATION



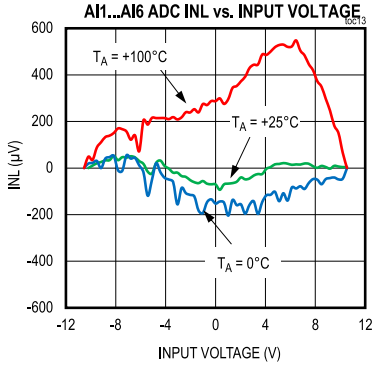
CURRENT OUTPUT MODE
GAIN ERROR DISTRIBUTION
BEFORE CALIBRATION



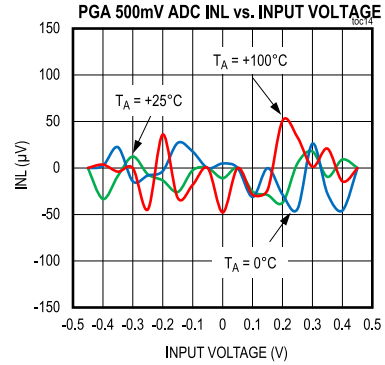
CURRENT OUTPUT MODE
GAIN ERROR DISTRIBUTION
AFTER CALIBRATION



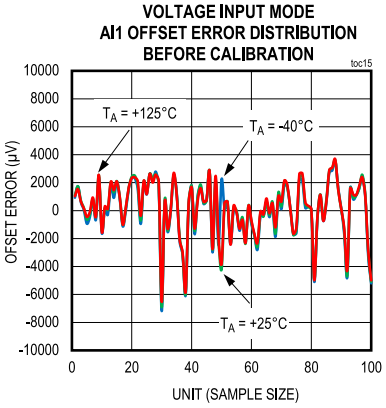
AI1...AI6 ADC INL vs. INPUT VOLTAGE



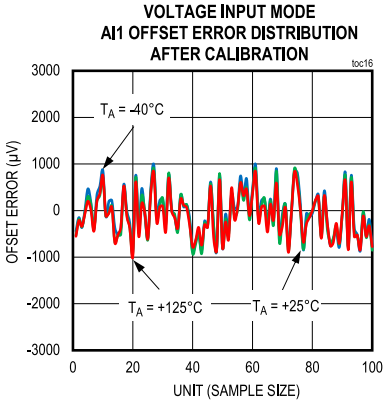
PGA 500mV ADC INL vs. INPUT VOLTAGE



VOLTAGE INPUT MODE
AI1 OFFSET ERROR DISTRIBUTION
BEFORE CALIBRATION

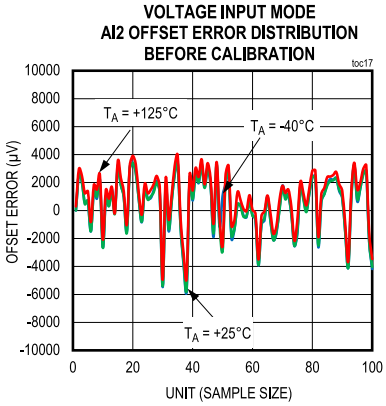


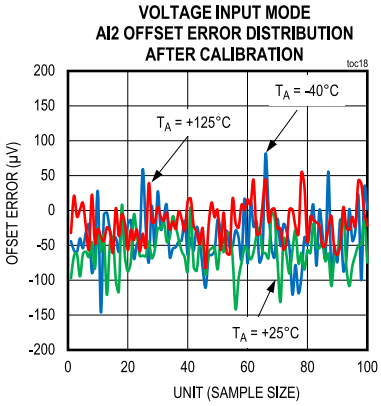
VOLTAGE INPUT MODE
AI1 OFFSET ERROR DISTRIBUTION
AFTER CALIBRATION

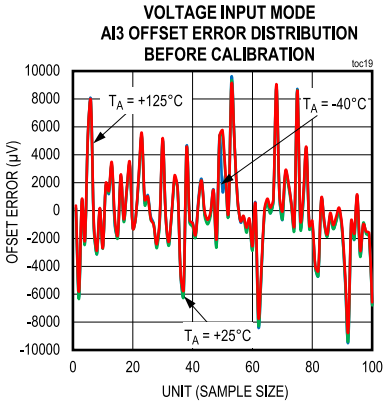


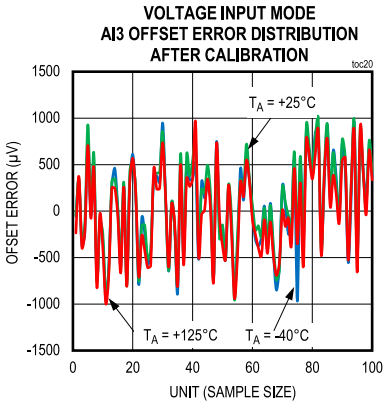
Typical Operating Characteristics (continued)

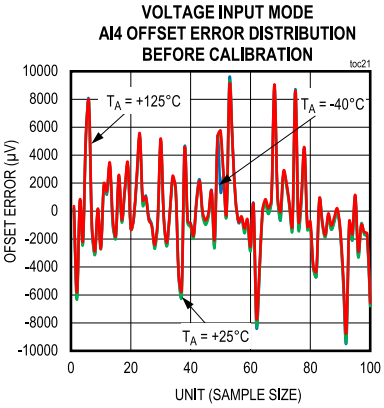
(V_{AVDD} = V_{DVDD} = 3.3V, V_{HVDD} = V_{HVDDO} = +18.0V, V_{HVSS} = V_{HVSSO} = -18.0V, T_A = +25°C unless specified otherwise)

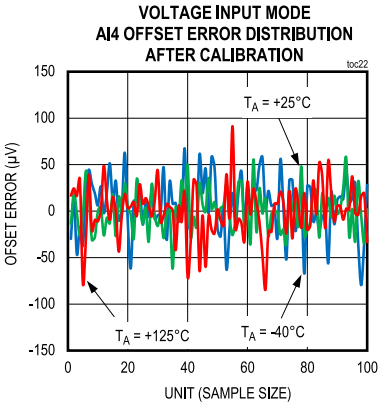




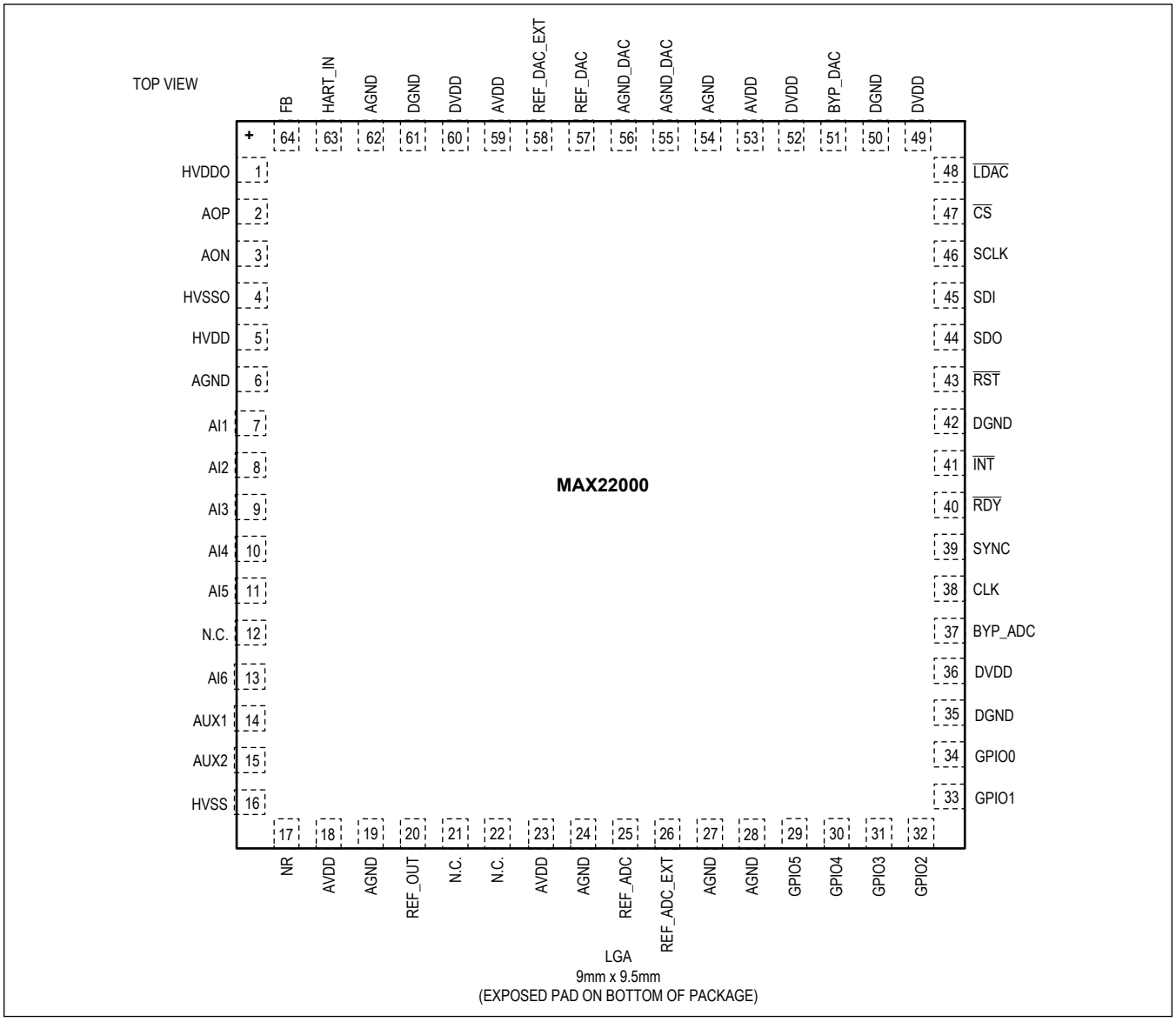








Pin Configuration



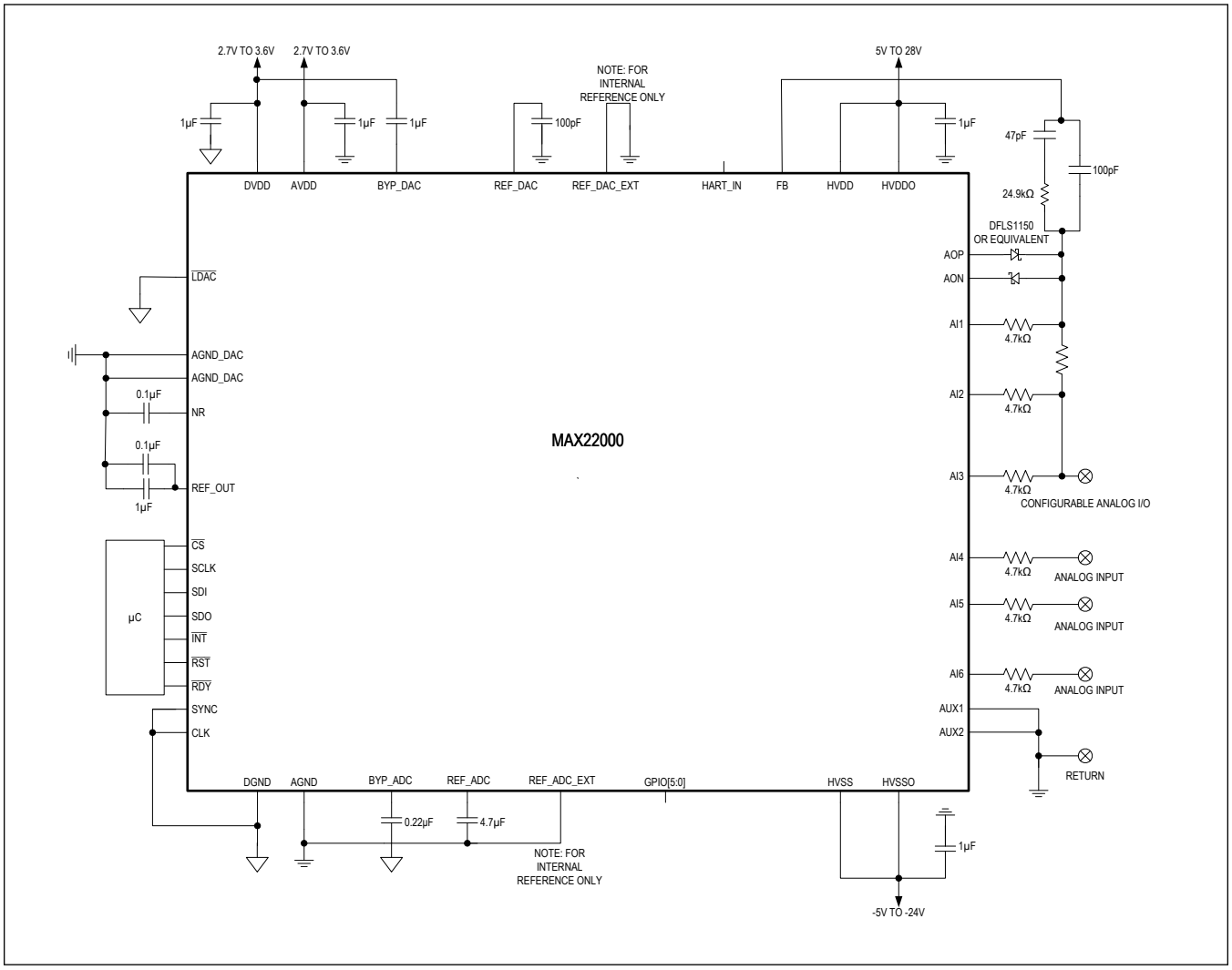
Pin Description

PIN	NAME	FUNCTION
1	HVDDO	Positive High-Voltage Supply for the Output Path. Bypass to AGND with a minimum of 1µF ceramic capacitor as close to the device as possible.
2	AOP	Positive Transmit Output. Connect to the anode of an external diode.
3	AON	Negative Transmit Output. Connect to the cathode of another external diode.
4	HVSSO	Negative High-Voltage Supply for the Output Path. Bypass to AGND with a minimum of 1µF ceramic capacitor as close to the device as possible.
5	HVDD	Positive High-Voltage Supply for the Input Paths. Bypass to AGND with a minimum of 1µF ceramic capacitor as close to the device as possible.
6, 19, 24, 27, 28, 54, 62	AGND	Analog Ground
7	AI1	Analog Input 1. In analog output current mode, the positive input of the current sense feedback amplifier. In all other modes, either the positive input of a current sense to the ADC with AI2, or a voltage sense to the ADC.
8	AI2	Analog Input 2. In analog output current mode, the negative input of the current sense feedback amplifier. In all other modes, either the negative input of a current sense to the ADC with AI1, or a voltage sense to the ADC.
9	AI3	Analog Input 3. In analog output voltage mode, the input to the voltage sense feedback amplifier. In all other modes, a high-voltage sense to the ADC.
10	AI4	Analog Input 4. A high-voltage sense to the ADC.
11	AI5	Analog Input 5. Along with AI6, a positive voltage input of a differential pair to the ADC.
12, 21, 22	N.C.	Not Connected. Do not connect.
13	AI6	Analog Input 6. Along with AI5, a negative voltage input of a differential pair to the ADC.
14	AUX1	Auxiliary Input 1. First of two auxiliary inputs to the ADC.
15	AUX2	Auxiliary Input 2. Second of two auxiliary inputs to the ADC.
16	HVSS	Negative High-Voltage Supply for the Input Paths. Bypass to AGND with a minimum of 1µF ceramic capacitor to AGND.
17	NR	Reference Noise Reduction. Connect a 0.1µF ceramic capacitor to AGND to reduce wideband noise. Leave unconnected if not used.
18, 23, 53, 59	AVDD	Analog Power Supply. Connect a 2.7V to 3.6V source here. Bypass each pin to AGND with a minimum of 1µF ceramic capacitor as close to the device as possible.
20	REF_OUT	Voltage Reference Output. Bypass to AGND with a minimum of 1µF ceramic capacitor in parallel with a 0.1µF ceramic capacitor as close to the device as possible.
25	REF_ADC	ADC Buffered Reference Voltage Output. Bypass to AGND with a minimum of 4.7µF ceramic capacitor as close to the device as possible.
26	REF_ ADC_EXT	ADC External Voltage Reference Input. If used to supply an external reference, bypass to AGND with a minimum 0.01µF ceramic capacitor as close to the device as possible. If unused, connect to AGND.
29	GPIO5	General Purpose Digital Input/Output 5
30	GPIO4	General Purpose Digital Input/Output 4
31	GPIO3	General Purpose Digital Input/Output 3
32	GPIO2	General Purpose Digital Input/Output 2
33	GPIO1	General Purpose Digital Input/Output 1
34	GPIO0	General Purpose Digital Input/Output 0
35, 42, 50, 61	DGND	Digital Ground

Pin Description (continued)

PIN	NAME	FUNCTION
36, 49, 52, 60	DVDD	Digital Power Supply. Connect a 2.7V to 3.6V source here. Bypass each pin to DGND with a minimum 1µF ceramic capacitor as close to the device as possible.
37	BYP_ADC	ADC Regulator Bypass. Bypass to DGND with a minimum 0.22µF ceramic capacitor.
38	CLK	External Clock Input (Optional). Use a 7.3728MHz frequency to match internal clock and to meet filter requirements. Connect to DGND if unused.
39	SYNC	ADC Synchronization Input. SYNC resets the ADC modulator and digital filters. If used, connect the SYNC pins of multiple MAX22000 in parallel. If unused, connect to DGND.
40	$\overline{RDY}$	Data Ready Output. Asserts active low when a new ADC conversion result is available. Reading a sample resets $\overline{RDY}$ inactive high. $\overline{RDY}$ is always driven.
41	$\overline{INT}$	Interrupt Output. Open Drain, asserts active low. Functionality controlled by registers GEN_INT and GEN_INTEN
43	$\overline{RST}$	Reset Input. When asserted active low, reconfigures all registers to their power-on default states, analog output goes high impedance, analog inputs power down, and ADC conversion stops.
44	SDO	SPI Serial Data Output. Three-states when $\overline{CS}$ is inactive high. Connect to SPI MISO signal.
45	SDI	SPI Serial Data Input. Connect to SPI MOSI signal.
46	SCLK	SPI Serial Clock Input. Connect to SPI interface CLK signal.
47	$\overline{CS}$	SPI Slave Select Input. The SPI interface responds only when $\overline{CS}$ is active low.
48	$\overline{LDAC}$	DAC Load Input. When asserted active low, transfers the contents of the DAC data register and updates the DAC output. $\overline{LDAC}$ is ignored while $\overline{RST}$ is active low. Connect to DGND if not used.
51	BYP_DAC	DAC Regulator Bypass. Bypass to DVDD with a minimum of 1µF ceramic capacitor.
55, 56	AGND_DAC	DAC Analog Ground.
57	REF_DAC	DAC Buffered Reference Voltage Output. Bypass to AGND with a minimum of 100pF ceramic capacitor as close to the device as possible.
58	REF_DAC_EXT	DAC External Voltage Reference Input. If used to supply an external reference, bypass to AGND with a minimum of 0.01µF ceramic capacitor as close to the device as possible. If unused, connect to AGND.
63	HART_IN	Highway Addressable Remote Transducer (HART) Input. Please refer to HART_IN description.
64	FB	Transmit Output Buffer Feedback. Please refer to FB pin description.
EP1 through 5	EP1 through 5	Exposed Pad. Exposed pads are on the bottom of the package. Connect to HVSS. Solder exposed pad area to HVSS with multiple vias for best thermal performance.

Application Block Diagram



Detailed Description

The MAX22000 is an industrial-grade, software configurable analog input/output solution. The device offers one output that can be configured as voltage or current output, and also offers up to six analog inputs that can be configured as voltage or current inputs. Two of the analog inputs are configured as a differential programmable gain amplifier (PGA), allowing for both low- and high-voltage inputs. The other analog inputs are high-voltage single-ended inputs. The transmit path (analog output) and the receive path (analog inputs) are completely independent; thus, can be programmed for different configurations and modes of operation.

The MAX22000 provides a high-performance 18-bit DAC in the transmit path, and a 24-bit delta-sigma ADC in the receive path. A high-performance filter follows the ADC to provide 50Hz/60Hz normal mode rejection at select ADC data rates.

The device includes a high-performance 5ppm/°C (max) voltage reference on-chip. However, external references can optionally be used for either or both of the transmit and the receive path.

Modes of Operation

The MAX22000 provides five main modes of operation:

- Analog Output Voltage Mode (AOVM)
- Analog Output Current Mode (AOCM)
- Analog Input Voltage Mode (AIVM)
- Analog Input Current Mode (AICM)
- RTD and TC Modes

Mode selection using the GEN_CNFG register determines which of the available input ports, AI1 through AI6, are used. Analog input conversion on available ports is independent of analog output activity.

For example, providing an analog output voltage requires only the use of AI3 for voltage feedback. If the application only needs this mode, all the other input channels are available for other uses, including the use of AI1 and AI2 as a current sense amplifier (CSA). Providing an analog output current reserves both AI1 and AI2 for current feedback. In this case, the resistor across AI1 and AI2 should be 50Ω. AI1 and AI2 can also report current when providing an analog output voltage. Here, a 50Ω resistor results in a ±25mA current measurement range.

Current measurement using AI5 and AI6 of the MAX22000 relies on an external precision resistor to effect current-to-voltage conversion. For current measurements not using differential sense, a GPIO pin can control an external analog switch to connect or disconnect the current sense resistor electronically.

Alternatively, an application requiring all 4 main modes of operation leaves only AI4, AI5, and AI6 for general use.

Besides their use as general purpose analog inputs, AI5 and AI6 can also be configured as a differential programmable gain amplifier (PGA) for either low-voltage or high-voltage inputs.

Regardless of mode of operation, ports AUX1 and AUX2 are always available for cold junction measurements.

The MAX22000 implements a safety switch, activated by the LINE_CNFG bit in the GEN_CNFG register, ensuring a feedback path whether in a 2-wire, 3-wire, or 4-wire configuration.

Input and Output Range Settings

To maintain the best accuracy, the MAX22000 provides multiple voltage and current ranges for its inputs and outputs.

Table 1 summarizes the available ranges. From narrowest to widest, the nominal range specifies the range for the intended application. The linear range encompasses the nominal range, where performance specifications such as gain error, offset error, INL, PSRR, and CMRR are still guaranteed. Even wider, the full-scale range defines the conversion limits of the data converters. This extended range guards against clipping of signals significantly beyond the nominal range of the application.

The MAX22000 sets the linear range at 105% of the nominal range, and the full-scale range at 125% of the nominal range. For example, for a ±10V nominal range, the MAX22000 provides a linear range of ±10.5V and a full-scale range of ±12.5V.

To provide other ranges, manage the codes in the digital domain. For example, for applications providing a ±5V range, limit the provided DAC code range between negative half-scale and positive half-scale, and double the received ADC code while using ±10V calibration coefficients.

Table 1. Input and Output Ranges

MODE	SETTING	NOMINAL	LINEAR	FULL-SCALE
AOVM	±12.5V	±10.0V	±10.5V	±12.5V
	+25V	N/A	N/A	+12.5V to +37.5V
AOCM	±25mA	±20mA	±21mA	±25mA
	±2.5mA	±2.0mA	±2.1mA	±2.5mA
AIVM	±25V (differential)	±20.0V	±21.0V	±25V
	±12.5V (single-ended)	±10.0V	±10.5V	±12.5V
	±2.5V (differential)	±2.0V	±2.1V	±2.5V
	±500mV (differential)	±400mV	±420mV	±500mV
	±250mV (differential)	±200mV	±210mV	±250mV
	±125mV (differential)	±100mV	±105mV	±125mV

PGA Input Common-Mode Range

If the signal amplitude into the PGA is known to be less than its selected full-scale range, the MAX22000 allows a greater input common-mode range than specified in the *Electrical Characteristics* tables.

For the 25V, 2.5V, 500mV, 250mV, and 125mV settings, the maximum allowed input common-mode range is calculated as follows:

$$V_{CM} = V_{REF} - V_{PEAK} \times \frac{A}{2}$$

where,

V_{CM} = Maximum input in common-mode range

V_{REF} = Reference voltage (2.5V)

V_{PEAK} = Peak input voltage

A = Gain constant as per Table 2

For the 12.5V input range, the maximum input common-mode range is:

$$V_{CM} = 5V_{REF} - \frac{V_{PEAK}}{2}$$

Table 2. Gain Setting for Various Input Voltage Ranges

INPUT	GAIN (A)
25V	1
2.5V	1
500mV	5
250mV	10
125mV	20

Analog Output Setting

Table 3 summarizes settling performance in AOVM and AOCM modes. Settling time is defined as the time for the output to reach 1% error in response to a step of 105% of the linear range.

AOVM 25V mode setting specifies bandwidth instead, using the load circuit shown in Figure 3.

Table 3. Settling Time for Various Load Conditions

ANALOG OUTPUT MODE	LOAD TYPE	MIN LOAD	MAX LOAD	SETTLING TIME
AOVM, 12.5V Setting	Resistive	1kΩ	10MΩ	0.2ms
	Capacitive	0µF	1µF	1.0ms
AOCM	Resistive	0Ω	250Ω	0.5ms
	Resistive	0Ω	750Ω	1.0ms
	Inductive	0mH	1mH	0.5ms

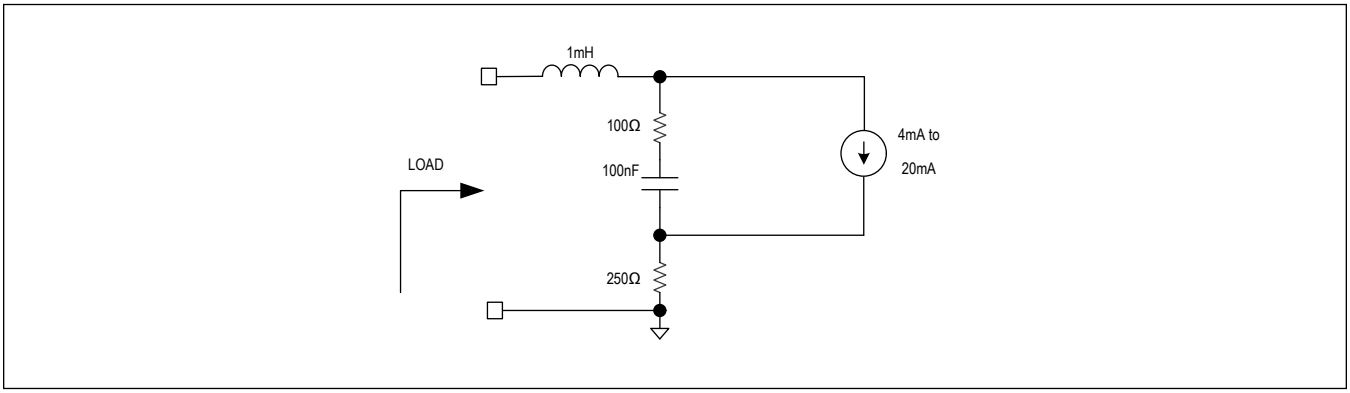


Figure 3. Load Condition for AOVM, 25V Setting

Analog Output Short-Circuit Protection

The MAX22000 provides output short-circuit protection in AOVM mode, responding to possible output overcurrent conditions in one of two ways, selectable using the OVC_CTRL bit in the GEN_CNFG register. In automatic mode, the output goes high impedance when an overcurrent condition is detected, and retries for about 300µs every 6ms until the overcurrent condition ends.

Alternatively, in host controlled mode, the output goes high-impedance and resets bits AO_CNFG[3:0] to 0b0000. The output remains high-impedance until the user writes bits AO_CNFG[3:0] with a code for a proper output configuration.

Regardless of overcurrent mode, the OVC_INT interrupt bit (in the GEN_INT register) asserts high to indicate overcurrent detection. In automatic mode, the OVC_INT bit automatically deasserts low once the MAX22000 senses that the overcurrent condition ends.

The 300µs dwell time ensures that completely discharged capacitive loads up to 1µF, charging to ±10V do not falsely trigger an overcurrent condition in AOVM mode

Power-On Reset

The AVDD and DVDD supplies are monitored by power-on reset circuitry. The MAX22000 is held in a reset state until the AVDD and DVDD supplies have reached a certain threshold that allows safe operation without loss of data. Once this threshold is exceeded, the SPI interface and low-voltage circuitry are fully functional. The high-voltage supplies are also constantly monitored. The MAX22000 needs only the AVDD and DVDD supplies to communicate over the SPI interface. With AVDD and DVDD powered, loss of any high voltage supply is reported through the HVDD_INT and the HVDDO_INT bits in the GEN_INT register.

SPI Interface

An SPI interface allows communication of all important information between a system host and the MAX22000.

An optional CRC enhances confidence in the data communicated to and from the MAX22000. This feature, disabled by default after hardware reset or power-up (but not a software reset), can be enabled or disabled at any time through the SPI interface. When enabled, it affects both read and write SPI transactions.

All SPI transactions without CRC are 4 bytes long. When CRC is enabled, all SPI transactions become 5 bytes long.

For an SPI write transaction, the host appends a correct CRC, calculated from the 4 bytes of that SPI transaction. The MAX22000 checks the CRC and flags a CRC error should there be a mismatch.

During an SPI read transaction, the MAX22000 expects no CRC, so does not check for one. The MAX22000 appends a correct CRC, calculated from the first byte sent from the host (the address and R/W bit), followed by the 3 bytes of register content. It is up to the host to check the validity of this returned CRC.

SPI command format consists of a 7-bit register address, followed by a read/write bit, followed by 24 bits of data to read from or write to the register specified. The two possible SPI transaction formats are shown in Table 4 and Table 5.

When enabled, the CRC uses a polynomial based on 0x31 ($x^8 + x^5 + x^4 + x^0$). This CRC has the following properties:

- detects all errors involving an odd number of bits
- detects all double-bit errors
- detects an error burst of up to 8 bits
- calculates and checks the CRC based on the 32-bits that would have been sent were the CRC not enabled

Refer to AN27 for more details at: *https://www.maximintegrated.com/en/app-notes/index.mvp/id/27*.

CRC code parameters:

- Width = 8
- Polynomial = 0x31
- Input XOR = 0x00
- Output XOR = 0x00
- Input Reflected = True
- Output Reflected = True

CRC write example: To write 0x00_0F00 to register GEN_ CHNL_CTRL, the SPI transaction from the host would be 0x06_000F_0011.

CRC read transaction example: To read the default value from register GEN_CNFG, the SPI transaction from the host would be 0x05_XXXX_XXXX. The returned value from the MAX22000 would be 0x05_1000_00CB.

Table 4. SPI Transaction Format with CRC Disabled

BITS 31:25	BIT 24	BITS 23:0
Register Address	R/$\overline{W}$	24-bit Payload

Table 5. SPI Transaction Format with CRC Enabled

BITS 39:33	BIT 32	BITS 31:8	BITS 7:0
Register Address	R/$\overline{W}$	24-bit Payload	CRC

Product Tracking

The MAX22000 includes a 32-bit device tracking number, unique to each device manufactured, accessible through the SPI interface.

Besides tracking individual ICs, this feature can also enable tracking of individual products incorporating the MAX22000.

Analog Output DAC

The analog output is driven by a high accuracy 18-bit, serial SPI input, digital-to-analog converter (DAC).

At power-up, the output is set to high-impedance. If subsequently programmed to switch to AOVM mode, the output goes to approximately 0V. If subsequently programmed to switch to AOCM mode, the output goes to approximately 0mA.

One of the settings, the +25V mode, is meant to support HART or to source power for a 4mA–20mA sensor. As described later, the MAX22000 supports either a signal from a HART modem through the HART_IN pin, or the DAC can generate HART modulation directly through the firmware.

Output Correction

To ease system calibration, the MAX22000 corrects DAC codes with an 18-bit gain and an 18-bit offset adjustment, as shown in Figure 4.

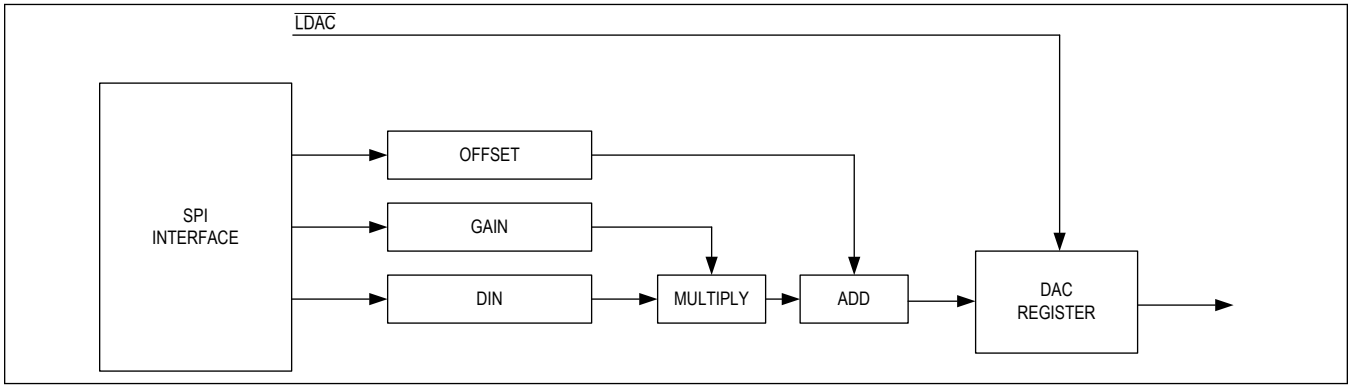


Figure 4. Gain and Offset Adjustment

The DAC code written to AO_DATA_W (in the AO_DATA_ WR register) is a signed two's complement value. Thus, a code of 0x00000 results in a nominal zero voltage or current, a code of 0x20000 results in the most negative voltage or current, and a code of 0x1FFFF results in the most positive voltage or current output. Details about the code-to-output mapping can be seen in Table 6.

Though AO_DATA_W is always interpreted as a signed two's complement value, the 25V mode adds a fixed 25V offset to the analog output, effectively making it positive-only. In the 25V mode case, programmed voltages might be restricted due to HVDDO headroom restrictions.

The gain coefficient, AO_GAIN_W, is always an unsigned 18-bit binary code, representing a gain between 1 LSB, and one unity gain. Table 7 summarizes the gain correction range of the MAX22000, where the last columns specify the gain as shown in Figure 4.

The offset coefficient, AO_OFFSET_W, is always a signed two's complement 18-bit code, representing an offset between about positive half-scale and negative half-scale. Table 8 summarizes the offset correction range of the MAX22000.

The results of the correction calculations can saturate. Should the correction calculations result in overflow or underflow, the code clips to the appropriate level. For 25V AOVM, the saturation calculations are the same as with ±12.5V AOVM, with an additional 25V offset added after the output voltage is calculated.

Writing to any of the AO_DATA_WR, AO_GAIN_CORR_ WR, or AO_OFFSET_CORR_WR registers results in a recalculation of the corrected output code as shown in Figure 4, and updates the analog output once the calculations have completed.

Table 6. Nominal Output Values vs. Code

MODE	SETTING	AO_DATA_W	OUTPUT VALUE
AOVM	+25V	0x20000	12.5V
		0x3FFFF	24.9999V
		0x00000	25.0V
		0x1FFFF	37.4999V
	±12.5V	0x20000	-12.5V
		0x3FFFF	-95.4µV
		0x00000	0V
		0x1FFFF	12.4999V
AOCM	±25mA	0x20000	-25mA
		0x3FFFF	-191nA
		0x00000	0mA
		0x1FFFF	24.9998mA
	±2.5mA	0x20000	-2.5mA
		0x3FFFF	-19.1nA
		0x00000	0mA
		0x1FFFF	2.49998mA

Table 7. Gain Range Examples

RANGE	AO_GAIN_W	GAIN	AS A DECIMAL
Minimum Gain	0x00000	$1/2^{18}$	0.0000038
Quarter Gain	0x0FFFF	1/4	0.25
Half Gain	0x1FFFF	1/2	0.50
Three-Quarters Gain	0x2FFFF	3/4	.75
Maximum Gain	0x3FFFF	1	1.00

Table 8. Offset Range Examples

MODE	SETTING	AO_DATA_W	OFFSET FRACTION	OUTPUT VALUE
AOVM	+25V	0x20000	-1	12.5V
		0x3FFFF	-1 / 131072	24.9999V
		0x00000	0	25.0V
		0x1FFFF	131071 / 131072	37.4999V
	±12.5V	0x20000	-1	-12.5V
		0x3FFFF	-1 / 131072	-95.4µV
		0x00000	0	0V
		0x1FFFF	131071 / 131072	12.4999V
AOCM	±25mA	0x20000	-1	-25mA
		0x3FFFF	-1 / 131072	-191nA
		0x00000	0	0mA
		0x1FFFF	131071 / 131072	24.9998mA
	±2.5mA	0x20000	-1	-2.5mA
		0x3FFFF	-1 / 131072	-19.1nA
		0x00000	0	0mA
		0x1FFFF	131071 / 131072	2.49998mA

Controlling the Analog Output with $\overline{\text{LDAC}}$

The $\overline{\text{LDAC}}$ pin controls the latch between the corrected digital code and the DAC, and can help time analog output changes precisely.

If precise timing is not needed, the simplest approach would be to leave $\overline{\text{LDAC}}$ tied permanently low. Writing to AO_DATA_WR, AO_OFFSET_CORR_WR, or AO_ GAIN_CORR_WR starts a correction calculation. The MAX22000 provides a new output once these calculations complete. Likewise, transitioning $\overline{\text{LDAC}}$ from high to low after one of these registers is written, also provides a new output, even if $\overline{\text{LDAC}}$ transitions high again before correction calculations have completed.

For more precise timing control, keep $\overline{\text{LDAC}}$ high, and transition low after correction calculations have completed. The analog output updates coincide with this falling edge. To determine when the calculations have completed, either wait at least 2.5µs after completion of the SPI transaction writing one of the registers specified above, or poll the BUSY bit in the AO_STA_RD register waiting for it to read low.

Conversion Formulas

Table 9 collects together in one place, the formulas mapping DAC data, gain, and offset codes to nominal output values. Recall that the calculation in brackets can saturate, so overflows and underflows limit to the maximum and minimum digital codes, respectively.

The MAX22000 limits digital gain correction to 1.0 or below. Commonly, applications need a small gain correction above or below unity. To allow for this, the MAX22000 output driver provides an analog gain of approximately 1.02, allowing for a small correction above 1.0 if needed.

Table 9. Converting from DAC Code to Analog Output

MODE	SETTING	FORMULA
AOVM	+25V	$V_{OUT} = 12.5V \times \left[\frac{AO_DATA_W}{2^{17}} \times \frac{AO_GAIN_W + 1}{2^{18}} + \frac{AO_OFFSET_W}{2^{17}}\right] + 25V$
AOVM	±12.5V	$V_{OUT} = 12.5V \times \left[\frac{AO_DATA_W}{2^{17}} \times \frac{AO_GAIN_W + 1}{2^{18}} + \frac{AO_OFFSET_W}{2^{17}}\right]$
AOCM	±25mA	$I_{OUT} = 25mA \times \left[\frac{AO_DATA_W}{2^{17}} \times \frac{AO_GAIN_W + 1}{2^{18}} + \frac{AO_OFFSET_W}{2^{17}}\right]$
AOCM	±2.5mA	$I_{OUT} = 2.5mA \times \left[\frac{AO_DATA_W}{2^{17}} \times \frac{AO_GAIN_W + 1}{2^{18}} + \frac{AO_OFFSET_W}{2^{17}}\right]$

Analog Output DAC Ground

As shown in Figure 5, connect both AGND_DAC pins together. Refer remote output loads to this system ground for best performance.

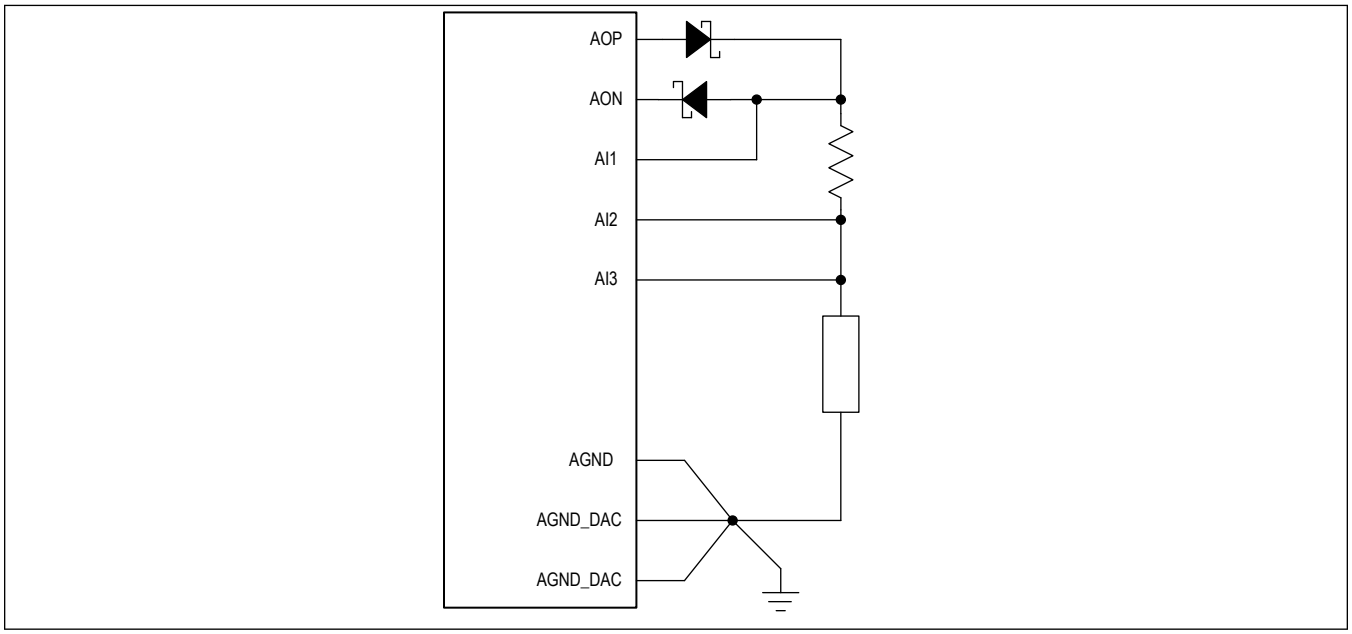


Figure 5. Star Ground Connection

HART (Highway Addressable Remote Transducer) Modulation

The MAX22000 supports HART devices in two ways. First, program a microcontroller to provide DAC samples, through the SPI interface, emulating the 1.2kHz and 2.2kHz sine waves characteristic of HART, following the correct format. Read ADC samples, also through the SPI interface, to demodulate the HART signal and recover the HART data. This technique requires no additional hardware, placing the burden of the HART interface implementation in the digital domain.

Alternatively, use an external HART modem. Couple the output of that modem to the MAX22000 HART_IN pin with a DC blocking network, as shown in Figure 6. Ensure that the high-pass cutoff frequency is approximately 100Hz or below.

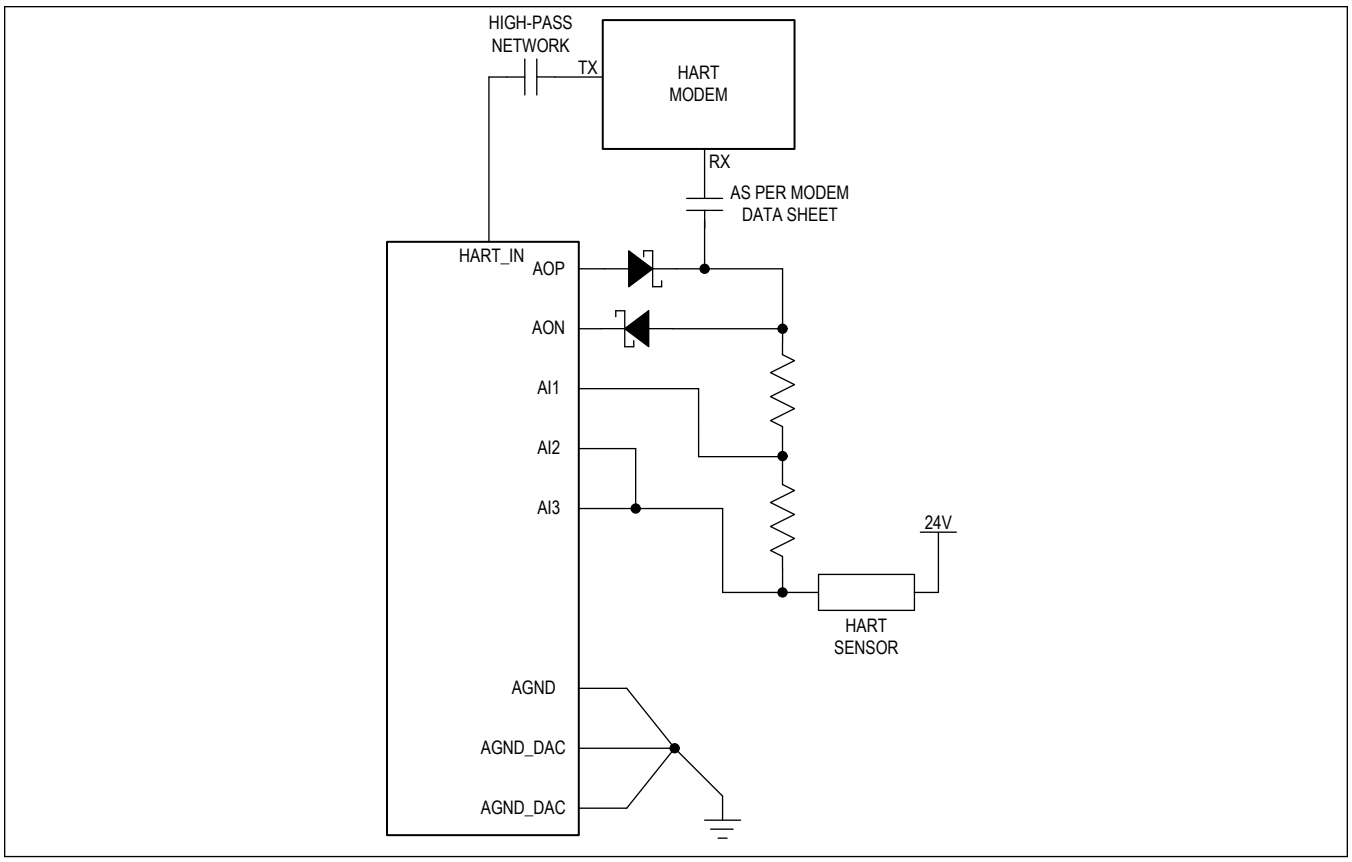


Figure 6. HART Connection

In AOVM mode, the gain from the HART_IN pin to the output is five, so a 1V peak-to-peak input results in a 5V peak-to-peak output swing.

In AOCM mode, the transconductance, assuming a 50Ω current sense resistor, is 10mA/V, so a 1V peak-to-peak input results in a 10mA peak-to-peak output swing.

Due to analog output headroom requirements, HVDD and HVDDO must be at least 26.5V for the 24V output mode. Also, HVSS and HVSSO must be -5V or more negative.

Output Driver Compensation

A passive network between the output driver and the FB pin compensates for load variations.

Figure 7 shows a recommended compensation network offering stable performance over a wide range of resistive and capacitive loads in AOVM mode, and a wide range or resistive and inductive loads in AOCM mode.

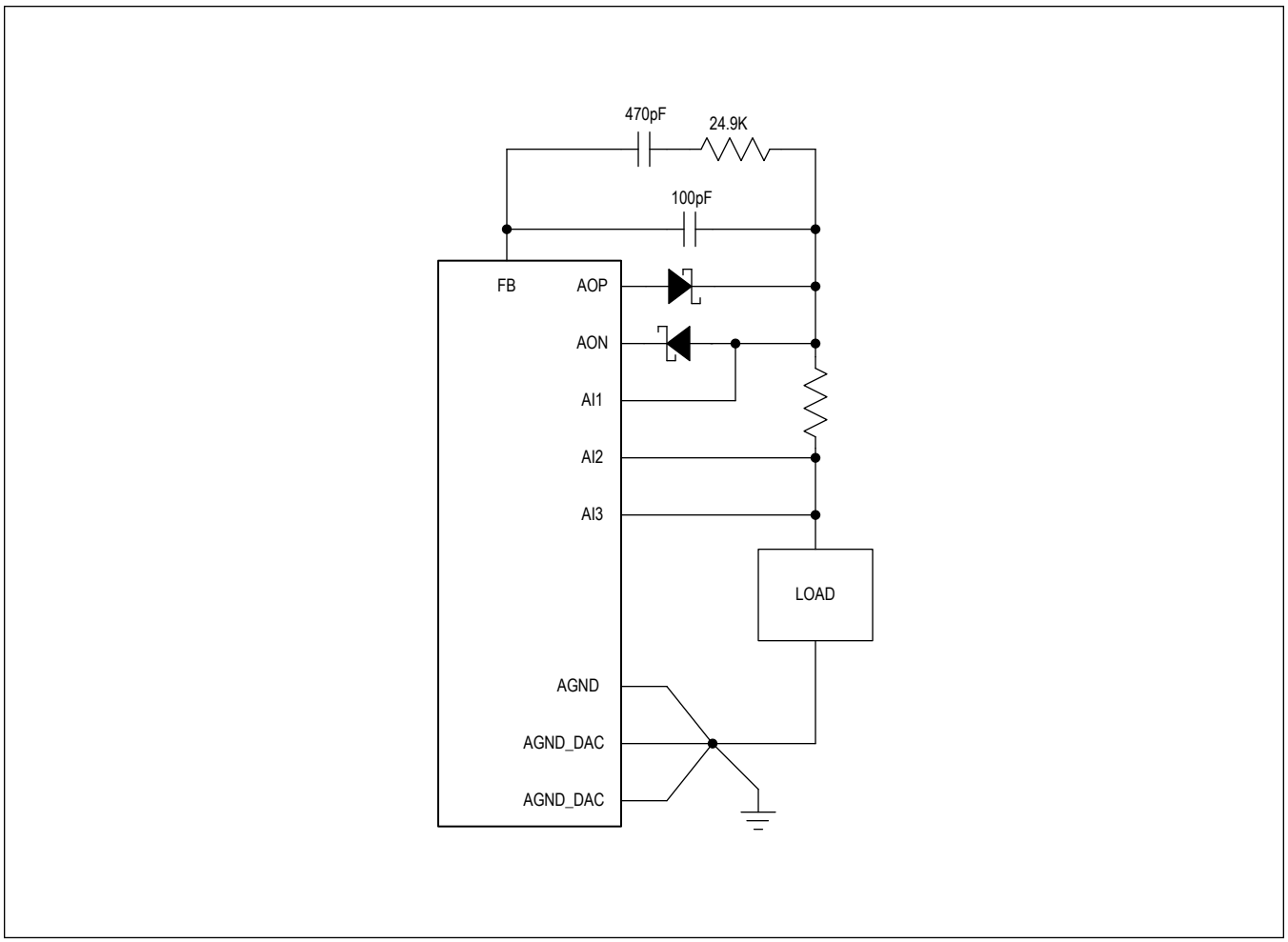


Figure 7. Recommended Compensation Network

Analog Input ADC

The MAX22000 features a high-performance, 24-bit delta-sigma analog-to-digital (ADC) converter, achieving exceptional performance while consuming minimal power. This ADC provides a selection of sample rates from 1sps up to 115.2ksps.

The delta-sigma modulator detects overrange conditions. The DOR bit in the DCHNL_STA register reports any such condition should it occur.

Post-conversion digital SINC filters provide better than 75dB 50Hz/60Hz normal mode rejection, and also provide overflow reporting. When an overflow occurs, the code returned is either 0x7FFFFF if positive overflow occurs, or 0x800000 if negative underflow occurs.

The MAX22000 also monitors the analog signals entering the ADC and reports an overrange condition in bit AOR in the DCHNL_STA register if the input to the ADC exceeds the full-scale range by approximately 120% or more. These conversions can result in nonsaturated digital codes, which might not meet the accuracy specifications in this data sheet.

ADC Clock

The MAX22000 incorporates a highly stable internal oscillator, providing a nominal system clock of 7.3728MHz (8.192MHz x 0.9) for both analog and digital timing. A highly stable external clock can be provided to synchronize ADC conversions across multiple MAX22000 using the SYNC pin. Set the EXTCLK bit in the DCHNL_CTRL2 register to 1 to use a clock source provided on the CLK pin. Provide only a 7.3728MHz frequency to meet filter requirements. Connect

CLK to DGND if unused and set the EXTCLK bit in DCHNL_CTRL2 register to 0 to select an internal clock source. Refer to the *ADC Conversion Synchronization* section for further information on use of the SYNC pin.

Analog Inputs

An internal multiplexer (MUX), controlled through the AI_DCHNL_ SEL[3:0] bits in the GEN_CHNL_CTRL register, selects from 11 available sources. Both single-ended and differential sources are available through this MUX, as detailed in Table 13.

For most MUX selections, a minimum voltage results in a converted code of 0x800000, a zero voltage results in a converted code of 0x000000, and a maximum voltage results in a converted code of 0x7FFFFF.

The exception to this are the AUX1 and AUX2 inputs, where an input of zero volts results in a converted code of 0x800000, an input of +1.25V results in a converted code of 0x000000, and an input of +2.5V results in a converted code of 0x7FFFFF.

ADC Operating Modes

The DCHNL_MODE bits in the DCHNL_CMD register control whether ADC conversions occur. By default, at power-up, the ADC is in a standby power-down mode (0b01), performing no conversions and minimizing ADC power consumption.

Writing 0b01 to the DCHNL_MODE bits in the DCHNL_ CMD register powers down the MAX22000 ADC. If the DCHNL_PD bit of the DCHNL_CTRL1 register is set low, then the MAX22000 ADC enters a standby mode, where conversions stop, but the internal LDO and oscillator are still powered, enabling fast startup. If the DCHNL_PD bit is set high, the ADC is reset.

To convert data through the ADC, write 0b11 to the DCHNL_MODE bits. This triggers either a single conversion or starts a continuous series of conversions, depending on the state of the SCYCLE and CONTSC bits in the DCHNL_CTRL1 register.

Set the DCHNL_MODE bits to 0b01 before making any changes to the ADC settings, as well as gain and offset calibration coefficients.

Select the conversion mode based on conversion latency and MUX usage.

If focusing on a single source of analog data with fast transients, choose continuous conversion mode. Select this mode by setting the SCYCLE bit in the DCHNL_CTRL1 register low before starting conversions. It yields the highest conversion rates possible, up to 115.2ksps. In this mode, depending on the selected conversion rate, received data has an initial filter settling of 5 samples. Refer to Table 10 for a menu of conversion rates.

Similar to continuous conversion mode, continuous single-cycle mode provides an on-going stream of samples, but bypasses the filter settling delay. Select this mode by setting the SCYCLE bit high and the CONTSC bit also high (both in the DCHNL_ CTRL1 register). It provides continuous conversions with no added latency, bypassing the pipeline delay of continuous conversion mode. Refer to Table 11 for a menu of conversion rates.

To provide on-demand conversions, consider single-cycle mode, offering a single no-latency conversion, but otherwise similar to continuous single-cycle mode. Select this mode by setting the SCYCLE bit high and the CONTSC bit low. Refer to Table 12 for maximum possible data rates in this mode.

When in either continuous conversion mode or continuous single-cycle mode, halt the conversions by setting the DCHNL_MODE bits in the DCHNL_CMD register to 0b01. Changing the MUX selection to a different source (AI_DCHNL_SEL bits in the GEN_CHNL_CTRL register) also halts continuous conversions and switches the ADC to standby.

Table 10. Data Rate Choices for Continuous Conversion

DCHNL_RATE [3:0]	DATA RATE (SPS)	DCHNL_RATE [3:0]	DATA RATE (SPS)
0b0000	**5**	0b1000	900
0b0001	**10**	0b1001	1,800
0b0010	**15**	0b1010	3,600
0b0011	**30**	0b1011	7,200
0b0100	**50**	0b1100	14,400
0b0101	**60**	0b1101	28,800
0b0110	225	0b1110	57,600
0b0111	450	0b1111	115,200*

** Disable all system calibrations to achieve this sampling rate.*

***Note**: Bold represents sampling rates that provide more than 90dB of 50Hz/60Hz normal mode rejection.*

Table 11. Data Rate Choices for Continuous Single-Cycle Conversion

DCHNL_RATE [3:0]	DATA RATE WITH SYSTEM CALIBRATION (SPS)	DATA RATE WITHOUT SYSTEM CALIBRATION (SPS)
0b0000	**1 (0.9955)**	**1 (0.9955)**
0b0001	**2.5**	**2.5**
0b0010	**5**	**5**
0b0011	**10**	**10**
0b0100	**12.5**	**12.5**
0b0101	**15**	**15**
0b0110	50	50
0b0111	60	60
0b1000	150	150
0b1001	299	299
0b1010	887	892
0b1011	1,755	1,776
0b1100	2,768	2,818
0b1101	5,327	5,519
0b1110	9,910	10,593
0b1111	17,389	19,609

***Note**: Bold represents sampling rates that provide more than 90dB of 50Hz/60Hz normal mode rejection.*

Table 12. Data Rate Choices for Single-Cycle Conversion

DCHNL_RATE [3:0]	DATA RATE WITH SYSTEM CALIBRATION (SPS)	DATA RATE WITHOUT SYSTEM CALIBRATION (SPS)
0b0000	**1 (0.9955)**	**1 (0.9955)**
0b0001	**2.5**	**2.5**
0b0010	**5**	**5**
0b0011	**10**	**10**
0b0100	**12.5**	**12.5**
0b0101	**15**	**15**
0b0110	50	50
0b0111	60	60
0b1000	150	150
0b1001	298	299
0b1010	886	891
0b1011	1,752	1,772
0b1100	2,759	2,810
0b1101	5,297	5,486
0b1110	9,804	10,473
0b1111	17,067	19,200

***Note**: Bold represents sampling rates that provide more than 90dB of 50Hz/60Hz normal mode rejection.*

Data Rates

Table 10, Table 11, and Table 12 summarize the available sampling rates of the MAX22000. Use the appropriate table depending on the conversion mode selected. In each case, the left-most column of the table indicates what to write to the DCHNL_RATE bits of the DCHNL_CMD register. In all 3 tables, the sampling rates in bold represent those that provide more than 90dB of 50Hz/60Hz normal mode rejection.

To achieve the highest possible sampling rate in Table 10, 115.2ksps in continuous sampling mode, system calibrations must first be disabled by setting both the NOSYSG and the NOSYSO bits in the DCHNL_CTRL2 register to 1. If either of these bits are zero, the sampling rate is instead 57.6ksps. The RATE bits in the DCHNL_STA register do not reflect this.

ADC Data Ready Output ($\overline{RDY}$)

The $\overline{RDY}$ pin indicates the availability of an ADC conversion result. A new conversion result always triggers a falling edge on $\overline{RDY}$. A valid read of the DCHNL_DATA register causes a rising edge on $\overline{RDY}$ if it is low. In continuous conversion mode or continuous single-cycle mode, a new conversion result might become available before the previous one had been read. In this case, the MAX22000 transitions the $\overline{RDY}$ pin high approximately 0.5µs prior to indicating that new conversion result with a falling edge.

Existing conversion results remain available until about 0.5µs before the next conversion result. In continuous mode, $\overline{RDY}$ initially remains high for the first four conversion results, then goes low for the fifth result. See Figure 8 for more detailed $\overline{RDY}$ timing.

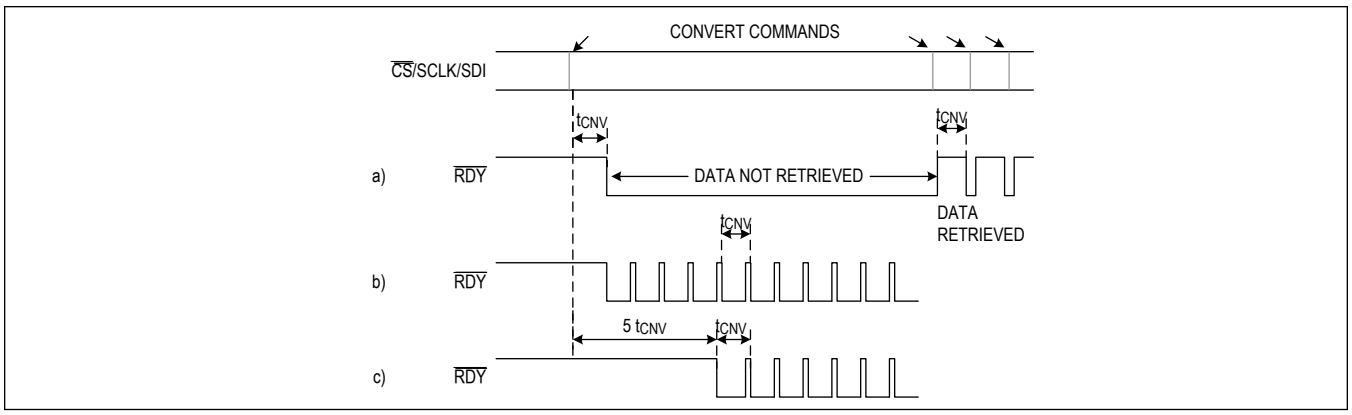


Figure 8. RDY Output Timing, a) Single-Cycle Mode, b) Continuous Single-Cycle Mode, c) Continuous Conversion Mode

ADC Conversion Synchronization

The SYNC pin—ideally in conjunction with an external clock—can be used to synchronize the data conversions to external events. Although the synchronization method also works with an internal clock, resynchronization is inevitable due to local oscillators with limited frequency accuracy. A highly stable external clock that can be shared by multiple MAX22000 devices, allows for much longer time intervals without the requirement of resynchronization.

Set bit SYNC_MODE in register DCHNL_CTRL2 to logic high to enable external synchronization mode. Optionally, set bit EXTCLK in register DCHNL_CTRL2 to logic high to use a highly accurate external clock signal.

The synchronization mode is used to detect if the current conversions are synchronized to a continuous pulse signal with a period greater than the data rate. The pulse width of the synchronization signal is not critical, as only the rising edge of the synchronization pulse is used as a timing reference. The pulse width, however, must be longer than 300ns if the internal clock source is used, and longer than twice the clock period if an external clock source is used. In addition, the low time of the SYNC signal between consecutive SYNC pulses must be longer than 300ns if the internal clock source is used, and longer than twice the clock period if an external clock source is used. Ideally, the frequency of the synchronization signal is an integer multiple of the conversion rate. The synchronization mode records the number of ADC clock cycles between a falling edge of $\overline{RDY}$ and the rising edge of the next SYNC pulse. At the following SYNC pulse, the number of ADC clock cycles between a falling edge of $\overline{RDY}$ and the rising edge of the SYNC pulse is evaluated again and compared to the recorded value. If the new number of ADC clock cycles differs by more than one from the recorded value, the conversion in progress is stopped, the digital filter content is reset, and a new conversion starts. As the digital filter is reset, the full digital filter latency is required before valid results are available. If the new ADC clock count is within the ±1 count limit, the conversions continue uninterrupted.

Figure 9 shows the timing relationship between the MAX22000 ADC clock and the SYNC signal. Due to startup delays, any SYNC pulses before the first falling edge of $\overline{RDY}$ are ignored. The first rising edge on the SYNC pin after a falling edge of $\overline{RDY}$ establishes the relationship between the SYNC signal and the conversion timing.

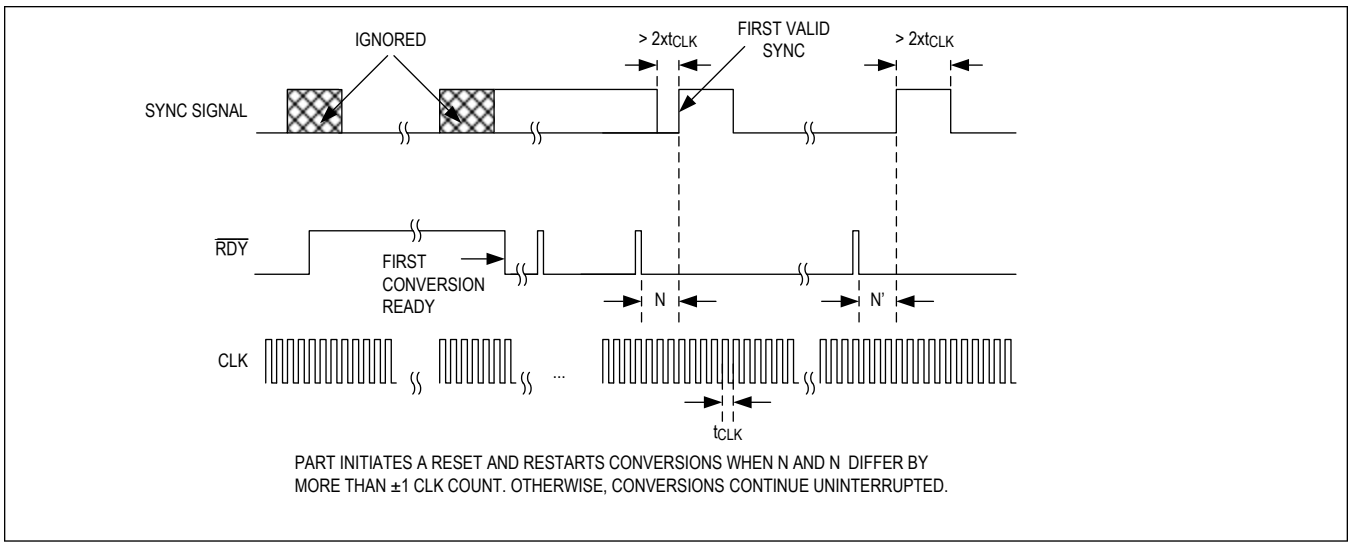


Figure 9. SYNC Input Timing

Analog Input System Calibration

The MAX22000 can eliminate gain and offset errors of the entire analog input signal chain, including board-level components, as well as internal MAX22000 circuits. The MAX22000 stores unique calibration coefficients for each of the available input channels, as selected by the AI_DCHNL_SEL bits in the GEN_CHNL_CTRL register. This simplifies calibration, as the coefficients need only be loaded once after reset or power-up. The MAX22000 automatically uses the appropriate coefficients on-the-fly. The MAX22000 supports automatic gain and offset correction in hardware for all conversion modes except for continuous conversion at 115,200 samples per second. Before this two-point calibration can take effect, the user must:

- Select two voltages near the application's full-scale maximum and minimum points for each selected channel used.
- Ensure that the calibration parameters for that channel are set to defaults.
- Apply these two voltages to the MAX22000, resulting in two codes.
- Calculate the gain and offset corrections for this channel.
- Format these for the MAX22000 gain and offset correction registers.
- Write these parameters to the appropriate registers, and repeat for any other channels being calibrated.

Select two test voltages near the application maximum and minimum. Supply them from a low noise source, and measure them with an accurate meter.

The MAX22000 employs indirect addressing to provide access to the offset and gain registers associated with each unique input channel. First, write the desired channel to the DCHNL_N_SEL register. Then, access calibration values with reads and writes to the DCHNL_N_SOC register for the offset, and the DCHNL_N_SGC for the gain.

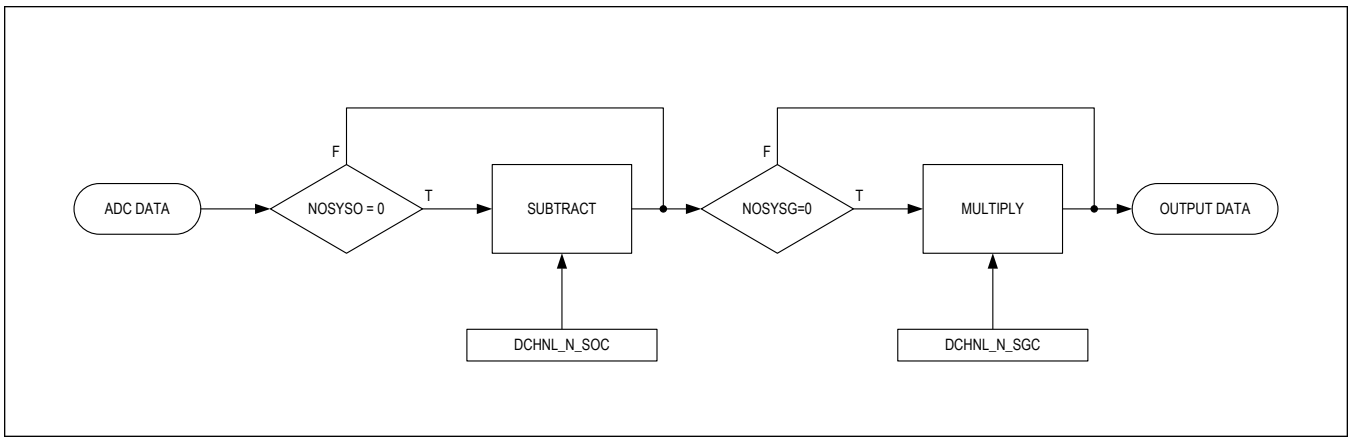


Figure 10. ADC System Calibration Data Flow

The offset and gain values must be at their defaults when the test voltages are applied. The defaults are 0x000000 for the offset and 0xC00000 for the gain of 1.5. Also, the NOSYSG and the NOSYSO bits in the DCHNL_CTRL2 register must both be at their default 0.

As illustrated in Figure 11, apply two test voltages, perform a conversion on each, and record the returned codes. For V1 and V2, C1 and C2 are obtained.

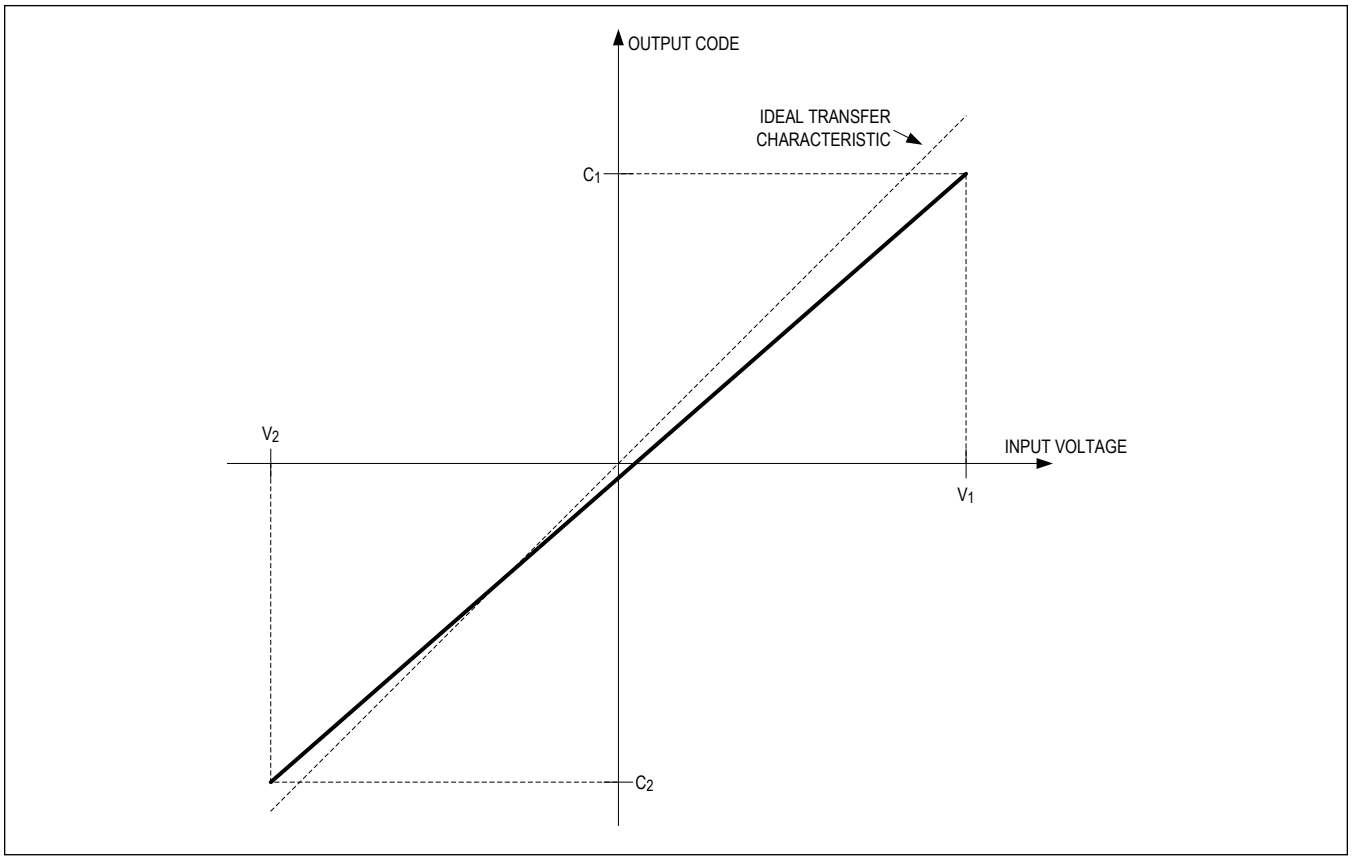


Figure 11. Definition of Parameters for Two-Point Calibration

Using the appropriate full-scale range voltage in Table 13, calculate the gain and offset as:

$$GAIN = 1.5 \times \frac{V_1 - V_2}{\left(\frac{C_1 - C_2}{2^{23}}\right) \times V_{FS}}$$

$$OFFSET = C_2 - \frac{1.5}{GAIN} \times \frac{V_2}{V_{FS}} \times 2^{23}$$

Since 0xC00000 is a gain of 1.5 our measured gain should be near 1.5. Calculate GAIN x 2^{23}. Write the rounded value of this in the DCHNL_N_SGC register as an unsigned number. For example, A = 1.48 translates to 12,415,139 (BD70A3h) in register DCHNL_N_SGC.

OFFSET is in bits, and can be either positive or negative. Using the appropriate digital gain entry in Table 13, calculate OFFSET/(ADIG x 1.5). Write this value in the DCHNL_N_SOC register as a two's complement number.

$$DCHNL_N_SGC = GAIN \times 2^{23}$$

$$DCHNL_N_SOC = \frac{OFFSET}{A_{DIG} \times 1.5}$$

The MAX22000 now corrects all further data from this channel using these associated correction parameters.

Table 13. Input Channel Conversion Parameters

AI_DCHNL_SEL[3:0]	INPUT CHANNEL	FULL-SCALE RANGE (V_{FS})	DIGITAL GAIN (A_{DIG})	VALUE FOR ADC CODE 0x800000	VALUE FOR ADC CODE 0x000000	VALUE FOR ADC CODE 0x7FFFFF
0b0000	None					
0b0001	AI1 Single Ended	12.5V	+2	-12.5V	0V	+12.5V
0b0010	AI2 Single Ended	12.5V	-2	-12.5V	0V	+12.5V
0b0011	AI1:AI2 Differential	1.25V	+2	-1.25V	0V	+1.25V
0b0100	AI3 Single Ended	12.5V	+2	-12.5V	0V	+12.5V
0b0101	AI4 Single Ended	12.5V	-2	-12.5V	0V	+12.5V
0b0110	AI3:AI4 Differential	25.0V	+1	-25.0V	0V	+25.0V
0b1001	AI5:AI6 Differential	25.0V	+1	-25.0V	0V	+25.0V
0b1100	AI5:AI6 Differential, AI5_DF_GAIN = 0b00	2.5V	+2	-2.5V	0V	+2.5V
0b1100	AI5:AI6 Differential, AI5_DF_GAIN = 0b01	500mV	+2	-500mV	0mV	+500mV
0b1100	AI5:AI6 Differential, AI5_DF_GAIN = 0b10	250mV	+2	-250mV	0mV	+250mV

Table 13. Input Channel Conversion Parameters (continued)

AI_DCHNL_SEL[3:0]	INPUT CHANNEL	FULL-SCALE RANGE (V_{FS})	DIGITAL GAIN (A_{DIG})	VALUE FOR ADC CODE 0x800000	VALUE FOR ADC CODE 0x000000	VALUE FOR ADC CODE 0x7FFFFF
0b1100	AI5:AI6 Differential, AI5_DF_GAIN = 0b11	125mV	+2	-125mV	0mV	+125mV
0b1101	AUX1 Single Ended	1.25V	+2	0V	+1.25V	+2.5V
0b1110	AUX2 Single Ended	1.25V	-2	0V	+1.25V	+2.5V
0b1111	AUX1:AUX2 Differential	2.5V	+1	-2.5V	0V	+2.5V

The data channel conversions do not need to be stopped while accessing the offset and gain correction registers. The ADC can be running or stopped. The channel whose correction parameters are being accessed cannot be the same as the channel actively being converted. The data channel keeps converting with one exception. A write to the offset or gain correction registers for a channel currently being converted aborts that conversion. Additionally, if the ADC is in either continuous conversion mode or continuous single-cycle mode, all further conversions are halted as well.

Either offset correction, gain correction, or both can be disabled with the NOSYSG and NOSYSO bits in the DCHNL_CTRL2 register, but these bits are global, and would prohibit calibration for all channels if activated. If gain correction is disabled, the MAX22000 behaves as if DCHNL_SGC is set to 0x800000. Note that this is 2/3 of the default gain correction value of 0xC00000. If offset correction is disabled, the MAX22000 behaves as if DCHNL_SOC is set to 0x000000.

Auxiliary ADC Inputs

The MAX22000 offers two auxiliary ADC inputs, AUX1 and AUX2. Both inputs can be used either as single-ended inputs with a 0V to 2.5V range, or as differential inputs, with a range of ±2.5V. Both inputs are high impedance, allowing for a wide range of source impedances without the need for a dedicated input buffer.

ADC Reference

The MAX22000 includes a built-in 2.5V reference, but can use external references under program control. The MAX22000 meets all electrical characteristic specifications using the internal precision reference. An external reference allows, for example, sharing one reference between multiple MAX22000.

ADC Software Reset

A software reset puts the DCHNL_ prefix registers to their default state and resets internal state machines. It does not affect the DAC.

To effect an ADC software reset:

- Write 1 to the DCHNL_PD bit in the DCHNL_CTRL1 register.
- Write 0b01 to the DCHNL_MODE bits in the DCHNL_ CMD register.
- Poll the PDSTAT bits in the DCHNL_STA register until it reads 0b10.

Hardware Reset

The MAX22000 features an active-low hardware reset. Pulse $\overline{RST}$ low to reconfigure all registers to their power-on state. The analog output goes in high impedance mode, all analog inputs are powered down, any ADC conversion in progress is stopped, and the digital filters are reset.

Thermal Monitoring and Shutdown

The MAX22000 monitors its own temperature, and provides both a thermal warning and a protective thermal shutdown.

The THWRNG_INT bit is set in the GEN_INT register, should the die temperature reach approximately 145°C. This bit remains set until the die temperature drops below approximately 135°C, at which point this bit clears. This high temperature warning condition can be programmed to cause an interrupt assertion on the $\overline{INT}$ pin.

Should the die temperature exceed approximately 165°C, the THSHDN_INT bit in the GEN_INT register asserts high and the $\overline{INT}$ pin asserts low, indicating a high temperature shutown condition. Note that thermal shutdown is a non-maskable interrupt. The GEN_CNFG and GEN_ CHNL_CTRL registers are reset to their default state, except for the DAC_REF_SEL, the ADC_REF_SEL, and the CRC_EN bits.

Register Map

Note: In the register map the top-most line represents the MSB byte (bits 23-16, the middle line represents the middle byte (bits 15-8), and the bottom line represents the LSB byte (bits 7-0).

ADDRESS	RESET	NAME	MSB							LSB
GEN Registers										
0x00	0x2D0000	GEN_PROD[23:16]	PROD_ID[7:0]							
		GEN_PROD[15:8]	SERIAL[15:8]							
		GEN_PROD[7:0]	SERIAL[7:0]							
0x01	0x020000	GEN_REV[23:16]	REV_ID[7:0]							
		GEN_REV[15:8]	SERIAL[15:8]							
		GEN_REV[7:0]	SERIAL[7:0]							
0x02	0x100000	GEN_CNFG[23:16]	CRC_EN	DACREF_SEL	ADCREF_SEL	LINE_CNFG	AO_CNFG[3:0]			
		GEN_CNFG[15:8]	AI1_2_CNFG[2:0]			AI3_CNFG	AI4_CNFG	AI5_6_CNFG[2:0]		
		GEN_CNFG[7:0]	AI5_DF_GAIN[1:0]		Reserved[1:0]		OVC_CTRL	Reserved[2:0]		
0x03	0x000000	GEN_CHNL_CTRL[23:16]	AI1_TEST[1:0]		AI2_TEST[1:0]		AI3_TEST[1:0]		AI4_TEST[1:0]	
		GEN_CHNL_CTRL[15:8]	AI5_TEST[1:0]		AI6_TEST[1:0]		AI_DCHNL_SEL[3:0]			
		GEN_CHNL_CTRL[7:0]	Reserved[7:0]							
0x04	0x000000	GEN_GPIO_CTRL[23:16]	Reserved[1:0]		GPIO_EN[5:0]					
		GEN_GPIO_CTRL[15:8]	Reserved[1:0]		GPIO_DIR[5:0]					
		GEN_GPIO_CTRL[7:0]	Reserved[1:0]		GPO_DATA[5:0]					
0x05	0x000000	GEN_GPI_INT[23:16]	Reserved[1:0]		GPI_POS_EDGE_INT[5:0]					
		GEN_GPI_INT[15:8]	Reserved[1:0]		GPI_NEG_EDGE_INT[5:0]					
		GEN_GPI_INT[7:0]	Reserved[7:0]							
0x06	0x000000	GEN_GPI_DATA[23:16]	Reserved[1:0]		GPI_POS_EDGE_INT_STA[5:0]					
		GEN_GPI_DATA[15:8]	Reserved[1:0]		GPI_NEG_EDGE_INT_STA[5:0]					
		GEN_GPI_DATA[7:0]	Reserved[1:0]		GPI_DATA[5:0]					

ADDRESS	RESET	NAME	MSB							LSB
0x07	0x000000	GEN_INT[23:16]	Reserved[14:7]							
		GEN_INT[15:8]	Reserved[6:0]							PGAOV_INT
		GEN_INT[7:0]	HVDD_INT	HVDDO_INT	THSHDN_INT	THWRNG_INT	OVC_INT	CNFG_INT	CRC_INT	GPI_INT
0x08	0x000000	GEN_INTEN[23:16]	Reserved[14:7]							
		GEN_INTEN[15:8]	Reserved[6:0]							PGAOV_INTEN
		GEN_INTEN[7:0]	HVDD_INTEN	HVDDO_INTEN	Reserved	THWRNG_INTEN	OVC_INTEN	CNFG_INTEN	CRC_INTEN	GPI_INTEN
0x09	0x000000	GEN_PWR_CTRL[23:16]	AODAC_PD	Reserved	AODAC_RST	Reserved	GEN_PD	Reserved	GEN_RST	Reserved[16]
		GEN_PWR_CTRL[15:8]	Reserved[15:8]							
		GEN_PWR_CTRL[7:0]	Reserved[7:0]							
DCHNL Registers										
0x20	0x100000	DCHNL_CMD[23:16]	Reserved[1:0]		DCHNL_MODE[1:0]		DCHNL_RATE[3:0]			
		DCHNL_CMD[15:8]	Reserved[15:8]							
		DCHNL_CMD[7:0]	Reserved[7:0]							
0x21	0x000008	DCHNL_STA[23:16]	Reserved[8:1]							
		DCHNL_STA[15:8]	Reserved[0]	REFDET	Reserved[3:0]				DOR	AOR
		DCHNL_STA[7:0]	RATE[3:0]				PDSTAT[1:0]		MSTAT	RDY
0x22	0x020000	DCHNL_CTRL1[23:16]	Reserved[2:0]			DCHNL_PD	Reserved[1:0]		SCYCLE	CONTSC
		DCHNL_CTRL1[15:8]	Reserved[15:8]							
		DCHNL_CTRL1[7:0]	Reserved[7:0]							
0x23	0x000000	DCHNL_CTRL2[23:16]	EXTCLK	Reserved	SYNC_MODE	Reserved	NOSYSG	NOSYSO	Reserved[17:16]	
		DCHNL_CTRL2[15:8]	Reserved[15:8]							
		DCHNL_CTRL2[7:0]	Reserved[7:0]							
0x24	0x000000	DCHNL_DATA[23:16]	DCHNL_DATA[23:16]							
		DCHNL_DATA[15:8]	DCHNL_DATA[15:8]							

ADDRESS	RESET	NAME	MSB							LSB
		DCHNL_DATA[7:0]	DCHNL_DATA[7:0]							
0x25	0x000000	DCHNL_N_SEL[23:16]	Reserved[19:12]							
		DCHNL_N_SEL[15:8]	Reserved[11:4]							
		DCHNL_N_SEL[7:0]	Reserved[3:0]				DCHNL_N_SEL[3:0]			
0x26	0x000000	DCHNL_N_SOC[23:16]	DCHNL_N_SOC[23:16]							
		DCHNL_N_SOC[15:8]	DCHNL_N_SOC[15:8]							
		DCHNL_N_SOC[7:0]	DCHNL_N_SOC[7:0]							
0x27	0xC00000	DCHNL_N_SGC[23:16]	DCHNL_N_SGC[23:16]							
		DCHNL_N_SGC[15:8]	DCHNL_N_SGC[15:8]							
		DCHNL_N_SGC[7:0]	DCHNL_N_SGC[7:0]							
AO Registers										
0x40	0x000000	AO_DATA_WR[23:16]	AO_DATA_W[17:10]							
		AO_DATA_WR[15:8]	AO_DATA_W[9:2]							
		AO_DATA_WR[7:0]	AO_DATA_W[1:0]				Reserved[5:0]			
0x41	0x000000	AO_OFFSET_CORR_WR[23:16]	AO_OFFSET_W[17:10]							
		AO_OFFSET_CORR_WR[15:8]	AO_OFFSET_W[9:2]							
		AO_OFFSET_CORR_WR[7:0]	AO_OFFSET_W[1:0]				Reserved[5:0]			
0x42	0xFFFFC0	AO_GAIN_CORR_WR[23:16]	AO_GAIN_W[17:10]							
		AO_GAIN_CORR_WR[15:8]	AO_GAIN_W[9:2]							
		AO_GAIN_CORR_WR[7:0]	AO_GAIN_W[1:0]				Reserved[5:0]			
0x43	0x000000	AO_CNFG_WR[23:16]	Reserved[3:0]				AO_RB_EN	Reserved[18:16]		
		AO_CNFG_WR[15:8]	Reserved[15:8]							
		AO_CNFG_WR[7:0]	Reserved[7:0]							

ADDRESS	RESET	NAME	MSB							LSB
0x44	0x000000	AO_DATA_RD[23:16]	Reserved[5:0]						AO_DATA_R[17:16]	
		AO_DATA_RD[15:8]	AO_DATA_R[15:8]							
		AO_DATA_RD[7:0]	AO_DATA_R[7:0]							
0x45	0x000000	AO_OFFSET_CORR_RD[23:16]	Reserved[5:0]						AO_OFFSET_R[17:16]	
		AO_OFFSET_CORR_RD[15:8]	AO_OFFSET_R[15:8]							
		AO_OFFSET_CORR_RD[7:0]	AO_OFFSET_R[7:0]							
0x46	0x03FFFF	AO_GAIN_CORR_RD[23:16]	Reserved[5:0]						AO_GAIN_R[17:16]	
		AO_GAIN_CORR_RD[15:8]	AO_GAIN_R[15:8]							
		AO_GAIN_CORR_RD[7:0]	AO_GAIN_R[7:0]							
0x47	0x000000	AO_STA_RD[23:16]	Reserved[10:3]							
		AO_STA_RD[15:8]	Reserved[2:0]			BUSY	Reserved[11:8]			
		AO_STA_RD[7:0]	Reserved[7:0]							

Register Details

GEN_PROD (0x00)

BIT	23	22	21	20	19	18	17	16
Field	PROD_ID[7:0]							
Reset	0x2D							
Access Type	Read Only							

BIT	15	14	13	12	11	10	9	8
Field	SERIAL[15:8]							
Reset	0xXXXX							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	SERIAL[7:0]							
Reset	0xXXXX							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
PROD_ID	23:16	PROD_ID. MAX22000 identification code PROD_ID[7:5]: Number of output channels PROD_ID[4:1]: Number of input channels PROD_ID[0]: RTD/TC support
SERIAL	15:0	SERIAL. Most significant 16 bits of a 32-bit code unique to each MAX22000

GEN_REV (0x01)

BIT	23	22	21	20	19	18	17	16
Field	REV_ID[7:0]							
Reset	0x02							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	SERIAL[15:8]							
Reset	0xXXXX							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	SERIAL[7:0]							
Reset	0xXXXX							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
REV_ID	23:16	REV_ID. Unique ID incremented with each die revision of the MAX22000
SERIAL	15:0	SERIAL. Least significant 16 bits of a 32-bit code unique to each MAX22000

GEN_CNFG (0x02)

BIT	23	22	21	20	19	18	17	16
Field	CRC_EN	DACREF_SEL	ADCREF_SEL	LINE_CNFG	AO_CNFG[3:0]			
Reset	0b0	0b0	0b0	0b1	0b0000			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			
BIT	15	14	13	12	11	10	9	8
Field	AI1_2_CNFG[2:0]			AI3_CNFG	AI4_CNFG	AI5_6_CNFG[2:0]		
Reset	0b000			0b0	0b0	0b000		
Access Type	Write, Read			Write, Read	Write, Read	Write, Read		

BIT	7	6	5	4	3	2	1	0
Field	AI5_DF_GAIN[1:0]		Reserved[1:0]		OVC_CTRL	Reserved[2:0]		
Reset	0b00		0b00		0b0	0b000		
Access Type	Write, Read		Read Only		Write, Read	Read Only		

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_EN	23	CRC_EN. CRC generator and checker enable	0: CRC disabled (default) 1: CRC enabled
DACREF_SEL	22	DACREF_SEL. DAC reference source	0: DAC uses a built-in voltage reference (default) 1: DAC uses reference provided on pin REF_DAC_EXT
ADCREF_SEL	21	ADCREF_SEL. ADC reference source	0: ADC uses a built-in voltage reference (default) 1: ADC uses reference provided on pin REF_ADC_EXT **Note**: A write transaction that changes this bit aborts any ADC conversion in progress
LINE_CNFG	20	LINE_CNFG. Line configuration safety switch	0: Switch between AI2 and AI3 is open 1: Switch between AI2 and AI3 is closed, ensuring a feedback path for analog output feedback, irrespective of the external configuration (default)
AO_CNFG	19:16	AO_CNFG. Analog output configuration	0000: High Impedance (default) 0001: Analog output voltage mode, 25V setting 0010: Analog output voltage mode, 12.5V setting 0011: Reserved 0100: Reserved 0101: Reserved 0110: Analog output current mode, 25mA setting 0111: Reserved 1000: Analog output current mode, 2.5mA setting 1001: Reserved 1010 through 1111: Writing these values is ignored, the current field value remains unchanged, and the CNFG_INT bit is set active high to indicate an invalid write attempt
AI1_2_CNFG	15:13	AI1_2_CNFG. AI1 and AI2 input configuration	000: Both AI1 and AI2 powered down (default) 001: AI1 single-ended, AI2 powered down 010: AI1 powered down, AI2 single-ended 011: Both AI1 and AI2 single-ended 100: AI1 and AI2 differential pair (CSA) 101 through 111: Writing these values is ignored, the current field value remains unchanged, and the CNFG_INT bit is set active high to indicate an invalid write attempt **Note**: Selecting any current output mode in AO_CNFG [3:0] (0b0110 or 0b1000) forces AI2_2_CNFG [2:0] to be set to 0b100, and reads back as 0b100, regardless of what the write transaction specifies for these bits. Additionally, if the write transaction specifies anything other than 0b100, the CNFG_INT bit is set active high to indicate an invalid write attempt

BITFIELD	BITS	DESCRIPTION	DECODE
AI3_CNFG	12	AI3_CNFG. AI3 input configuration	0: Powered down (default) 1: Single-ended **Note**: Selecting any voltage output mode in AO_CNFG [3:0] (0b0001 or 0b0010) forces AI3_CNFG to be set to 0b1, and reads back as 0b1, regardless of what the write transaction specifies for this bit. Additionally, if the write transaction specifies anything other than 0b1, the CNFG_INT bit is set active high to indicate an invalid write attempt
AI4_CNFG	11	AI4_CNFG. AI4 input configuration	0: Powered down (default) 1: Single-ended
AI5_6_CNFG	10:8	AI5_6_CNFG. AI5 and AI6 input configuration	000: Powered down (default) 001: Reserved 010: Reserved 011: Reserved 100: AI5 and AI6 differential pair (PGA) 101 through 111: Writing these values is ignored, the current field value remains unchanged, and the CNFG_INT bit is set active high to indicate an invalid write attempt
AI5_DF_GAIN	7:6	AI5_DF_GAIN. AI5 and AI6 differential input voltage range setting	00: 12.5V setting if AI_DCHNL_SEL [3:0] is 0b1001 (default) 2.5V setting if AI_DCHNL_SEL [3] = 0b1100 (default) 01: 500mV setting 10: 250mV setting 11: 125mV setting
Reserved	5:4	Reserved. Reserved	
OVC_CTRL	3	OVC_CTRL. Over-current response control, AOVM mode only	0: Automatic mode: an overcurrent condition sets the output in high impedance mode, and retries every 6ms until the overcurrent condition is removed, after which it automatically returns to the output mode it was in before the overcurrent condition began (default) 1: Host-controlled mode: an overcurrent condition sets the output in high impedance mode and resets the AO_CNFG [3:0] to 0b0000; The MAX22000 output then remains in high impedance until bits AO_CNFG [3:0] are written with a proper configuration.
Reserved	2:0	Reserved. Reserved	

GEN_CHNL_CTRL (0x03)

BIT	23	22	21	20	19	18	17	16
Field	AI1_TEST[1:0]		AI2_TEST[1:0]		AI3_TEST[1:0]		AI4_TEST[1:0]	
Reset	0b00		0b00		0b00		0b00	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BIT	15	14	13	12	11	10	9	8
Field	AI5_TEST[1:0]		AI6_TEST[1:0]		AI_DCHNL_SEL[3:0]			
Reset	0b00		0b00		0x0			
Access Type	Write, Read		Write, Read		Write, Read			

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AI1_TEST	23:22	AI1_TEST. AI1 diagnostic switches	00: Diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND
AI2_TEST	21:20	AI2_TEST. AI2 diagnostic switches	00: Diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND
AI3_TEST	19:18	AI3_TEST. AI3 diagnostic switches	00: Diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND
AI4_TEST	17:16	AI4_TEST. AI4 diagnostic switches	00: Diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND
AI5_TEST	15:14	AI5_TEST. AI5 diagnostic switches	00: Diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND
AI6_TEST	13:12	AI6_TEST. AI6 diagnostic switches	00: Diagnostic switches disabled (default) 01: 2MΩ resistor to AGND 10: 2MΩ resistor to HVDD 11: 2MΩ resistor each to HVDD and AGND

BITFIELD	BITS	DESCRIPTION	DECODE
AI_DCHNL_SEL	11:8	AI_DCHNL_SEL. Analog input ADC channel selection	0000: No channel selected (default) 0001: AI1 single-ended (±12.5V conversion range) 0010: AI2 single-ended (±12.5V conversion range) 0011: AI1:AI2 differential (±1.25V conversion range, ±25mA if using a 50Ω resistor) 0100: AI3 single-ended (±12.5V conversion range) 0101: AI4 single-ended (±12.5V conversion range) 0110: AI3:AI4 differential (±25V conversion range) 0111: Reserved 1000: Reserved 1001: AI5:AI6 differential, 12.5V setting (±25V conversion range) 1010: Reserved 1011: Reserved 1100: AI5:AI6 differential, (±2.5V through ±125mV conversion range) 1101: AUX1 single-ended (0V to +2.5V conversion range) 1110: AUX2 single-ended (0V to +2.5V conversion range) 1111: AUX1:AUX2 differential (±2.5V conversion range) **Note:** Changing the value of these bits causes any ongoing ADC conversion to abort. Do not select settings marked as Reserved.
Reserved	7:0	Reserved. Reserved	

GEN_GPIO_CTRL (0x04)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[1:0]		GPIO_EN[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Write, Read					
BIT	15	14	13	12	11	10	9	8
Field	Reserved[1:0]		GPIO_DIR[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Write, Read					
BIT	7	6	5	4	3	2	1	0
Field	Reserved[1:0]		GPO_DATA[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:22	Reserved. Reserved	
GPIO_EN	21:16	GPIO_EN. GPIO port enable control for each GPIO pin	0: Corresponding GPIO pin disabled (default) 1: Corresponding GPIO pin enabled
Reserved	15:14	Reserved. Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
GPIO_DIR	13:8	GPIO_DIR. GPIO port direction control for each GPIO pin	0: Corresponding GPIO pin configured as an input (GPI) (default) 1: Corresponding GPIO pin configured as an output (GPO)
Reserved	7:6	Reserved. Reserved	
GPO_DATA	5:0	GPO_DATA. Data bits driven by GPIO pins configured as outputs	0: Corresponding output-configured GPIO pin drives a low logic level (default) 1: Corresponding output-configured GPIO pin drives a high logic level

GEN_GPI_INT (0x05)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[1:0]		GPI_POS_EDGE_INT[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Write, Read					

BIT	15	14	13	12	11	10	9	8
Field	Reserved[1:0]		GPI_NEG_EDGE_INT[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:22	Reserved. Reserved	
GPI_POS_EDGE_INT	21:16	GPI_POS_EDGE_INT. Positive edge detection control for GPIO pins configured as inputs	0: Positive edge detection disabled on the corresponding pin (default) 1: Positive edge detection enabled on the corresponding pin
Reserved	15:14	Reserved. Reserved	
GPI_NEG_EDGE_INT	13:8	GPI_NEG_EDGE_INT. Negative edge detection control for GPIO pins configured as inputs	0: Negative edge detection disabled on the corresponding pin (default) 1: Negative edge detection enabled on the corresponding pin
Reserved	7:0	Reserved. Reserved	

GEN_GPI_DATA (0x06)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[1:0]		GPI_POS_EDGE_INT_STA[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Read Clears All					

BIT	15	14	13	12	11	10	9	8
Field	Reserved[1:0]		GPI_NEG_EDGE_INT_STA[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Read Clears All					

BIT	7	6	5	4	3	2	1	0
Field	Reserved[1:0]		GPI_DATA[5:0]					
Reset	0x0		0x00					
Access Type	Read Only		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:22	Reserved. Reserved	
GPI_POS_EDGE_INT_STA	21:16	GPI_POS_EDGE_INT_STA. Positive edge detection indication for GPIO pins configured as inputs	0: No positive edge was detected on the corresponding pin (default) 1: At least one positive edge was detected on the corresponding pin **Note**: These bits are **cleared upon reading**
Reserved	15:14	Reserved. Reserved	
GPI_NEG_EDGE_INT_STA	13:8	GPI_NEG_EDGE_INT_STA. Negative edge detection indication for GPIO pins configured as inputs	0: No negative edge was detected on the corresponding pin (default) 1: At least one negative edge was detected on the corresponding pin **Note**: These bits are **cleared upon reading**
Reserved	7:6	Reserved. Reserved	
GPI_DATA	5:0	GPI_DATA. GPI data bits for GPIO pins configured as inputs	0: Logic low level detected at corresponding input-configured GPIO pin 1: Logic high level detected at corresponding input-configured GPIO pin

GEN_INT (0x07)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[14:7]							
Reset	0x0000							
Access Type	Read Only							

BIT	15	14	13	12	11	10	9	8
Field	Reserved[6:0]							PGAOVV_INT
Reset	0x0000							0b0
Access Type	Read Only							Read Only

BIT	7	6	5	4	3	2	1	0
Field	HVDD_INT	HVDDO_INT	THSHDN_INT	THWRNG_INT	OVC_INT	CNFG_INT	CRC_INT	GPI_INT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Clears All	Read Only	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:9	Reserved. Reserved	
PGAOVV_INT	8	PGAOVV_INT. PGA overvoltage indication	0: Voltages at AI5 and AI6 within range 1: Voltages at AI5 and/or AI6 are too high, resulting in an out-of-range condition at the output of the PGA **Note**: When asserted active high, disconnects the inputs from the signal path
HVDD_INT	7	HVDD_INT. HVDD/HVSS undervoltage indication	0: HVDD-HVSS voltage above threshold 1: HVDD-HVSS voltage below threshold
HVDDO_INT	6	HVDDO_INT. HVDDO/HVSSO undervoltage indication	0: HVDDO-HVSSO voltage above threshold 1: HVDDO-HVSSO voltage below threshold
THSHDN_INT	5	THSHDN_INT. Thermal shutdown indication	0: Die temperature low enough to permit normal operation 1: Die temperature exceeds approximately 165ºC, GEN_CNFG and GEN_CHNL_CTRL registers are reset to their default state (except for the CRC_EN, DACREF_SEL, and ADCREF_SEL bits) **Note**: this bit is **cleared upon reading**
THWRNG_INT	4	THWRNG_INT. Thermal warning indication	0: Die temperature within normal range 1: Die temperature above approximately 145ºC **Note**: this read-only bit warns of a potential impending thermal shutdown condition, cleared when the temperature drops below approximately 135ºC
OVC_INT	3	OVC_INT. Overcurrent indication on the analog output	0: Current demand within the acceptable range 1: Current demand exceeds 50mA (typical) **Note**: The clearing behavior of this bit depends on the setting of the OVC_CTRL bit in the GEN_CNFG register. If OVC_CTRL is set logic low (automatic mode), OVC_INT clears once the overcurrent condition is resolved. If OVC_CTRL is set logic high (host-controlled mode), then OVC_INT **clears upon reading**.
CNFG_INT	2	CNFG_INT. Configuration error indication:	0: No configuration error 1: Either: - AO_CNFG is set to a value between 0x9 and 0xF, AI1_2_CNFG is set to a value between 0x5 and 0x7, or AI5_6_CNFG is set to a value between 0x5 and 0x7; those configuration bits retain their previous value. For this type of configuration error, CNFG_INT **clears upon reading.** - Input amplifiers required for analog output voltage or current mode are not powered up. While the CNFG_INT is asserted, the required amplifiers for the selected output mode are automatically powered up, as reflected by the updated state of the GEN_CNFG register. For this type of configuration error, CNFG_INT **clears upon reading.** - Input amplifier(s) corresponding to the selection made by AI_DCHNL_SEL are not powered up. For this type of configuration error, CNFG_INT clears after **the inconsistency is resolved.**

BITFIELD	BITS	DESCRIPTION	DECODE
CRC_INT	1	CRC_INT. CRC error detection indication	0: No CRC error detected 1: CRC error detected **Note**: this **clear-on-read** bit never asserts unless the CRC is enabled
GPI_INT	0	GPI_INT. GPI edge detection indication	0: No new specified edges detected since last time this bit was read 1: At least one edge was detected at an input-configured GPIO pin since the last time this bit was read **Note**: Bit GPI_INT clears on read, and does not affect the bits in the GEN_GPI_DATA register. This bit reasserts upon detection of another selected edge after the register GEN_GPI_DATA has been read.

GEN_INTEN (0x08)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[14:7]							
Reset	0x0000							
Access Type	Read Only							

BIT	15	14	13	12	11	10	9	8
Field	Reserved[6:0]							PGAOVV_INTEN
Reset	0x0000							0b0
Access Type	Read Only							Write, Read

BIT	7	6	5	4	3	2	1	0
Field	HVDD_INTEN	HVDDO_INTEN	Reserved	THWRNG_INTEN	OVC_INTEN	CNFG_INTEN	CRC_INTEN	GPI_INTEN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:9	Reserved. Reserved	
PGAOVV_INTEN	8	PGAOVV_INTEN. PGAOVV interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin
HVDD_INTEN	7	HVDD_INTEN. HVDD interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin
HVDDO_INTEN	6	HVDDO_INTEN. HVDDO interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin
Reserved	5	Reserved. Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
THWRNG_INTEN	4	THWRNG_INTEN. THWRNG interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin
OVC_INTEN	3	OVC_INTEN. OVC interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin
CNFG_INTEN	2	CNFG_INTEN. CNFG interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin
CRC_INTEN	1	CRC_INTEN. CRC interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin
GPI_INTEN	0	GPI_INTEN. GPI interrupt enable	0: The corresponding interrupt cannot assert the $\overline{INT}$ pin (default) 1: The corresponding interrupt can assert the $\overline{INT}$ pin

GEN_PWR_CTRL (0x09)

BIT	23	22	21	20	19	18	17	16
Field	AODAC_PD	Reserved	AODAC_RST	Reserved	GEN_PD	Reserved	GEN_RST	Reserved[16]
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0x00000
Access Type	Write, Read	Read Only	Write, Read	Read Only	Write, Read	Read Only	Write, Read	Read Only

BIT	15	14	13	12	11	10	9	8
Field	Reserved[15:8]							
Reset	0x00000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
AODAC_PD	23	AODAC_PD. DAC power down control	0: Normal operation (default) 1: DAC powered down
Reserved	22	Reserved. Reserved	
AODAC_RST	21	AODAC_RST. DAC software reset control	0: Normal operation (default) 1: DAC is reset and stays reset until this bit is set to zero
Reserved	20	Reserved. Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
GEN_PD	19	GEN_PD. General power down control	0: Normal operation (default) 1: Powers down all amplifiers irrespective of the settings in the GEN_CNFG and the GEN_CHNL_CTRL registers. When GEN_PD is subsequently written with 0, returns the MAX22000 to the state defined by the GEN_CNFG and the GEN_CHNL_CTRL registers. The GEN_CNFG and the GEN_CHL_CTRL registers can be modified while GEN_PD is set to 1, and these modifications take effect when GEN_PD is written with 0.
Reserved	18	Reserved. Reserved	
GEN_RST	17	GEN_RST. General software reset control	0: Normal operation (default) 1: The GEN_CNFG and the GEN_CHNL_CTRL registers are reset. However, the values of CRC_EN, DACREF_SEL, and ADC_REF_SEL are not changed. Asserting GEN_RST also aborts any ADC conversion in progress. **Note**: This bit does not reset automatically, and, while it is set to 1, GEN_CNFG and GEN_CHNL_CTRL cannot be modified until GEN_RST is set back to 0.
Reserved	16:0	Reserved. Reserved	

DCHNL_CMD (0x20)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[1:0]		DCHNL_MODE[1:0]		DCHNL_RATE[3:0]			
Reset	0b00		0b01		0x0			
Access Type	Read Only		Write, Read		Write, Read			
BIT	15	14	13	12	11	10	9	8
Field	Reserved[15:8]							
Reset	0x0000							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:22	Reserved. Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
DCHNL_MODE	21:20	DCHNL_MODE. Analog input ADC mode	00: Reserved. Do not use 01: Power-down, see the DCHNL_PD bit for the type of power-down performed (default) 10: Reserved. Do not use 11: Conversion mode **Note**: If an ADC conversion is in progress, writing to the DCHNL_MODE register is ignored unless it is to power down the ADC
DCHNL_RATE	19:16	DCHNL_RATE. ADC data rate	- See Table 10 for data rate selection for continuous conversion - See Table 11 for data rate selection for single-cycle conversion - See Table 12 for single-cycle continuous conversion. Default is 0x0.
Reserved	15:0	Reserved. Reserved	

DCHNL_STA (0x21)

Note: DCHNL_STA updates coincident with the availability of a new converted ADC sample.

BIT	23	22	21	20	19	18	17	16
Field	Reserved[8:1]							
Reset	0x000							
Access Type	Read Only							

BIT	15	14	13	12	11	10	9	8
Field	Reserved[0]	REFDET	Reserved[3:0]				DOR	AOR
Reset	0x000	0b0	0x0				0b0	0b0
Access Type	Read Only	Read Only	Read Only				Read Only	Read Only

BIT	7	6	5	4	3	2	1	0
Field	RATE[3:0]				PDSTAT[1:0]		MSTAT	RDY
Reset	0x0				0b10		0b0	0b0
Access Type	Read Only				Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:15	Reserved. Reserved	
REFDET	14	REFDET. Reference voltage detection	0: No reference voltage detected 1: Reference voltage detected **Note**: This bit results from a comparison of the selected ADC reference voltage, either internal or external, against a fixed threshold of approximately 350mV
Reserved	13:10	Reserved. Reserved	
DOR	9	DOR. Digital overrange	0: The conversion result is within the digital range of the ADC 1: The conversion result exceeds the digital range of the ADC. The result is set to the minimum or maximum value, as appropriate **Note**: Updated when RDY asserts for a new sample

BITFIELD	BITS	DESCRIPTION	DECODE
AOR	8	AOR. Analog overrange	0: The conversion result is within the analog operating range of the ADC 1: The conversion result exceeds the analog operating range of the ADC, and the converted value is possibly corrupted **Note**: Updated when RDY asserts for a new sample
RATE	7:4	RATE. Conversion rate readback	These bits indicate the conversion rate corresponding to the result in the DCHNL_DATA register that is about to be read. Refer to Tables 10, 11, or 12.
PDSTAT	3:2	PDSTAT. Power down status	00: ADC performing conversions 01: Reserved. Do not use. 10: ADC is on standby (default) 11: ADC is in reset
MSTAT	1	MSTAT. ADC modulator status	0: ADC delta-sigma modulator is not converting 1: Conversion in progress **Note**: The status update of the MSTAT bit may be delayed up to 2µs after start or completion of a conversion, which should be taken into account if polling the MSTAT bit immediately after a status change
RDY	0	RDY. Conversion result ready	0: No new conversion result available 1: New conversion result available **Note**: this bit resets upon reading of the DCHNL_DATA register

DCHNL_CTRL1 (0x22)

Note: Any write to the DCHNL_CTRL1 register that changes any non-reserved bits aborts any ongoing ADC conversion.

BIT	23	22	21	20	19	18	17	16
Field	Reserved[2:0]			DCHNL_PD	Reserved[1:0]		SCYCLE	CONTSC
Reset	0b000			0b0	0b00		0b1	0b0
Access Type	Read Only			Write, Read	Read Only		Write, Read	Write, Read

BIT	15	14	13	12	11	10	9	8
Field	Reserved[15:8]							
Reset	0x0000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:21	Reserved. Reserved	
DCHNL_PD	20	DCHNL_PD. ADC power down State	0: ADC in standby when powered down (default) 1: ADC in reset when powered down

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	19:18	Reserved. Reserved	
SCYCLE	17	SCYCLE. Single-cycle conversion mode	0: Continuous conversion, with latency due to digital filtering 1: Single-cycle no-latency conversion (default)
CONTSC	16	CONTSC. Continuous single-cycle mode	0: Single conversion, then transition to standby (default) 1: Continuous single-cycle conversion **Note**: Only in effect when SCYCLE is 1
Reserved	15:0	Reserved. Reserved	

DCHNL_CTRL2 (0x23)

Note: Any write to the DCHNL_CTRL2 register that changes any non-reserved bits aborts any ongoing ADC conversion.

BIT	23	22	21	20	19	18	17	16
Field	EXTCLK	Reserved	SYNC_MODE	Reserved	NOSYSG	NOSYSO	Reserved[17:16]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0x00000	
Access Type	Write, Read	Read Only	Write, Read	Read Only	Write, Read	Write, Read	Read Only	

BIT	15	14	13	12	11	10	9	8
Field	Reserved[15:8]							
Reset	0x00000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
EXTCLK	23	EXTCLK. External clock source selection	0: Use the internal oscillator for the ADC (default) 1: Use an external clock source on the CLK pin for the ADC
Reserved	22	Reserved. Reserved	
SYNC_MODE	21	SYNC_MODE. External synchronization selection	0: Disabled (default) 1: Enabled using the SYNC pin
Reserved	20	Reserved. Reserved	
NOSYSG	19	NOSYSG. No system calibration gain correction	0: System calibration coefficient SGC used to correct ADC data (default) 1: Behaves as if the gain correction were set to 0x800000 **Note**: This global bit affects all ADC gain corrections

BITFIELD	BITS	DESCRIPTION	DECODE
NOSYSO	18	NOSYSO. No system offset correction	0: System calibration coefficient SOC used to correct ADC data (default) 1: Behaves as if offset correction were set to 0x000000 **Note**: This global bit affects all ADC offset corrections
Reserved	17:0	Reserved. Reserved	

DCHNL_DATA (0x24)

BIT	23	22	21	20	19	18	17	16
Field	DCHNL_DATA[23:16]							
Reset	0x000000							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	DCHNL_DATA[15:8]							
Reset	0x000000							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	DCHNL_DATA[7:0]							
Reset	0x000000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
DCHNL_DATA	23:0	DCHNL_DATA. Digital result of ADC conversion, two’s complement

DCHNL_N_SEL (0x25)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[19:12]							
Reset	0x00000							
Access Type	Read Only							
BIT	15	14	13	12	11	10	9	8
Field	Reserved[11:4]							
Reset	0x00000							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	Reserved[3:0]				DCHNL_N_SEL[3:0]			
Reset	0x00000				0x0			
Access Type	Read Only				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:4	Reserved. Reserved	
DCHNL_N_SEL	3:0	DCHNL_N_SEL. Data channel N calibration coefficient access selection	The value written in this register field corresponds to the channel number described for the register field AI_DCHNL_SEL[3:0]. Once this register field is written with the desired channel number value, the SOC and SGC registers for the selected channel are accessed when writing to or reading from registers DCHNL_N_SOC and DCHNL_N_SGC. This is an indirect addressing scheme.

DCHNL_N_SOC (0x26)

BIT	23	22	21	20	19	18	17	16
Field	DCHNL_N_SOC[23:16]							
Reset	0x000000							
Access Type	Write, Read							
BIT	15	14	13	12	11	10	9	8
Field	DCHNL_N_SOC[15:8]							
Reset	0x000000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DCHNL_N_SOC[7:0]							
Reset	0x000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DCHNL_N_SOC	23:0	DCHNL_N_SOC. Data channel N system offset calibration value	Accesses the offset calibration value, in two's complement format, for the channel selected by the DCHNL_N_SEL bits in the DCHNL_N_SEL register **Note**: The write does not occur if an ADC conversion is in progress and the DCHNL_N_SEL bits match the AI_DCHNL_SEL bits

DCHNL_N_SGC (0x27)

BIT	23	22	21	20	19	18	17	16
Field	DCHNL_N_SGC[23:16]							
Reset	0xC00000							
Access Type	Write, Read							

BIT	15	14	13	12	11	10	9	8
Field	DCHNL_N_SGC[15:8]							
Reset	0xC00000							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	DCHNL_N_SGC[7:0]							
Reset	0xC00000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
DCHNL_N_SGC	23:0	DCHNL_N_SGC. Data channel N system gain calibration value	Access the gain calibration value, in unsigned binary format, for the channel selected by the DCHNL_N_SEL bits in the DCHNL_N_SEL register. The gain is: $\frac{DCHNL_N_SGC}{2^{23}}$ **Note**: The write does not occur if an ADC conversion is in progress and the DCHNL_N_SEL bits match the AI_DCHNL_SEL bits

AO_DATA_WR (0x40)

BIT	23	22	21	20	19	18	17	16
Field	AO_DATA_W[17:10]							
Reset	0x00000							
Access Type	Write Only							

BIT	15	14	13	12	11	10	9	8
Field	AO_DATA_W[9:2]							
Reset	0x00000							
Access Type	Write Only							

BIT	7	6	5	4	3	2	1	0
Field	AO_DATA_W[1:0]		Reserved[5:0]					
Reset	0x00000		0x00					
Access Type	Write Only		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
AO_DATA_W	23:6	AO_DATA_W. Analog output data write	Digital code, in two's complement format. Consult Table 9 to map from code to output
Reserved	5:0	Reserved. Reserved	

AO_OFFSET_CORR_WR (0x41)

BIT	23	22	21	20	19	18	17	16
Field	AO_OFFSET_W[17:10]							
Reset	0x00000							
Access Type	Write Only							

BIT	15	14	13	12	11	10	9	8
Field	AO_OFFSET_W[9:2]							
Reset	0x00000							
Access Type	Write Only							

BIT	7	6	5	4	3	2	1	0
Field	AO_OFFSET_W[1:0]		Reserved[5:0]					
Reset	0x00000		0x00					
Access Type	Write Only		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
AO_OFFSET_W	23:6	AO_OFFSET_W. Analog output offset correction write	Digital code in two's complement. Consult Table 8 to calculate offset correction.
Reserved	5:0	Reserved. Reserved	

AO_GAIN_CORR_WR (0x42)

BIT	23	22	21	20	19	18	17	16
Field	AO_GAIN_W[17:10]							
Reset	0x3FFFF							
Access Type	Write Only							

BIT	15	14	13	12	11	10	9	8
Field	AO_GAIN_W[9:2]							
Reset	0x3FFFF							
Access Type	Write Only							

BIT	7	6	5	4	3	2	1	0
Field	AO_GAIN_W[1:0]		Reserved[5:0]					
Reset	0x3FFFF		0x00					
Access Type	Write Only		Read Only					

BITFIELD	BITS	DESCRIPTION	DECODE
AO_GAIN_W	23:6	AO_GAIN_W. Analog output gain correction write	Digital code, in unsigned binary. Consult Table 7 to calculate gain correction
Reserved	5:0	Reserved. Reserved	

AO_CNFG_WR (0x43)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[3:0]				AO_RB_EN	Reserved[18:16]		
Reset	0x0				0b0	0x00000		
Access Type	Read Only				Write Only	Read Only		

BIT	15	14	13	12	11	10	9	8
Field	Reserved[15:8]							
Reset	0x00000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:20	Reserved. Reserved	
AO_RB_EN	19	AO_RB_EN. Analog output readback enable	0: AO_DATA_RD, AO_OFFSET_CORR_RD, and AO_GAIN_CORR_RD registers do not return valid data 1: AO_DATA_RD, AO_OFFSET_CORR_RD, and AO_GAIN_CORR_RD return valid data
Reserved	18:0	Reserved. Reserved	

AO_DATA_RD (0x44)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[5:0]						AO_DATA_R[17:16]	
Reset	0x00						0x00000	
Access Type	Read Only						Read Only	

BIT	15	14	13	12	11	10	9	8
Field	AO_DATA_R[15:8]							
Reset	0x00000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AO_DATA_R[7:0]							
Reset	0x00000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:18	Reserved. Reserved	

BITFIELD	BITS	DESCRIPTION	DECODE
AO_DATA_R	17:0	AO_DATA_R. Analog output data readback	Reads back the contents of the analog output data register when bit AO_RB_EN is high

AO_OFFSET_CORR_RD (0x45)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[5:0]						AO_OFFSET_R[17:16]	
Reset	0x00						0x00000	
Access Type	Read Only						Read Only	

BIT	15	14	13	12	11	10	9	8
Field	AO_OFFSET_R[15:8]							
Reset	0x00000							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AO_OFFSET_R[7:0]							
Reset	0x00000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:18	Reserved. Reserved	
AO_OFFSET_R	17:0	AO_OFFSET_R. Analog output offset correction readback	Reads back the contents of the analog output offset correction register when bit AO_RB_EN is high

AO_GAIN_CORR_RD (0x46)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[5:0]						AO_GAIN_R[17:16]	
Reset	0x00						0x3FFFF	
Access Type	Read Only						Read Only	

BIT	15	14	13	12	11	10	9	8
Field	AO_GAIN_R[15:8]							
Reset	0x3FFFF							
Access Type	Read Only							

BIT	7	6	5	4	3	2	1	0
Field	AO_GAIN_R[7:0]							
Reset	0x3FFFF							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:18	Reserved. Reserved	
AO_GAIN_R	17:0	AO_GAIN_R. Analog ouput gain correction readback	Reads back the contents of the analog output gain correction register when bit AO_RB_EN is high

AO_STA_RD (0x47)

BIT	23	22	21	20	19	18	17	16
Field	Reserved[10:3]							
Reset	0x000							
Access Type	Read Only							

BIT	15	14	13	12	11	10	9	8
Field	Reserved[2:0]			BUSY	Reserved[11:8]			
Reset	0x000			0x0	0x000			
Access Type	Read Only			Read Only	Read Only			

BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	23:13	Reserved. Reserved	
BUSY	12	BUSY. Analog output status	0: Analog output calculations completed; analog output reflects digital input 1: Analog output calculations in progress; the latest digital input not yet reflected in analog output
Reserved	11:0	Reserved. Reserved	

Applications Information

Power Supply Headroom Requirements

Analog inputs power from HVDD and HVSS, and generally need 2.5V of headroom to meet all linearity specifications. Low voltage PGA inputs (±2.5V, ±500mV, ±250mV, and ±125mV) require at least a ±5V supply, as long as both AI5 and AI6 meet the ±2.5V range individually. To accept ±10V inputs, whose full-scale range is ±12.5V, supply the MAX22000 with at least ±15V on HVDD/HVSS.

The analog output powers from HVDDO and HVSSO. For the AOVM ±12.5V setting, power from at least a recommended ±15.2V supply. For the AOVM +25V setting, power HVDDO with at least a recommended +28V and HVSSO with a recommended -5V supply. For any AOCM setting, power from at least a recommended ±22.5V supply. Depending on the application, it might be possible to use lower voltages. Refer to Notes 2 and 6 of the *Electrical Characteristics* table for further details.

Power Supply Sequencing

The four supplies, AVDD, DVDD, HVDD/HVSS, and HVDDO/HVSSO can power up in any order. It is recommended to have a minimum delay between respective pairs, such as HVDD and HVSS, HVDDO and HVSSO referenced to AGND.

The only restriction is that HVSS must always be more negative than HVSSO. Refer to the *Absolute Maximum Ratings* section for all power supply restrictions.

Any external reference voltage on the REF_DAC_EXT pin must never exceed V_{AVDD}. A schottky diode connected between REF_DAC_EXT and AVDD can help satisfy this requirement.

Board Layout

Use proper grounding techniques such as a multilayer board with a low-inductance ground plane.

- Keep DGND separate from AGND, connecting the two at one point.
- Use ground plane shielding to improve noise immunity.
- Keep analog signal traces away from digital signal traces, especially clock traces.
- Connect the exposed pads on the bottom of the MAX22000 to HVSS.

For a detailed recommended layout, refer to the MAX22000 EV kit data sheet.

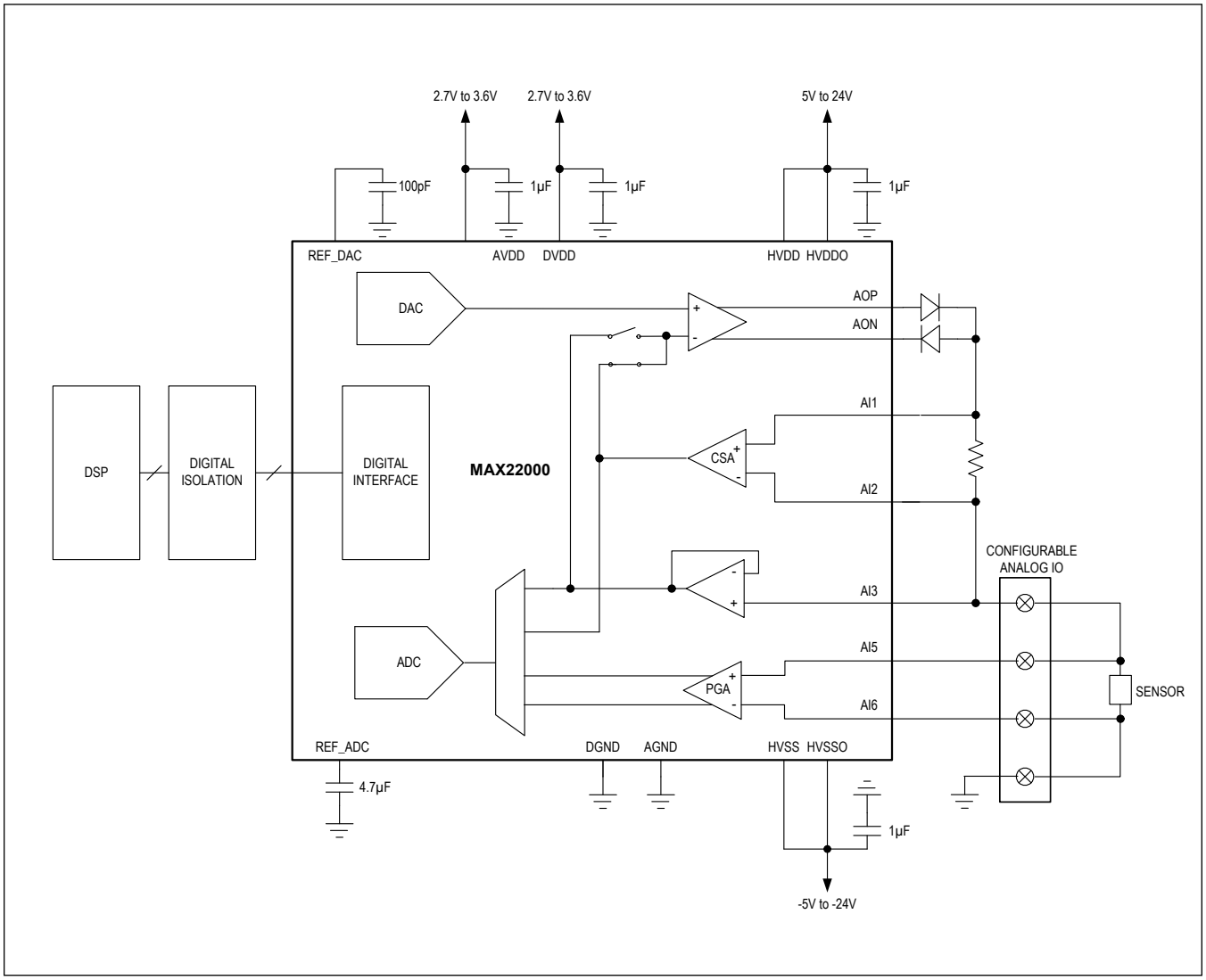
Surge Protection

With external circuitry, the input and output ports are protected against ±1kV/42Ω surge pulses as per IEC610004-5. Place a 36V bidirectional TVS between the output and AGND, past the AOP/AON diodes and past the current sense resistor. Place a minimum 4.7kΩ surge tolerant resistor in series with each input port at risk.

The other MAX22000 pins are rated for Human Body Model (HBM). If surge voltages can couple from the high voltage supplies (HVDD, HVDDO, HVSS, or HVSSO) to the low voltage supplies (DVDD or AVDD), place additional TVS suppressors on these power rails, or place TVS suppressors on the digital signal traces.

Typical Application Circuits

Typical Application Diagram



Ordering Information

PART NUMBER	ADC RESOLUTION	DAC RESOLUTION	TEMP. RANGE	PACKAGE
MAX22000ALB+	24 bits	18 bits	-40ºC to +125ºC	64 LGA
MAX22000ALB+T	24 bits	18 bits	-40ºC to +125ºC	64 LGA

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/19	Initial release	—
1	5/20	Updated the *Electrical Characteristics* section, updated Table 1 and Table 2, added the *Typical Application Circuit*; fixed typos	1, 7, 23, 67
2	6/20	Replaced the *Typical Application Circuit*	67
3	3/22	Updated *Benefits and Features* section, *Electrical Characteristics* table, Table 3, *ADC Operating Modes* section, Tables 10-13, *ADC Software Reset* section, and added bit description for Register 0x00 and reset value for Register 0x01 in Register Map; removed Figure 7	1, 6, 7, 12, 13, 24, 32, 33, 34, 38, 39, 41

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