

## N-Channel Enhancement Mode Power MOSFET

### Description

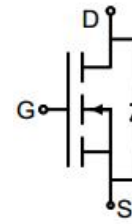
The GT52N10D5 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. It can be used in a wide variety of applications.

### General Features

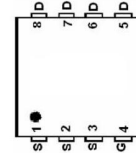
- $V_{DS}$  100V
- $I_D$  (at  $V_{GS} = 10V$ ) 71A
- $R_{DS(ON)}$  (at  $V_{GS} = 10V$ ) < 7.5m $\Omega$
- $R_{DS(ON)}$  (at  $V_{GS} = 4.5V$ ) < 10m $\Omega$
- 100% Avalanche Tested
- RoHS Compliant

### Application

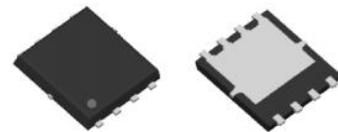
- Power switch
- DC/DC converters



Schematic diagram



pin assignment



DFN5X6-8L

### Ordering Information

| Device    | Package   | Marking | Packaging    |
|-----------|-----------|---------|--------------|
| GT52N10D5 | DFN8L-5*6 | GT52N10 | 5000pcs/Reel |

### Absolute Maximum Ratings $T_C = 25^\circ C$ , unless otherwise noted

| Parameter  | Symbol         | Value      | Unit       |
|--|----------------|------------|------------|
| Drain-Source Voltage                             | $V_{DS}$       | 100        | V          |
| Continuous Drain Current                         | $I_D$          | 71         | A          |
| Pulsed Drain Current (note1)                     | $I_{DM}$       | 284        | A          |
| Gate-Source Voltage                              | $V_{GS}$       | $\pm 20$   | V          |
| Power Dissipation                                | $P_D$          | 100        | W          |
| Single pulse avalanche energy (note2)            | $E_{AS}$       | 196        | mJ         |
| Operating Junction and Storage Temperature Range | $T_J, T_{stg}$ | -55 To 150 | $^\circ C$ |

### Thermal Resistance

| Parameter                               | Symbol     | Value | Unit         |
|---|------------|-------|--------------|
| Thermal Resistance, Junction-to-Ambient | $R_{thJA}$ | 60    | $^\circ C/W$ |
| Maximum Junction-to-Case                | $R_{thJC}$ | 1.25  | $^\circ C/W$ |

| Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted |               |  |       |      |           |            |
|--|---------------|--|-------|------|-----------|------------|
| Parameter  | Symbol        | Test Conditions  | Value |      |           | Unit       |
|  |               |  | Min.  | Typ. | Max.      |            |
| <b>Static Parameters</b>   |               |  |       |      |           |            |
| Drain-Source Breakdown Voltage                                   | $V_{(BR)DSS}$ | $V_{GS} = 0V, I_D = 250\mu A$                            | 100   | --   | --        | V          |
| Zero Gate Voltage Drain Current                                  | $I_{DSS}$     | $V_{DS} = 100V, V_{GS} = 0V$                             | --    | --   | 1         | $\mu A$    |
| Gate-Source Leakage  | $I_{GSS}$     | $V_{GS} = \pm 20V$                                       | --    | --   | $\pm 100$ | nA         |
| Gate-Source Threshold Voltage                                    | $V_{GS(th)}$  | $V_{DS} = V_{GS}, I_D = 250\mu A$                        | 1     | 1.4  | 2.5       | V          |
| Drain-Source On-Resistance                                       | $R_{DS(on)}$  | $V_{GS} = 10V, I_D = 50A$                                | --    | 6    | 7.5       | m $\Omega$ |
|  |               | $V_{GS} = 4.5V, I_D = 50A$                               | --    | 7.5  | 10        |            |
| Forward Transconductance   | $g_{FS}$      | $V_{GS} = 5V, I_D = 50A$                                 | --    | 71   | --        | S          |
| <b>Dynamic Parameters</b>  |               |  |       |      |           |            |
| Input Capacitance  | $C_{iss}$     | $V_{GS} = 0V,$<br>$V_{DS} = 50V,$<br>$f = 1.0\text{MHz}$ | --    | 2234 | --        | pF         |
| Output Capacitance   | $C_{oss}$     |  | --    | 387  | --        |            |
| Reverse Transfer Capacitance                                     | $C_{rss}$     |  | --    | 19   | --        |            |
| Total Gate Charge  | $Q_g$         | $V_{DD} = 50V,$<br>$I_D = 50A,$<br>$V_{GS} = 10V$        | --    | 35   | --        | nC         |
| Gate-Source Charge   | $Q_{gs}$      |  | --    | 8    | --        |            |
| Gate-Drain Charge  | $Q_{gd}$      |  | --    | 5    | --        |            |
| Turn-on Delay Time   | $t_{d(on)}$   | $V_{DD} = 50V,$<br>$I_D = 50A,$<br>$R_G = 3\Omega$       | --    | 10   | --        | ns         |
| Turn-on Rise Time  | $t_r$         |  | --    | 4    | --        |            |
| Turn-off Delay Time  | $t_{d(off)}$  |  | --    | 31   | --        |            |
| Turn-off Fall Time   | $t_f$         |  | --    | 6    | --        |            |
| <b>Drain-Source Body Diode Characteristics</b>                   |               |  |       |      |           |            |
| Continuous Body Diode Current                                    | $I_S$         | $T_C = 25^\circ\text{C}$                                 | --    | --   | 70        | A          |
| Body Diode Voltage   | $V_{SD}$      | $T_J = 25^\circ\text{C}, I_{SD} = 50A, V_{GS} = 0V$      | --    | --   | 1.2       | V          |
| Reverse Recovery Charge  | $Q_{rr}$      | $I_F = 50A, V_{GS} = 0V$<br>$di/dt = 500A/\mu s$         | --    | 170  | --        | nC         |
| Reverse Recovery Time  | $T_{rr}$      |  | --    | 34   | --        | ns         |

### Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition :  $T_J = 25^\circ\text{C}, V_{DD} = 50V, V_{GS} = 10V, L = 0.5\text{mH}, R_G = 25\Omega$
3. Identical low side and high side switch with identical  $R_G$

### Gate Charge Test Circuit



### Switch Time Test Circuit

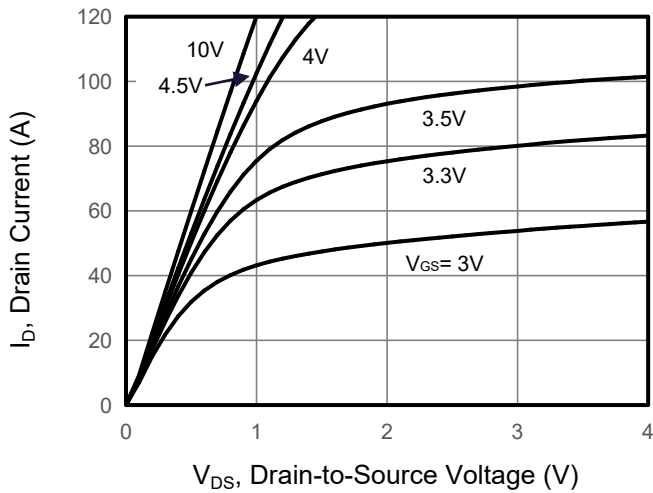


### EAS Test Circuit

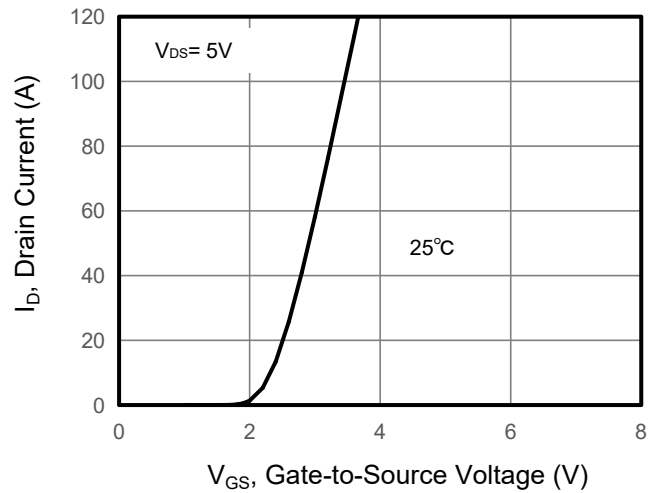


Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

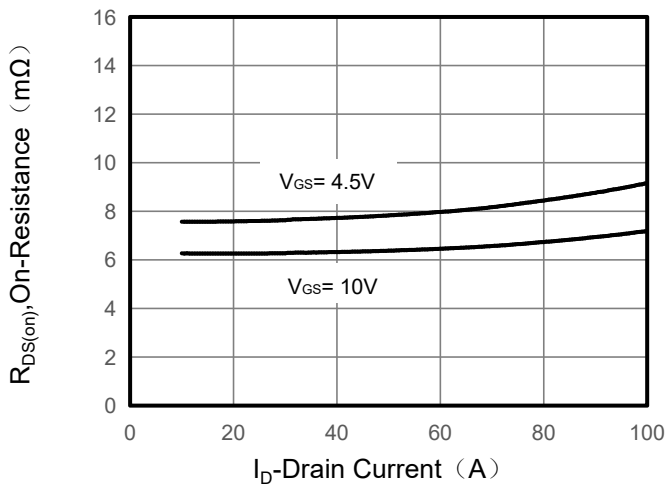
**Figure 1. Output Characteristics**



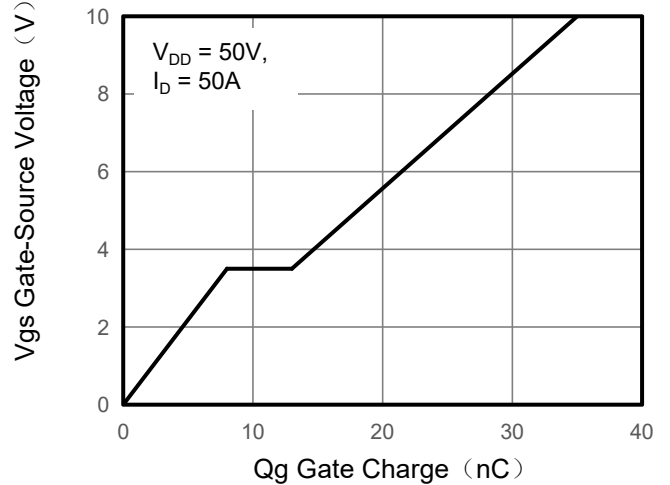
**Figure 2. Transfer Characteristics**



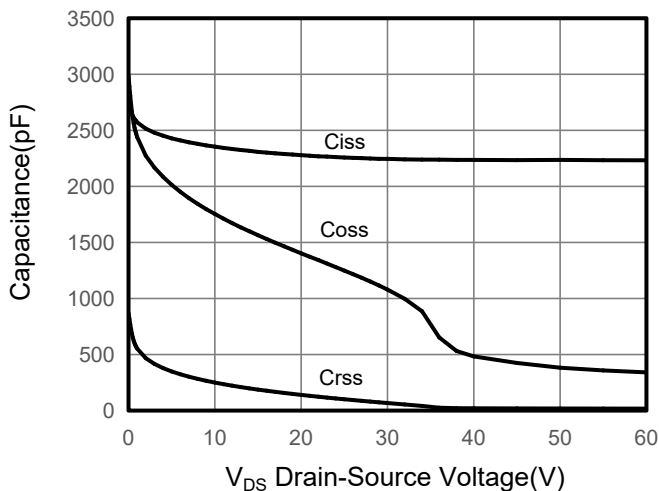
**Figure 3. Drain Source On Resistance**



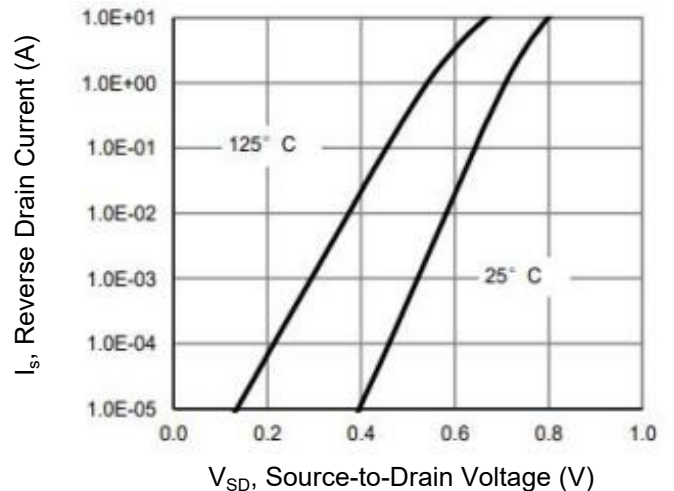
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Source-Drain Diode Forward**



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Drain-Source On-Resistance

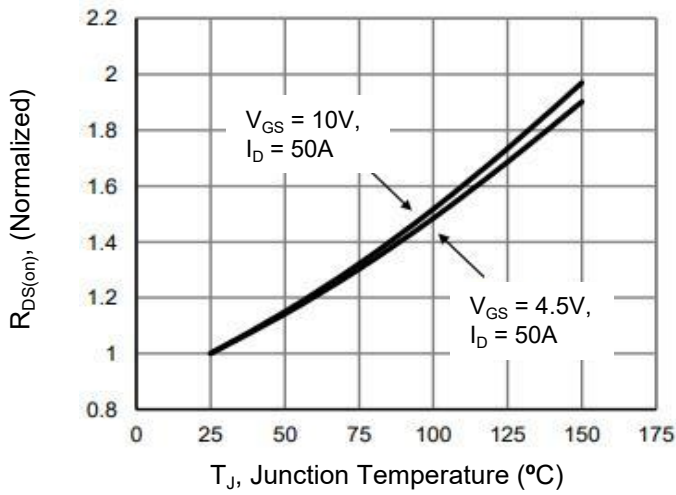


Figure 8. Safe Operation Area

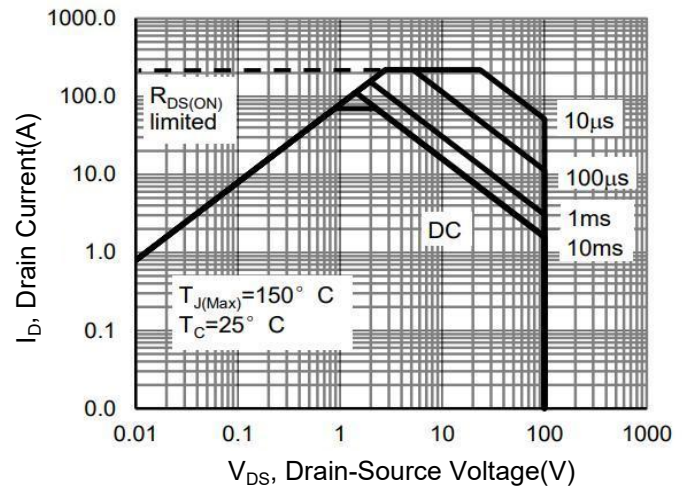
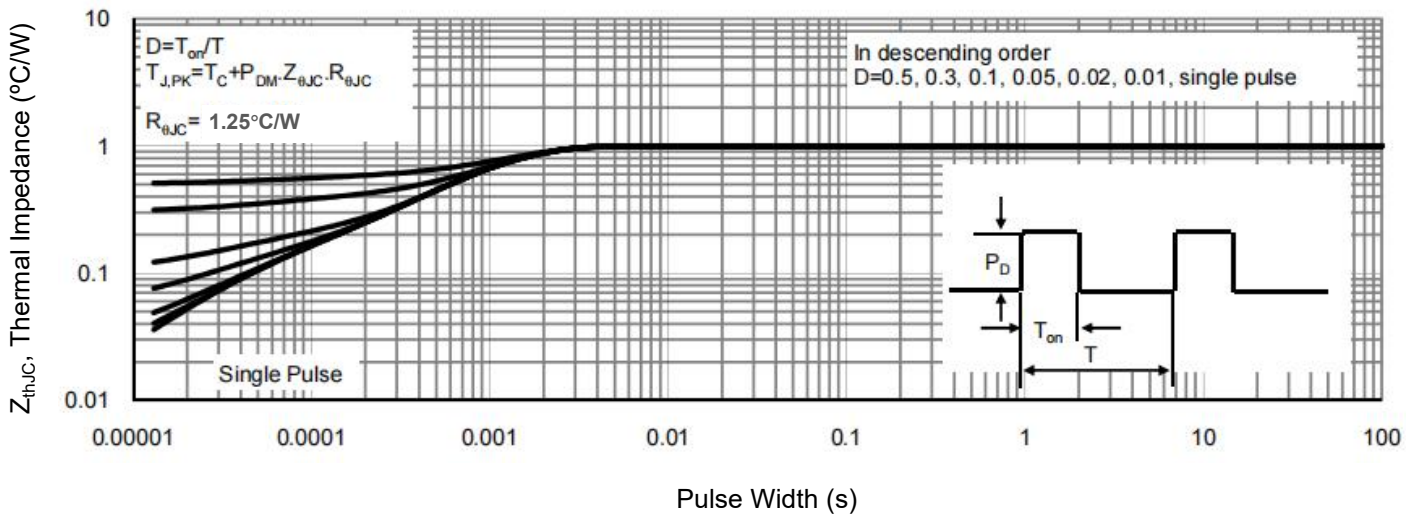
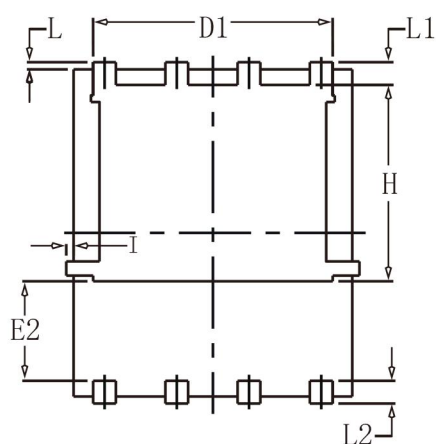
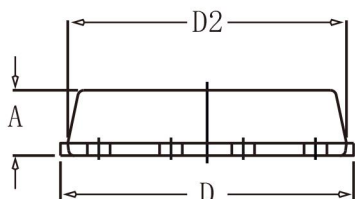
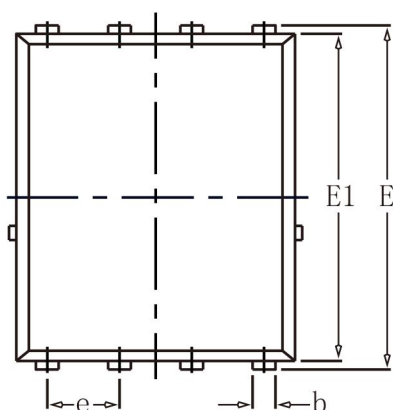


Figure 9. Normalized Maximum Transient Thermal Impedance



## DFN5X6-8L Package Information



| SYMBOL | COMMON   |       |          |        |
|--------|----------|-------|----------|--------|
|        | MM       |       | INCH     |        |
|        | MIN      | MAX   | MIN      | MAX    |
| A      | 1.03     | 1.17  | 0.0406   | 0.0461 |
| b      | 0.34     | 0.48  | 0.0134   | 0.0189 |
| c      | 0.824    | 0.970 | 0.0324   | 0.0382 |
| D      | 4.80     | 5.40  | 0.1890   | 0.2126 |
| D1     | 4.11     | 4.31  | 0.1618   | 0.1697 |
| D2     | 4.80     | 5.00  | 0.1890   | 0.1969 |
| E      | 5.59     | 6.15  | 0.2343   | 0.2421 |
| E1     | 5.65     | 5.85  | 0.2224   | 0.2303 |
| E2     | 1.60     | -     | 0.0630   | -      |
| e      | 1.27 BSC |       | 0.05 BSC |        |
| L      | 0.05     | 0.25  | 0.0020   | 0.0098 |
| L1     | 0.38     | 0.50  | 0.0150   | 0.0197 |
| L2     | 0.38     | 0.50  | 0.0150   | 0.0197 |
| H      | 3.30     | 3.50  | 0.1299   | 0.1378 |
| I      | -        | 0.18  | -        | 0.0070 |