

NTLJS3180PZ

Power MOSFET

-20 V, -7.7 A, μ Cool™ Single P-Channel, ESD, 2x2 mm WDFN Package

Features

- WDFN 2x2 mm Package with Exposed Drain Pads for Excellent Thermal Conduction
- Lowest $R_{DS(on)}$ Solution in 2x2 mm Package
- Footprint Same as SC-88 Package
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- ESD Protected
- This is a Pb-Free Device

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- High Side Load Switch
- Battery Switch
- DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	-20	V	
Gate-to-Source Voltage	V_{GS}	± 8.0	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-5.9	A
		$T_A = 85^\circ\text{C}$	-4.2	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$	-7.7	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.9	W
		$t \leq 5 \text{ s}$	3.3	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	-3.5	A
		$T_A = 85^\circ\text{C}$	-2.5	
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	0.7	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-23	A
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode) (Note 2)	I_S	-2.8	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

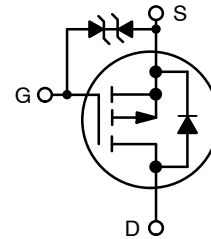
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size, (30 mm², 2 oz Cu).



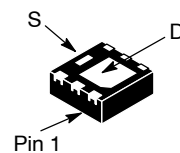
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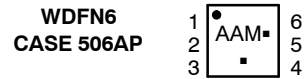
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-20 V	38 m Ω @ -4.5 V	-7.7 A
	50 m Ω @ -2.5 V	
	75 m Ω @ -1.8 V	
	200 m Ω @ -1.5 V	



P-CHANNEL MOSFET

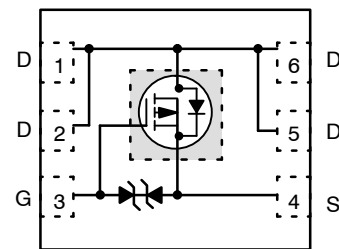


MARKING DIAGRAM



AA = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLJS3180PZTAG	WDFN6	3000/Tape & Reel
NTLJS3180PZTBG	(Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	65	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	180	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	38	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).

4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}$, Ref to 25°C		-5.0		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1.0	μA
					-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			± 10	μA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.45		-1.0	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.0		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}$		30	38	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -3.0\text{ A}$		40	50	
		$V_{GS} = -1.8\text{ V}, I_D = -2.0\text{ A}$		55	75	
		$V_{GS} = -1.5\text{ V}, I_D = -1.8\text{ A}$		85	200	
Forward Transconductance	g_{FS}	$V_{DS} = -16\text{ V}, I_D = -3.0\text{ A}$		7.7		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -16\text{ V}$		1100		pF
Output Capacitance	C_{OSS}			180		
Reverse Transfer Capacitance	C_{RSS}			130		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -16\text{ V}, I_D = -3.0\text{ A}$		13	19.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.5		
Gate-to-Source Charge	Q_{GS}			1.4		
Gate-to-Drain Charge	Q_{GD}			4.2		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -3.0\text{ A}, R_G = 3.0\ \Omega$		8.0		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(OFF)}$			70		
Fall Time	t_f			67		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -2.0\text{ A}$	$T_J = 25^\circ\text{C}$		-0.7	-1.0	V
			$T_J = 125^\circ\text{C}$		-0.6		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, d_{ISD}/d_t = 100\text{ A}/\mu\text{s}, I_S = -2.0\text{ A}$		60		ns	
Charge Time	t_a			16			
Discharge Time	t_b			44			
Reverse Recovery Time	Q_{RR}			41			nC

5. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

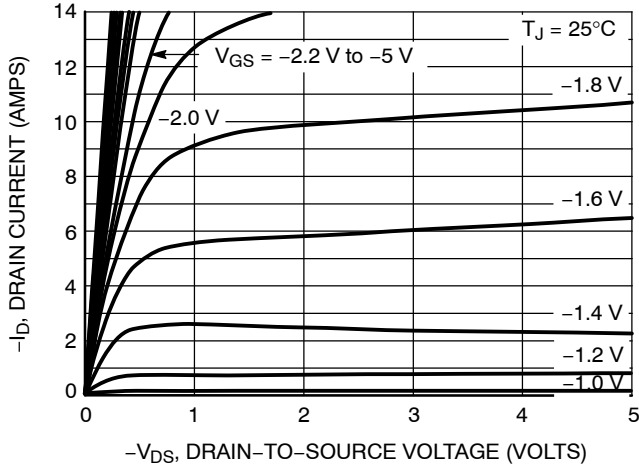


Figure 1. On-Region Characteristics

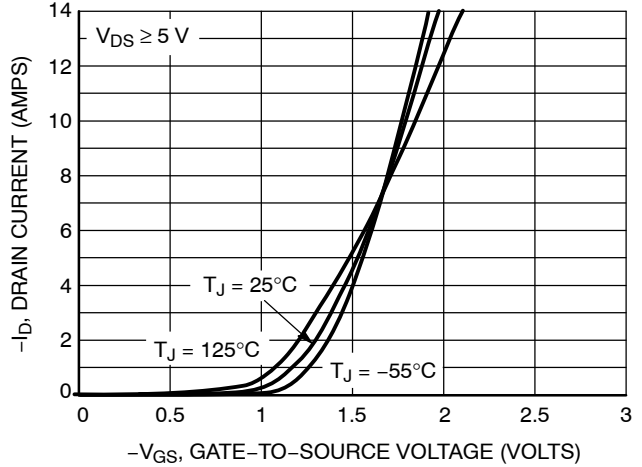


Figure 2. Transfer Characteristics

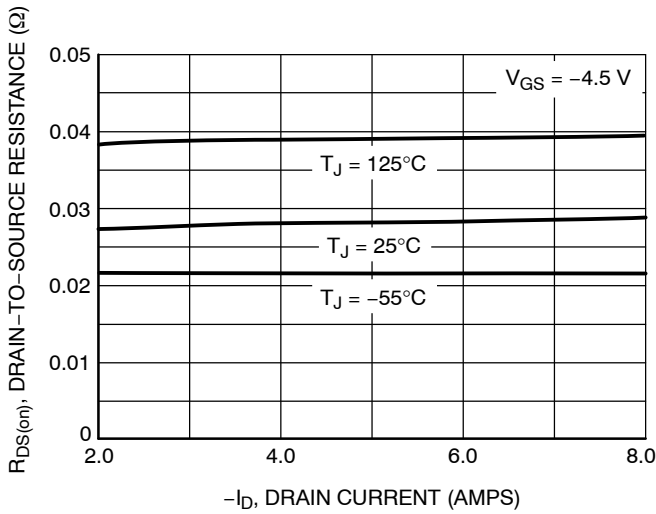


Figure 3. On-Resistance versus Drain Current

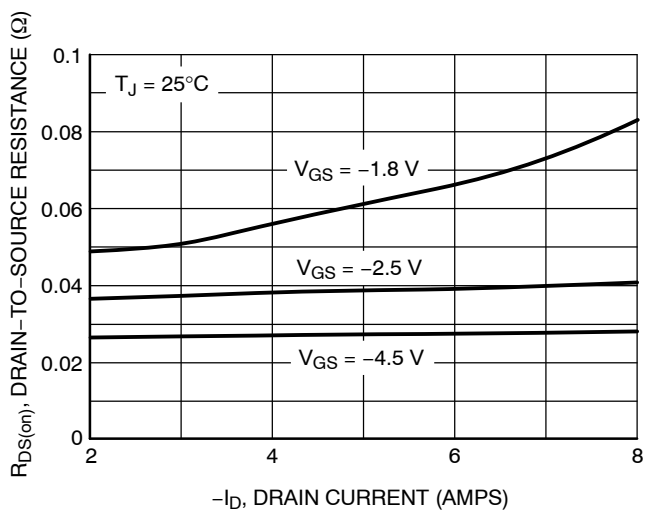


Figure 4. On-Resistance versus Drain Current and Gate Voltage

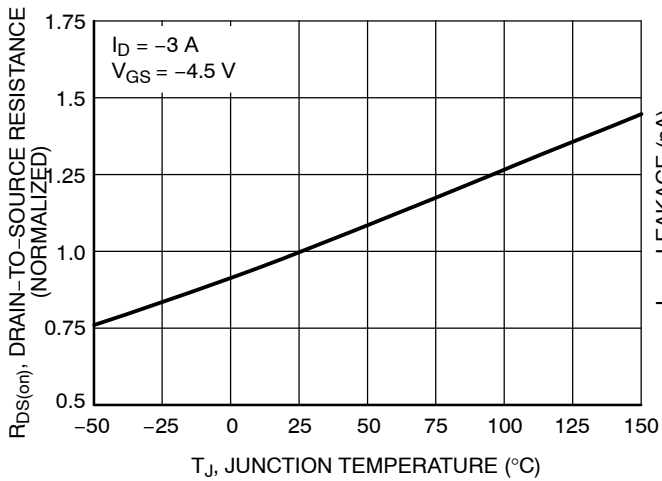


Figure 5. On-Resistance Variation with Temperature

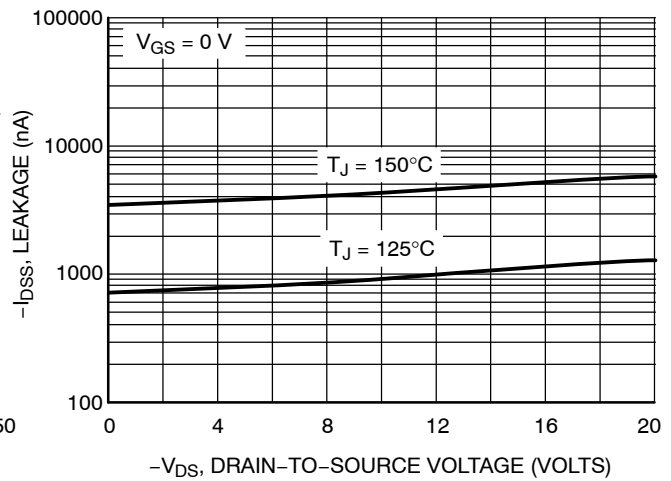


Figure 6. Drain-to-Source Leakage Current versus Voltage

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

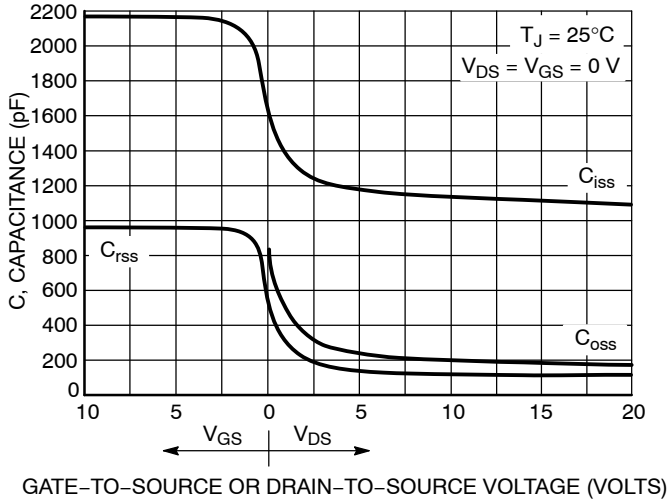


Figure 7. Capacitance Variation

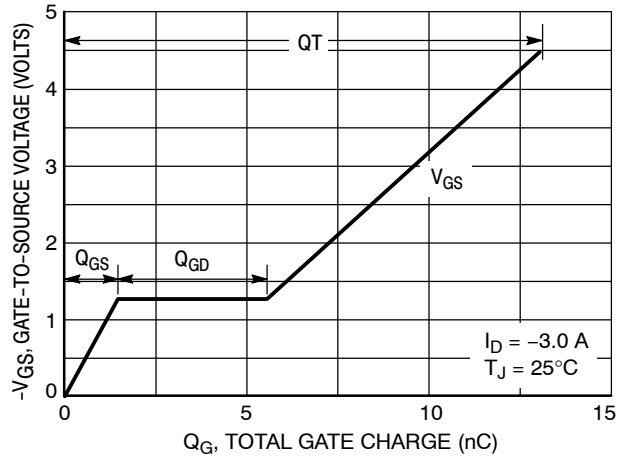


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

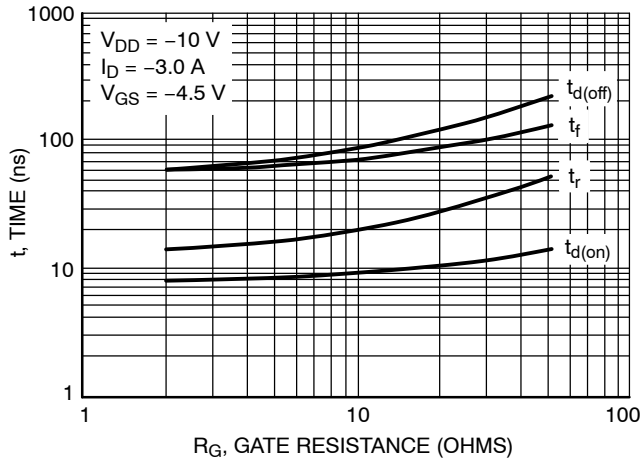


Figure 9. Resistive Switching Time Variation versus Gate Resistance

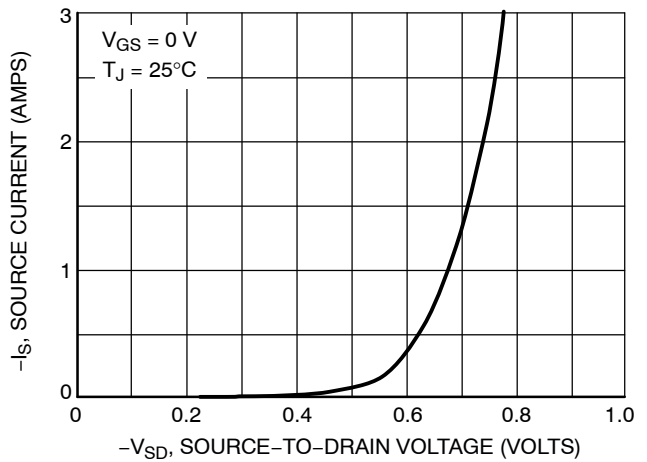


Figure 10. Diode Forward Voltage versus Current

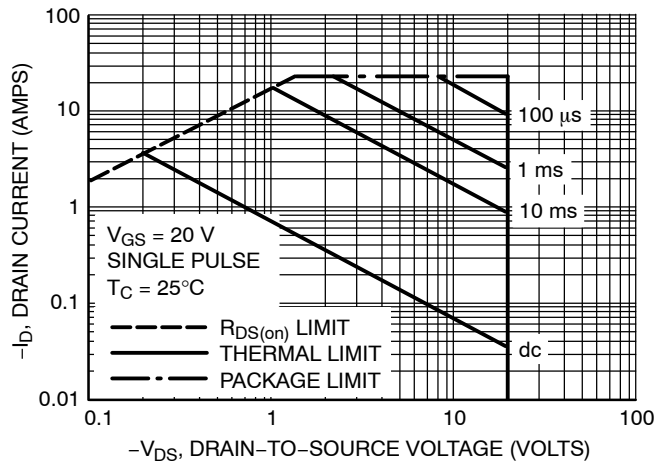


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

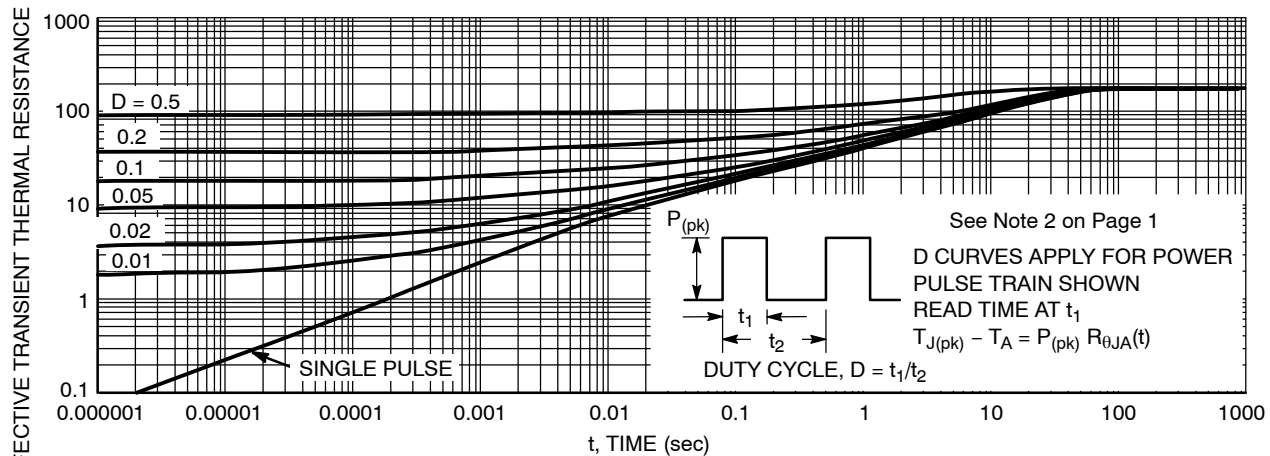


Figure 12. Thermal Response

MECHANICAL CASE OUTLINE

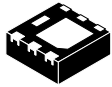
PACKAGE DIMENSIONS

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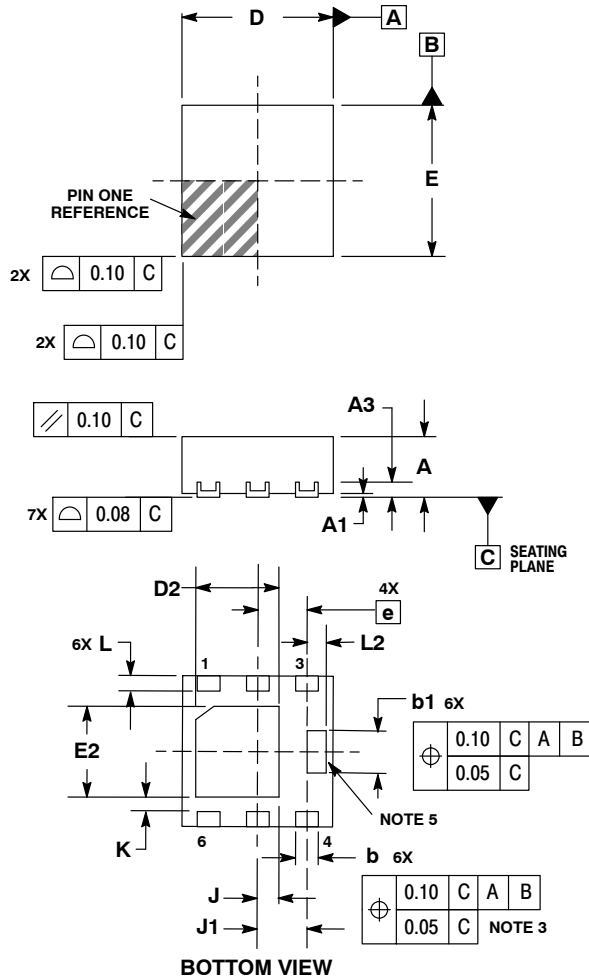


WDFN6 2x2 CASE 506AP-01 ISSUE B

DATE 26 APR 2006



SCALE 4:1



STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

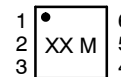
STYLE 2:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
1. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
2. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

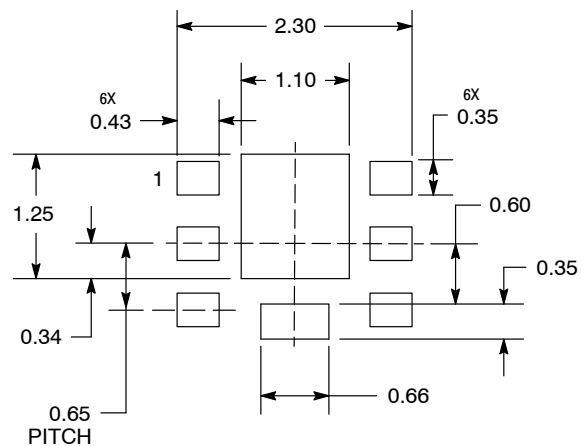
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	6 PIN WDFN 2X2, 0.65P	PAGE 1 OF 1

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