

N-Channel Power MOSFET

600V, 4A, 2.2Ω

FEATURES

- 100% UIS and R_g tested
- Advanced planar process
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	2.2	Ω
Q_g	17.2	nC

APPLICATIONS

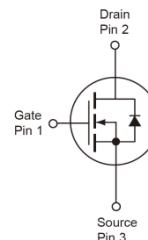
- AC/DC LED Lighting
- Power Supply



✓
ROHS
COMPLIANT

HALOGEN
FREE

ITO-220



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ^(Note 1)	I_D	4	A
		2.5	
Pulsed Drain Current ^(Note 2)	I_{DM}	16	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_{DTOT}	41.6	W
Single Pulse Avalanche Energy ^(Note 3)	E_{AS}	160	mJ
Single Pulse Avalanche Current ^(Note 3)	I_{AS}	4	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	R_{eJC}	3	°C/W
Junction to Ambient Thermal Resistance	R_{eJA}	62	°C/W

Thermal Performance Note: R_{eJA} is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. R_{eJA} is guaranteed by design while R_{eCA} is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	$V_{GS(\text{TH})}$	2.5	3	3.8	V
Gate Body Leakage	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}$, $V_{GS} = 0\text{V}$	I_{DSS}	--	--	1	μA
Drain-Source On-State Resistance (Note 4)	$V_{GS} = 10\text{V}$, $I_D = 1.4\text{A}$	$R_{DS(\text{on})}$	--	1.7	2.2	Ω
Dynamic ^(Note 5)						
Total Gate Charge	$V_{DS} = 480\text{V}$, $I_D = 2.7\text{A}$, $V_{GS} = 10\text{V}$	Q_g	--	17.2	--	nC
Gate-Source Charge		Q_{gs}	--	2.9	--	
Gate-Drain Charge		Q_{gd}	--	7.8	--	
Input Capacitance	$V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$, $f = 1.0\text{MHz}$	C_{iss}	--	582	--	pF
Output Capacitance		C_{oss}	--	38	--	
Reverse Transfer Capacitance		C_{rss}	--	1	--	
Gate Resistance		R_g	--	2	4	Ω
Switching ^(Note 6)						
Turn-On Delay Time	$V_{DD} = 300\text{V}$, $R_G = 5\Omega$, $I_D = 2.7\text{A}$, $V_{GS} = 10\text{V}$	$t_{d(on)}$	--	6	--	ns
Turn-On Rise Time		t_r	--	19	--	
Turn-Off Delay Time		$t_{d(off)}$	--	17	--	
Turn-Off Fall Time		t_f	--	21	--	
Source-Drain Diode						
Body-Diode Continuous Forward Current		I_S	--	--	4	A
Body-Diode Pulsed Current		I_{SM}	--	--	16	A
Forward Voltage ^(Note 4)	$I_S = 2.7\text{A}$, $V_{GS} = 0\text{V}$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 2.7\text{A}$ $dI_F/dt = 100\text{A}/\mu\text{s}$	t_{rr}	--	225	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.5	--	μC

Notes:

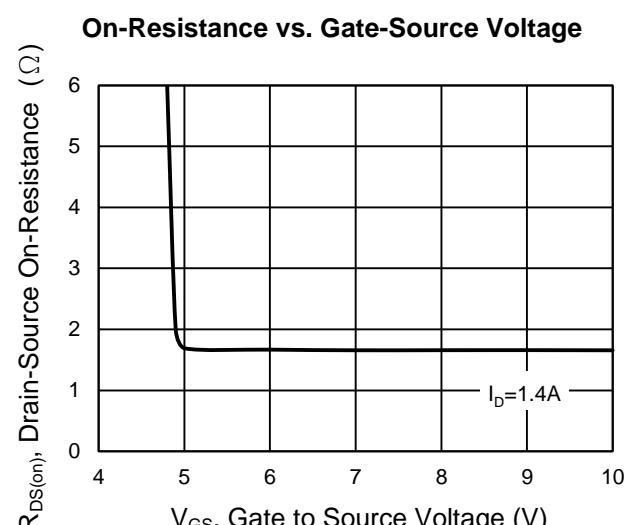
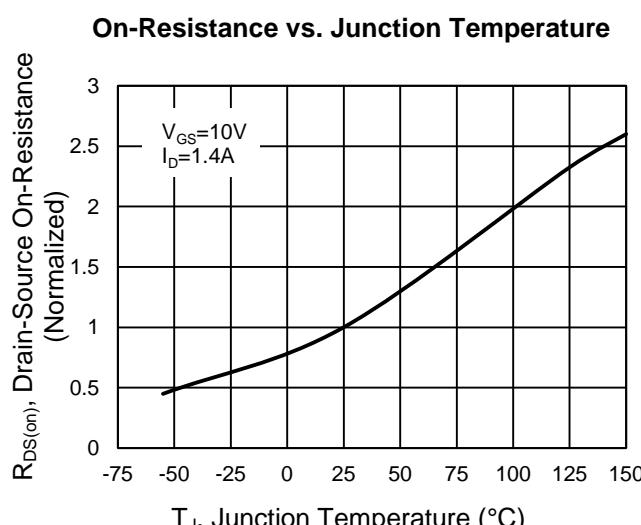
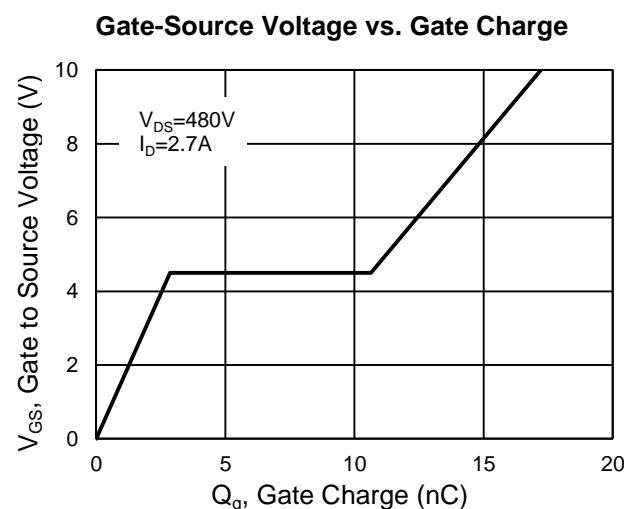
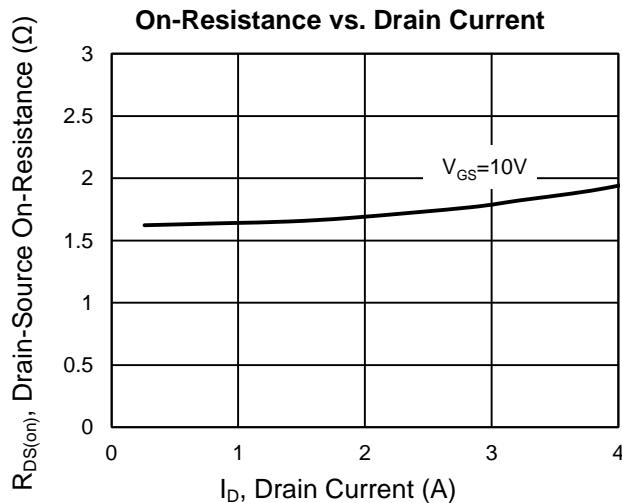
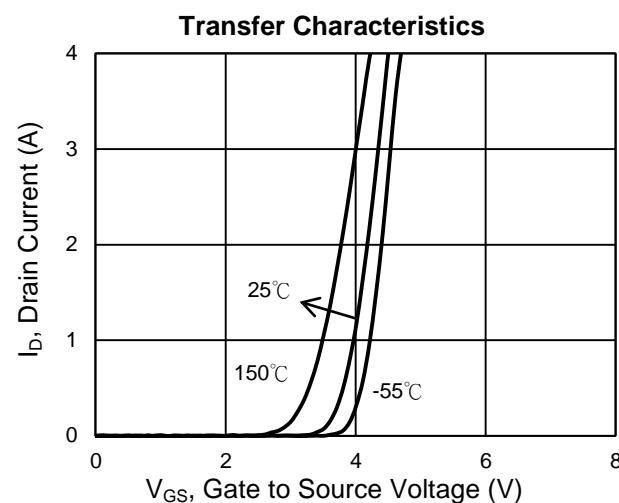
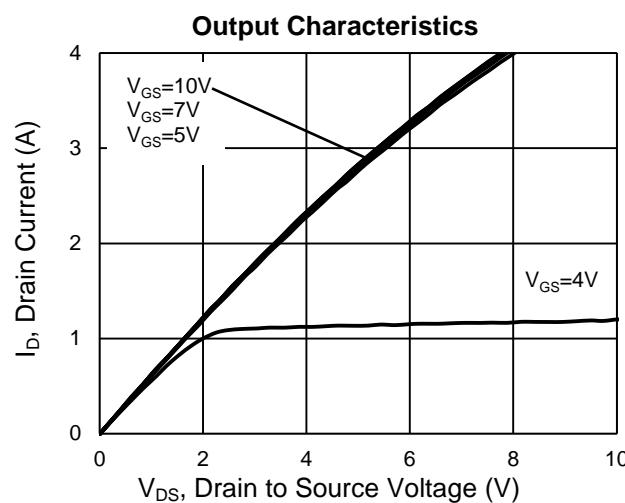
1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3. $L = 20\text{mH}$, $I_{AS} = 4\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: PW $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM4ND60CI C0G	ITO-220	50pcs / Tube

CHARACTERISTICS CURVES

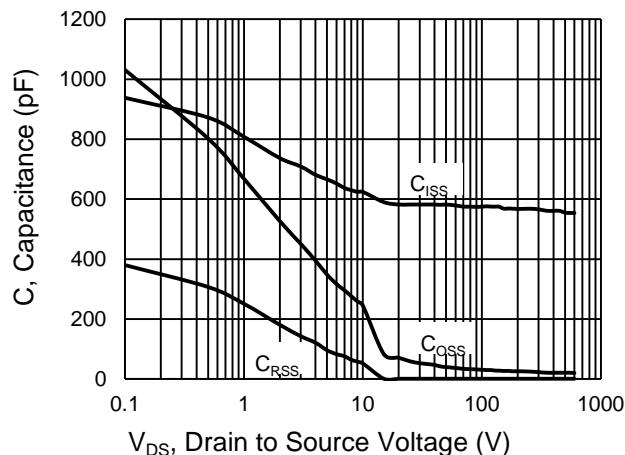
($T_C = 25^\circ\text{C}$ unless otherwise noted)



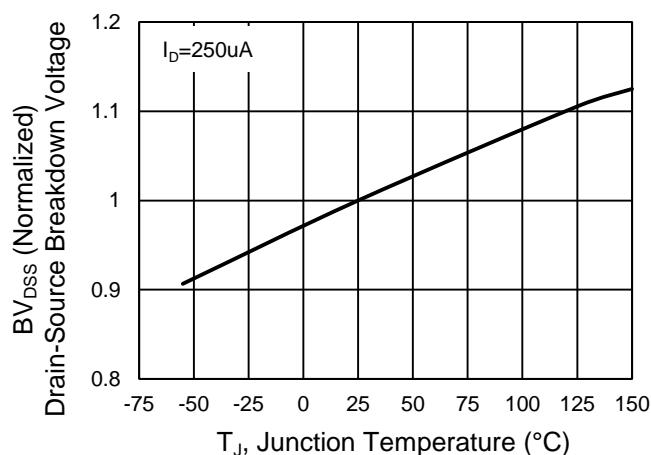
CHARACTERISTICS CURVES

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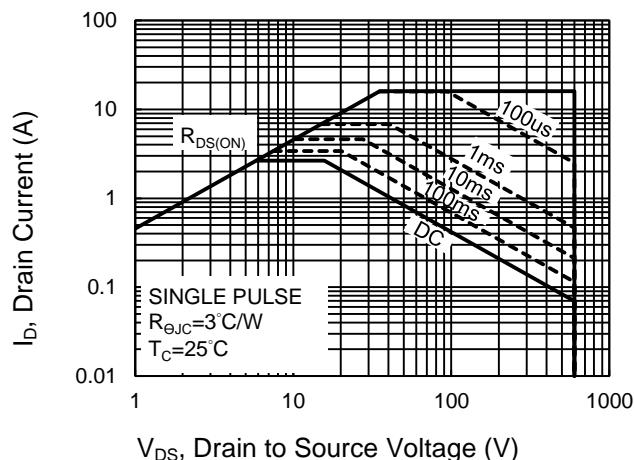
Capacitance vs. Drain-Source Voltage



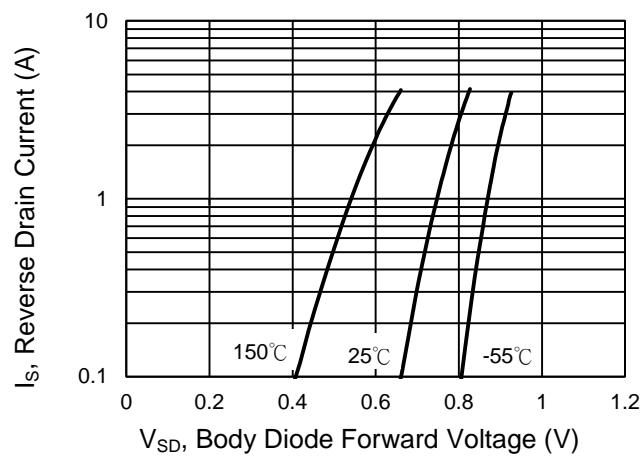
BV_{DSS} vs. Junction Temperature



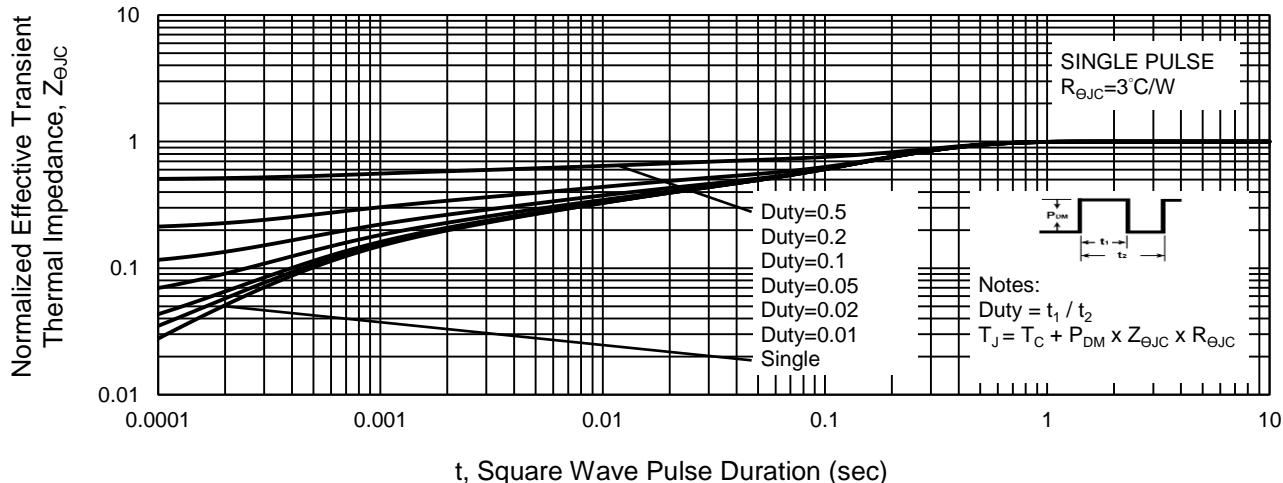
Maximum Safe Operating Area, Junction-to-Case

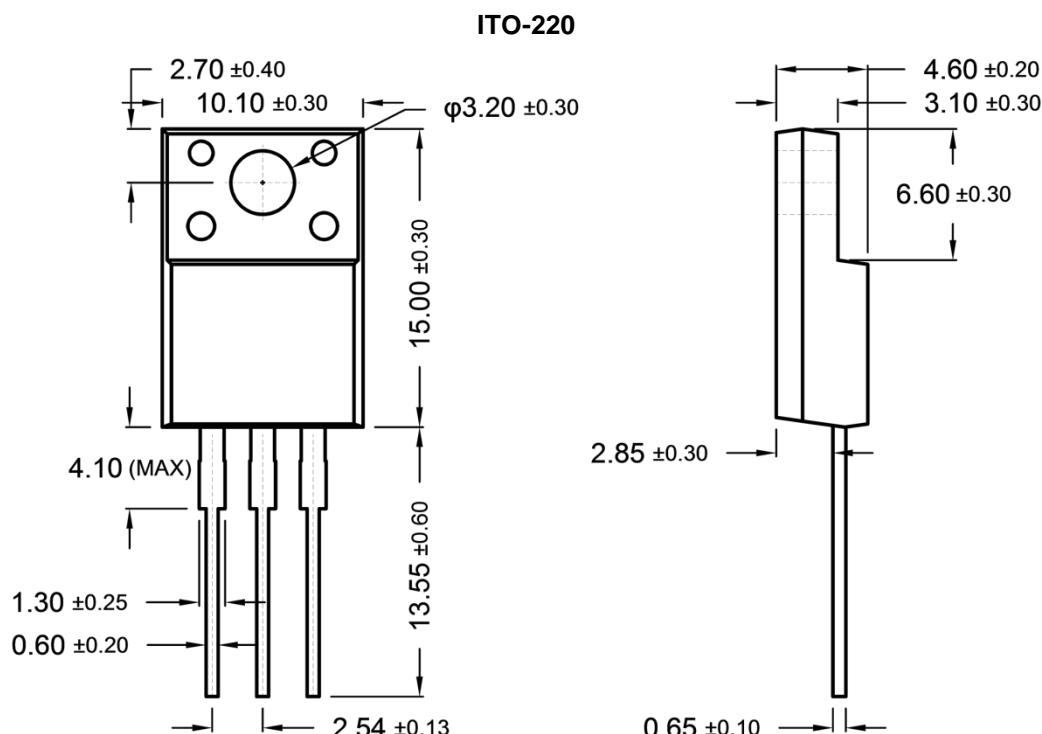
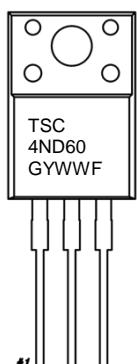


Source-Drain Diode Forward Current vs. Voltage



Normalized Thermal Transient Impedance, Junction-to-Case



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

MARKING DIAGRAM


- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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