DATASHEET

MLX120A0XY3-SRZ Non-Isolated DC-DC Power Module

7.0V_{DC} - 14V_{DC} input; 0.45V_{DC} to 2.0V_{DC} output; 120A Output Current

RoHS Compliant

The MLX120A0XY3 Digital DLynxIII^{TM} power module is a non-isolated dc-dc converter that can deliver up to 120A of output current. It operates over a wide input voltage range from 7.0V_{DC} to 14V_{DC} and provides precisely regulated output voltage programmable from 0.45V_{DC} to 2.0V_{DC} via PMBus^{TM}. The module employs an advanced PID based adjustable digital control loop which ensures loop stability, provides fast transient response and reduces amount of required output capacitance. Up to 160A of additional satellite based phase modules can be connected in parallel to form a high current common rail or a second stand-alone bus. Main features include: digital PMBus^{TM} interface, programmable enable logic and control, cycle-by-cycle output current monitoring, input and output under-voltage and over-voltage protections, under-temperature and over-temperature protections and more. The module has an extensive set of PMBus^{TM} commands for both control and monitoring of the system parameters. The MLX120A0XY3 power module is highly configurable, and yet easy to use.

Applications

- High performance ASIC with dual power rails
- Networking processor power (Broadcom, Cavium, Marvell, NXP)
- High current FPGA power (Xilinx, Intel)
- High performance ARM processor power
- Telecommunications and networking equipment
- Servers and storage applications
- Test and Measurement equipment
- Industrial equipment

Features

- Compliant to RoHS II EU Directive 2011/65/EC and amended Directive (EU) 2015/863
- Compliant to IPC-9592 (Sept. 2008), Category 2, Class TBD
- Compliant to REACH Directive (EC) No 1907/2006
- Compatible with a Pb-free or SnPn reflow soldering process
- Wide Input voltage range: 7.0V_{DC}-14V_{DC}
- Output voltage programable from 0.45V_{DC} to 2.0V via PMBus™
- Delivers up to 120 A_{DC} output current
- Supports Voltage Rails requiring 3% tolerance
- Operation of up to 4 Satellite phases in parallel(160A) as a separate bus.
- PID control and multi-phase operation provides fast transient response, reduced output capacitance, and stability.
- Tightly regulated output voltage
- Low output ripple and noise
- Fixed switching frequency
- Small size: 12.9 mm x 31.37 mm x 11.05 mm
  0.507 in x 1.235 in x 0.435 in
- Digital interface compliant to PMBus™ Rev.1.3 protocol
- Programmable enable logic with On/Off Control.
- Protections: OVP, UVP, OCP, OTP
- Cycle-by-cycle output current monitoring and protection
- Over temperature protection
- Wide operating temperature range -40°C to 85°C
- Excellent Thermal Performance – Module delivers full output @12V_{IN}, 1V_{OUT}, 70°Cambient and 200 LFM (1m/s) airflow
- Power Stages are Interleaved to reduce input and output ripple.
- UL* 62368-1, 3rd Ed. Recognized, and VDE (EN62368-1 3rd Ed.) Licensed
- ISO** 9001 and ISO14001 certified manufacturing facilities

* UL is a registered trademark of Underwriters Laboratories, Inc.
† CSA is a registered trademark of Canadian Standards Association.
‡ VDE is a trademark of Verband Deutscher Elektrotechniker e.V.
** ISO is a registered trademark of the International Organization of Standards.
# The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF).

Technical Specifications

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Operational functionality of the device is not implied at these or any other conditions in the excess of those given in the operations sections of the data sheet. Exposure to the absolute maximum ratings for extended periods may adversely affect the device reliability.

Parameter	Symbol	Min	Max	Unit
Input Voltage (continuous)	V_{IN}	-0.3	14.5	V
Operating Ambient Temperature	T_A	-40*	85	°C
Storage Temperature		-55	125	°C

* At –40°C and 7Vin, module may experience a few hiccup cycles before starting into full load

CAUTION: This power module is not internally fused. An input line fuse must always be used.
This power module can be used in a wide variety of applications, ranging from simple standalone operation to an integrated part of sophisticated power architecture. To preserve maximum flexibility, internal fusing is not included, however, to achieve maximum safety and system protection, always use an input line fuse. The safety agencies require a fast-acting fuse with a maximum rating of 60 A / two x 40A (see Safety Considerations section) in the ungrounded input. Based on the information provided in this Data Sheet on inrush energy and maximum dc input current, the same type of fuse with a lower rating can be used. Refer to the fuse manufacturer's Data Sheet for further information.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
VOUTx_SENx, IMON_SATx, TSEN, PWM_SATx, VRRDYx, VR_ENx, PROG, VRHOT, WARN#/GP		0	4	V
SM_DAT, SM_CLK, SM_ALERT#		0	5.5	V

Electrical Specifications

Unless otherwise indicated, specifications apply for all operating input voltages, resistive load and temperature conditions.

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Operating Input Voltage	All	V_{IN}	7.0		14	V_{DC}
Maximum Input Current (V_{IN}=7.0V to 14V, I_O=$I_{O,\,max}$)	All	$I_{IN,max}$		36.8		A_{DC}
Input No Load Current (V_{IN} = 12V_{DC}, I_O = 0, module enabled)	$V_{O,set}$ = 0.45V_{DC}	$I_{IN,No\ load}$		148		mA
	$V_{O,set}$ = 2.0V_{DC}	$I_{IN,No\ load}$		223		mA
Input Stand-by Current (V_{IN} = 12V_{DC}, module disabled)	All	$I_{IN,stand\text{-}by}$		50		mA
Inrush Transient	All	I^2t		1.24		A^2s
Input Reflected Ripple Current, peak-to-peak (5Hz to 20MHz, 1μH source impedance; V_{IN} =7.0 to 14V, I_O= I_{Omax} ; See Test Configurations)	All			36		mA_{p-p}
Input Ripple Rejection (120Hz)	All			-56		dB
Output Voltage Set-point accuracy over entire output range						
0 to 85°C, V_o = 0.45	All	$V_{o,\,set}$		-0.7/+1.7		$\%V_{o,\,set}$
0 to 85°C, V_o = 0.6	All	$V_{o,\,set}$		-0.6/+1.2		$\%V_{o,\,set}$
0 to 85°C, V_o = 0.7	All	$V_{o,\,set}$		-0.4/+1		$\%V_{o,\,set}$
0 to 85°C, V_o = 0.8	All	$V_{o,\,set}$		-0.4/+0.8		$\%V_{o,\,set}$
0 to 85°C, V_o = 0.9	All	$V_{o,\,set}$		-0.3/+0.7		$\%V_{o,\,set}$
0 to 85°C, V_o = 1.0	All	$V_{o,\,set}$		-0.2/+0.6		$\%V_{o,\,set}$
0 to 85°C, V_o = 1.2	All	$V_{o,\,set}$		-0.2/+0.5		$\%V_{o,\,set}$
0 to 85°C, V_o = 1.8	All	$V_{o,\,set}$		-0.3/+0.07		$\%V_{o,\,set}$
0 to 85°C, V_o = 2.0	All	$V_{o,\,set}$		-0.4/+0.0		$\%V_{o,\,set}$

Technical Specifications (continued)

Electrical Specifications (continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Output Voltage Set-point accuracy over entire output range						
-40 to 85°C, V_o = 0.45	All	$V_{o, set}$		-2.2/+1.7		%$V_{o, set}$
-40 to 85°C, V_o = 0.6	All	$V_{o, set}$		-1.6/+1.2		%$V_{o, set}$
-40 to 85°C, V_o = 0.7	All	$V_{o, set}$		-1.2/+1		%$V_{o, set}$
-40 to 85°C, V_o = 0.8	All	$V_{o, set}$		-1/+0.8		%$V_{o, set}$
-40 to 85°C, V_o = 0.9	All	$V_{o, set}$		-0.8/+0.7		%$V_{o, set}$
-40 to 85°C, V_o = 1.0	All	$V_{o, set}$		-0.7/+0.6		%$V_{o, set}$
-40 to 85°C, V_o = 1.2	All	$V_{o, set}$		-0.5/+0.5		%$V_{o, set}$
-40 to 85°C, V_o = 1.8	All	$V_{o, set}$		-0.5/+0.1		%$V_{o, set}$
-40 to 85°C, V_o = 2.o	All	$V_{o, set}$		-0.5/+0.0		%$V_{o, set}$

Note:

The 5.5V and 3.3V Voltage rails on the module are only to be used to power Satellite units (SLX series) and pull-up resistors needed for the POL module. Use with Pull-up resistors as recommended in the datasheet. Do not use these voltage rails for any other purpose.

Technical Specifications (continued)

Electrical Specifications (continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Voltage Regulation						
Line Regulation (V_{IN}=$V_{IN, min}$ to $V_{IN, max}$), V_{OUT} < 1V	All			0.22		%$V_{o, set}$
Line Regulation (V_{IN}=$V_{IN, min}$ to $V_{IN, max}$), V_{OUT} ≥1V	All			0.2		%$V_{o, set}$
Load Regulation (I_o=$I_{o, min}$ to $I_{o, max}$), V_{OUT} < 1V	All			0.4		%$V_{o, set}$
Load Regulation (I_o=$I_{o, min}$ to $I_{o, max}$), V_{OUT} ≥1V	All			0.3		%$V_{o, set}$
PMBus Adjustable Output Voltage Range	All	V_O	0.45		2.00	V_{DC}
PMBus Output Voltage Adjustment Step Size	All			3.904		mV
Remote Sense Range	All				0.5	V_{DC}
Input Ripple (V_{IN}=$V_{IN, nom}$ and I_O=$I_{O, min}$ to $I_{O, max}$ and Ta=25°C Cin = 8 x 1 µF ||16 x 10 µF || 4 x 22 µF ||2 x 560 µF)				105 @0.45V_o		mV_{pk-pk}
Peak-to-Peak (5Hz to 20MHz bandwidth)	All			116 @2V_o		mV_{pk-pk}
Output Ripple @580kHz (V_{IN}=$V_{IN, nom}$ and I_O=$I_{O, min}$ to $I_{O, max}$ and Ta=25°C Co = 4x0.1 µF ||4x0.047 µF || 15x22 µF ||73x47 µF || 6x470 µF				1.2mV@ 0.45V_o		mV_{pk-pk}
Peak-to-Peak (5Hz to 20MHz bandwidth)	All			2.2mV@ 2V_o		mV_{pk-pk}
RMS (5Hz to 20MHz bandwidth)	All			0.8mV		mV_{rms}
Output Current (in source mode)	All	I_o		120		A_{DC}
Output Current Limit Inception (Hiccup Mode)	All	$I_{o, lim}$		197		$A_{DC,max}$
Efficiency	$V_{O,set}$ = 0.45V_{DC}			80.5		%
V_{IN}= 12V_{DC}, T_A=25°C	$V_{O, set}$ = 0.6V_{DC}			84.2		%
I_O=$I_{O, max}$, V_O= $V_{O,set}$	$V_{O, set}$ = 0.8V_{DC}			87.5		%
	$V_{O,set}$ = 1.0V_{DC}	η		89.7		%
	$V_{O,set}$ = 1.8V_{DC}			93.2		%
	$V_{O,set}$ = 2.0V_{DC}			93.7		%
Switching Frequency (Fixed)	All	f_{sw}		580		kHz

Feature Specifications

Unless otherwise indicated, specifications apply for all operating input voltages, resistive load and temperature conditions. See Feature Descriptions for additional information.

Parameter	Device	Symbol	Min	Typ	Max	Units
On/Off Signal Interface (Negative Logic)#						
Logic High (Module OFF)						
Input High Current	All	I_{IH}			5	uA
Input High Voltage	All	V_{IH}	1.97		3.3	V
Logic Low (Module ON)						
Input Low Current	All	I_{IL}			5	uA
Input Low Voltage	All	V_{IL}	0		1.42	V
Turn-On Delay and Rise Times (V_{IN}=$V_{IN, nom}$, I_O=$I_{O, max}$, V_O to within ±1% of steady state)						
Case 1: Input power is applied for at least one second and then the On/Off input is enabled (delay from instant at which Von/Off is enabled until V_o = 10% of $V_{o, set}$)	All	Tdelay		2.5		msec
Case 2: On/Off input is enabled and then input power is applied (delay from instant when V_{IN} = $V_{IN, min}$ until V_o = 10% of $V_{o, set}$)	All	Tdelay		1.1		msec
Output voltage Rise time (time for V_o to rise from 10% of $V_{o,set}$ to 90% of $V_{o, set}$)	All	Trise		12.0		msec
Output voltage overshoot (T_A = 25°C V_{IN}= $V_{IN, min}$ to $V_{IN, max}$,I_O = $I_{O, min}$ to $I_{O, max}$) With or without maximum external capacitance					3.5	% $V_{O, set}$

Technical Specifications (continued)

Feature Specifications (continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Over Temperature Protection (See Thermal Considerations section)	All	T_{OT}		125		°C
PMBus Over Temperature Warning Threshold *	All	T_{WARN}		110		°C
Input Undervoltage Lockout						
Turn-on Threshold	All			6.25		V_{DC}
Turn-off Threshold	All			5.75		V_{DC}
Hysteresis	All			0.5		V_{DC}
PMBus Input Under Voltage Lockout Thresholds (Do not change)	All			5.75	14	V_{DC}
Resolution of Input Under Voltage Threshold	All			250		mV
VRRDYx – PGOOD Equivalent Signal Interface Open Drain, $V_{supply} \leq 3.6V_{DC}$, Recommended pull-up circuit: 10K resistor with 3.3Vsupply						
Output Low voltage (4mA Drive)	All				0.3	V
Output Leakage (Vpad = 0 to 3.6V)	All				±5	µA

* Over temperature Warning – Warning may not activate before alarm and unit may shutdown before warning.

General Specifications

Parameter	Device	Min	Typ	Max	Unit
Calculated MTBF (I_O=0.8$I_{O, max}$, T_A=40°C) Telecordia Issue 4 Method 1 Case 3	All		35,871,318		Hours
Weight			9.7(0.342)		g (oz.)

Digital Interface Specifications

Unless otherwise indicated, specifications apply for all operating input voltages, resistive load and temperature conditions. See Feature Descriptions for additional information.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
PMBus Signal Interface Characteristics						
Input High Voltage (SM_DAT, SM_ALERT#)		V_{IH}	2.1		5	V
Input Low Voltage (SM_DAT, SM_ALERT#)		V_{IL}			0.8	V
Input Leakage (SM_DAT, SM_CLK, VR_ENx)	Vpad = 0 – 3.6V	I_{IH}	-1		1	µA
Output Low Voltage (Open-Drain Outputs – 4mA drive, SM_DAT, SM_ALERT#)	I_{OUT}=4mA	V_{OL}			0.3	V
Output Leakage (Open-drain outputs – 4mA drive, VRRDYx, SM_DAT, SM_ALERT#)	V_{OUT}= 0 – 3.6V	I_{OH}	-5		5	µA
Pin capacitance		C_O		0.7		pF
PMBus Operating frequency range		FPMB	10		1000	kHz
Measurement System Characteristics						
Output current measurement range		$I_{OUT(rng)}$	0	511.5		A
Output current measurement accuracy -40 to 85°C		I_{ACC}		-9/+5		%
Output Current Resolution (settable vi a PMBus)			0.25		0.5	mA
Temperature measurement accuracy @12V_{IN}, 25 to 85°C		T_{ACC}		10		°C
Temperature measurement resolution		$T_{MEAS(res)}$		1		°C
V_{IN} measurement range		$V_{IN(rng)}$	0		16.8	V
V_{IN} measurement accuracy		$V_{IN, ACC}$		±2		%
V_{IN} measurement resolution		$V_{IN, RES}$		31.25		mV
V_{OUT} measurement range		$V_{OUT(rng)}$	0		2.55	V
V_{OUT} measurement resolution		$V_{OUT(res)}$		4		mV
V_{OUT} measurement accuracy		$V_{OUT, ACC}$		±2		%

Technical Specifications (continued)

Characteristic Curves

The following figures provide typical characteristics for the 120A Master DLynxIII[TM] module at 0.45Vo and 25°C.

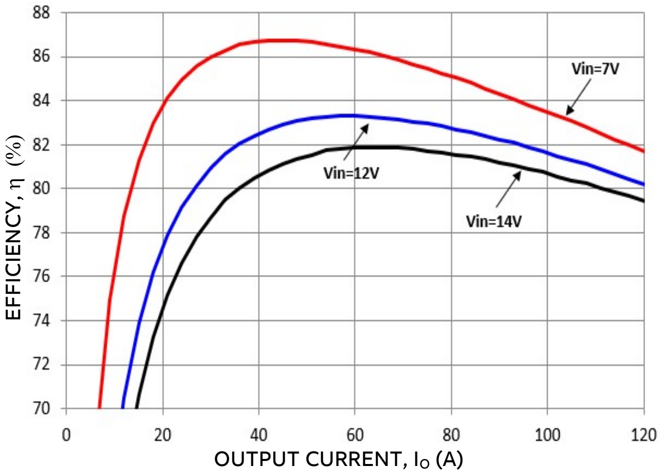

Figure 1. Converter Efficiency versus Output Current.

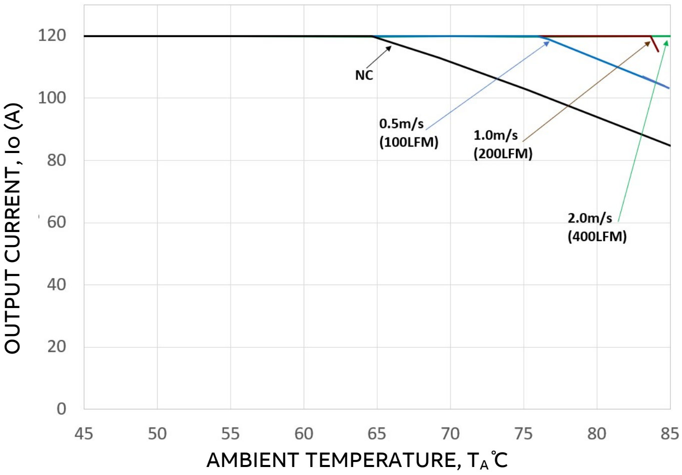

Figure 2. Derating Output Current versus Ambient Temperature and Airflow.

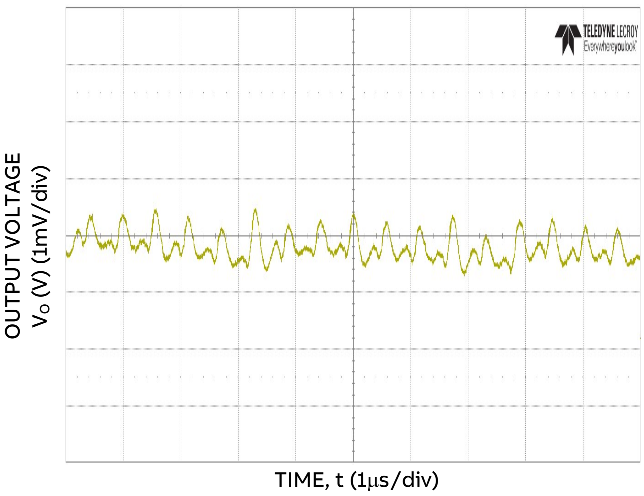

Figure 3. Typical output ripple (C_O=4x0.047μF +4x0.1μF + 15x22μF + 73x47μF + 6x470μF polymer, V_{IN} = 12V, I_o = $I_{o,max}$).

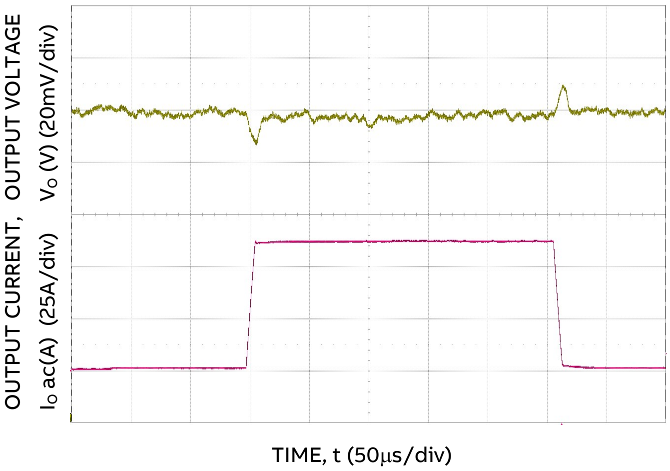

Figure 4. Trans. Resp. to 10A/µs Load Change from 25% to 75% at $12V_{IN}$, Co=4x0.047µF +4x0.1µF + 15x22µF + 73x47µF + 6x470µF polymer

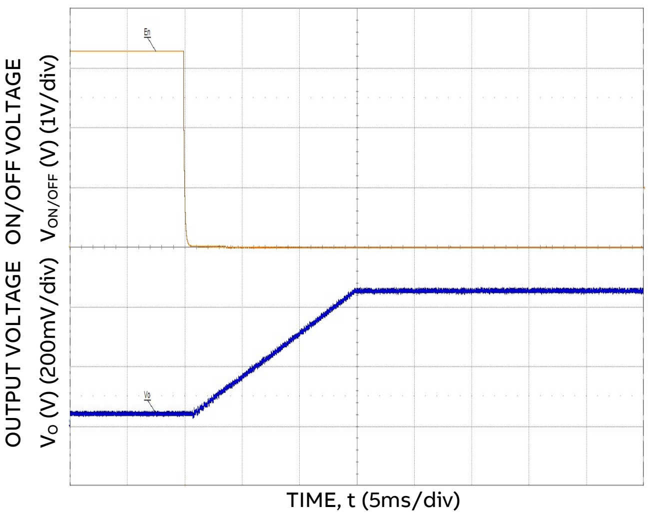

Figure 5. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

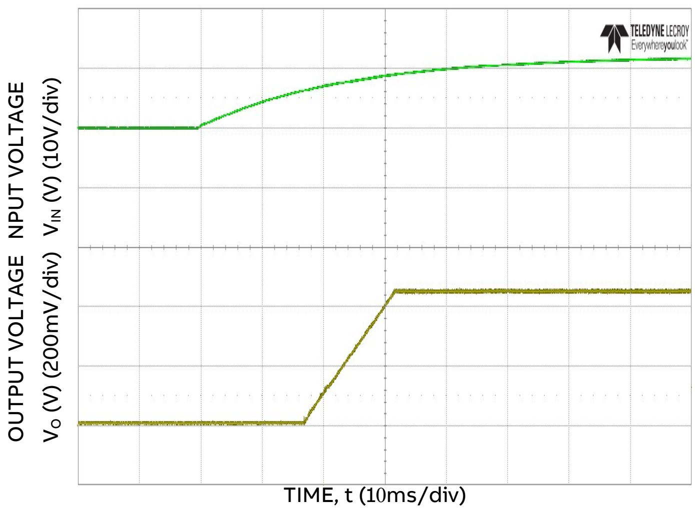

Figure 6. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Technical Specifications (continued)

Characteristic Curves

The following figures provide typical characteristics for the 120A Master DLynxIII[TM] module at 1.0V_o and 25°C.

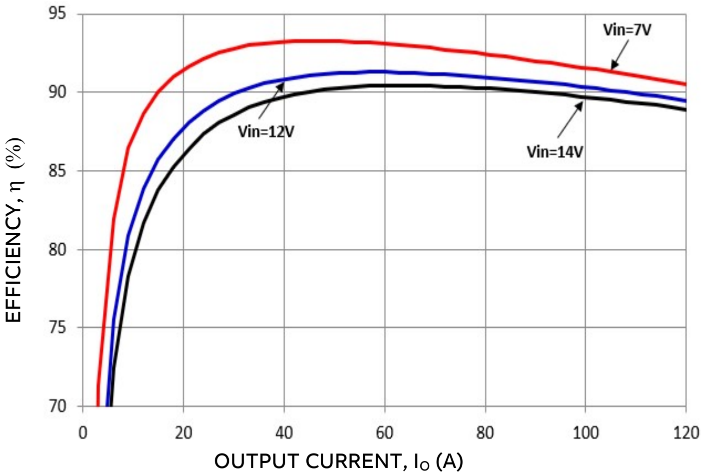

Figure 7. Converter Efficiency versus Output Current.

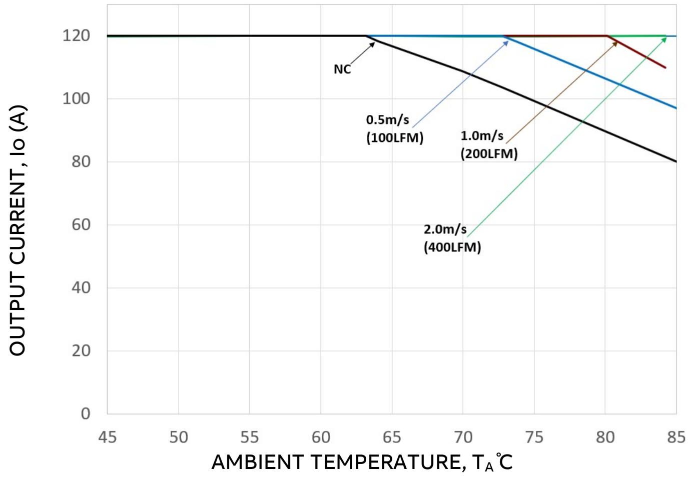

Figure 8. Derating Output Current versus Ambient Temperature and Airflow.

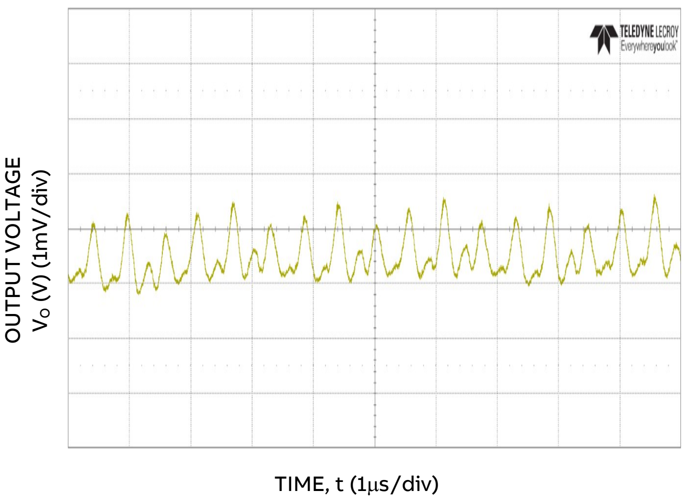

Figure 9. Typical output ripple(C_O=4x0.047µF +4x0.1µF + 15x22µF + 73x47µF + 6x470µF polymer, V_{IN} = 12V, I_o = $I_{o,max}$).

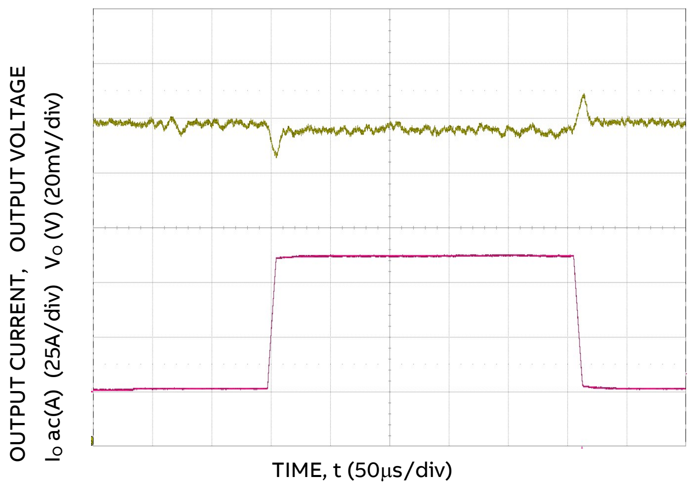

Figure 10. Trans. Resp. to 10A/µs Load Change from 25% to 75% at 12V_{IN}, Co=4x0.047µF +4x0.1µF + 15x22µF + 73x47µF + 6x470µF polymer

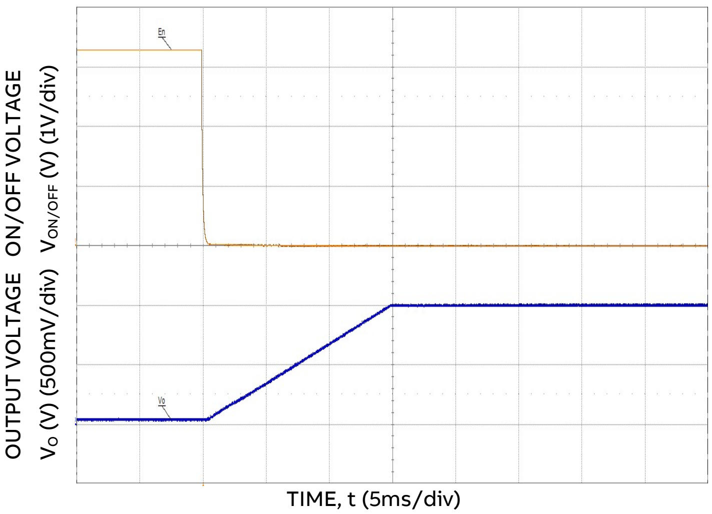

Figure 11. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

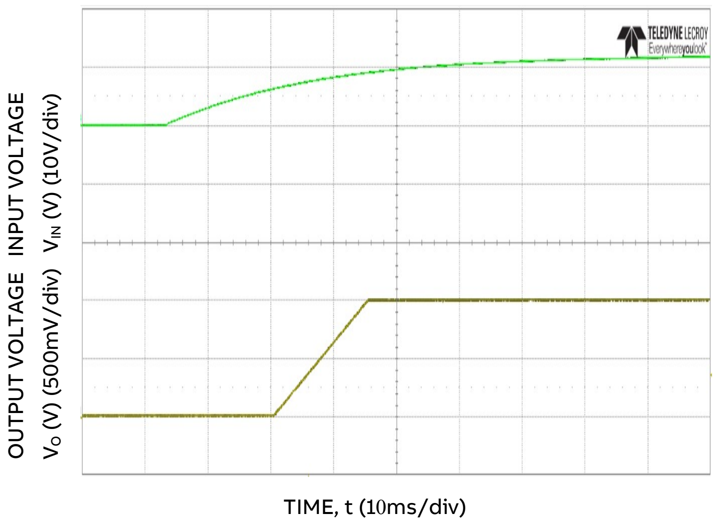

Figure 12. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Technical Specifications (continued)

Characteristic Curves

The following figures provide typical characteristics for the 120A Master DLynxIII^{TM} module at 1.5V_o and 25°C.

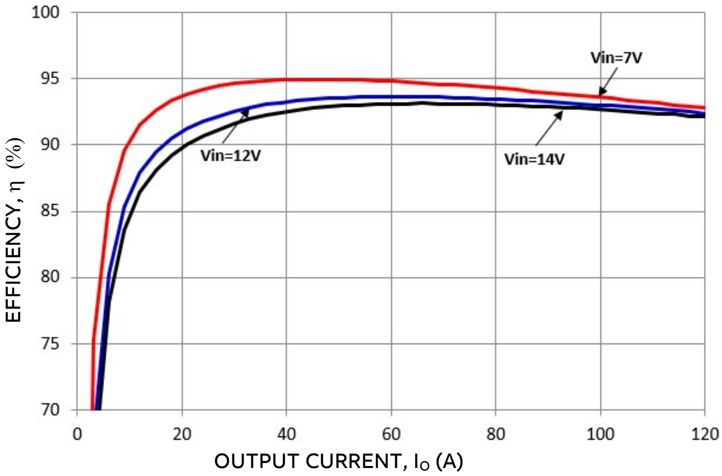

Figure 13. Converter Efficiency versus Output Current.

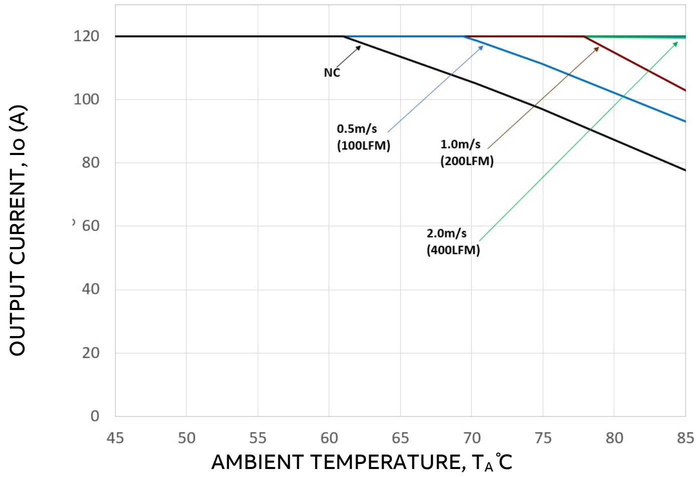

Figure 14. Derating Output Current versus Ambient Temperature and Airflow.

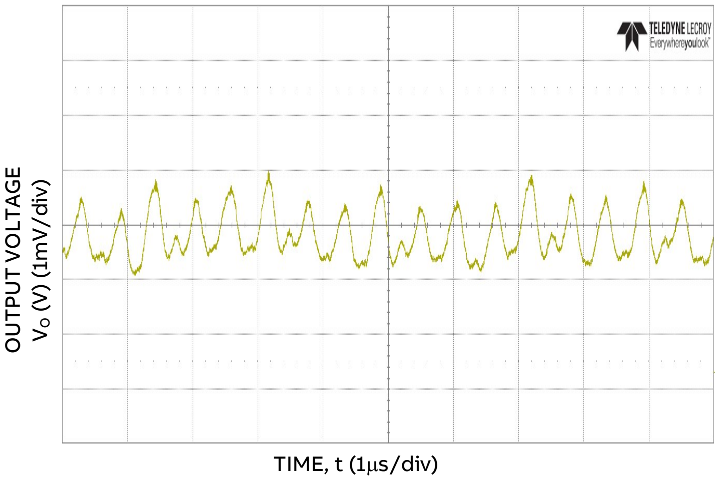

Figure 15. Typical output ripple(C_O=4x0.047µF +4x0.1µF + 15x22µF + 73x47µF + 6x470µF polymer, V_{IN} = 12V, I_o = $I_{o,max}$).

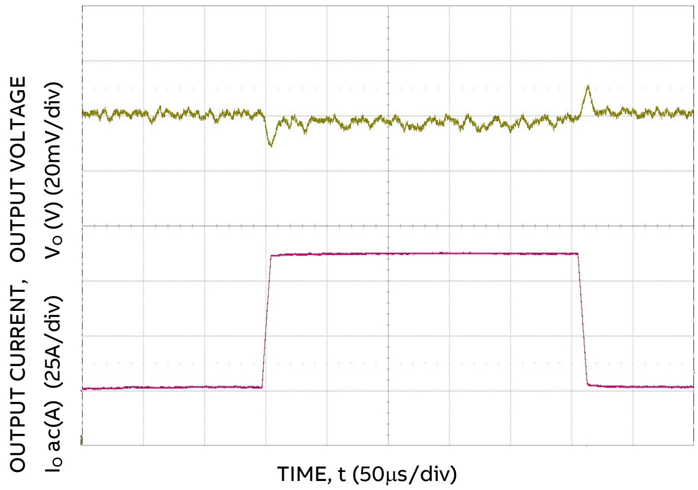

Figure 16. Trans. Resp. to 10A/µs Load Change from 25% to 75% at 12V_{IN}, Co=4x0.047µF +4x0.1µF + 15x22µF + 73x47µF + 6x470µF polymer

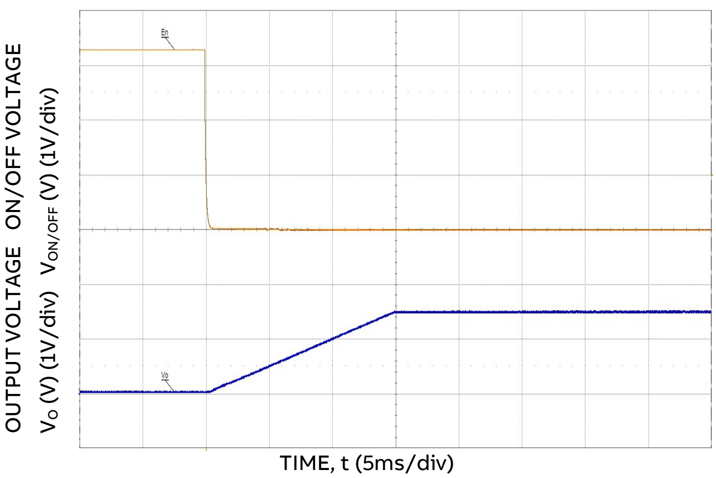

Figure 17. Typical Start-up Using On/Off Voltage (I_o = $I_{o,max}$).

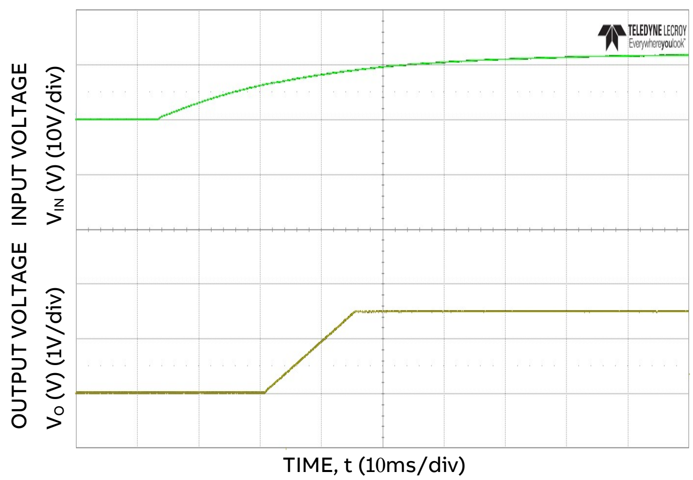

Figure 18. Typical Start-up Using Input Voltage (V_{IN} = 12V, I_o = $I_{o,max}$).

Technical Specifications (continued)

Characteristic Curves

The following figures provide typical characteristics for the 120A Master DLynxIII^{TM} module at $2V_o$ and 25°C.

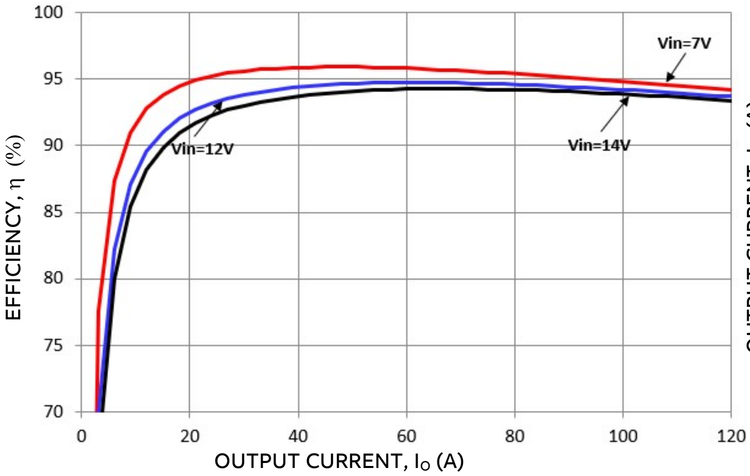

Figure 19. Converter Efficiency versus Output Current.

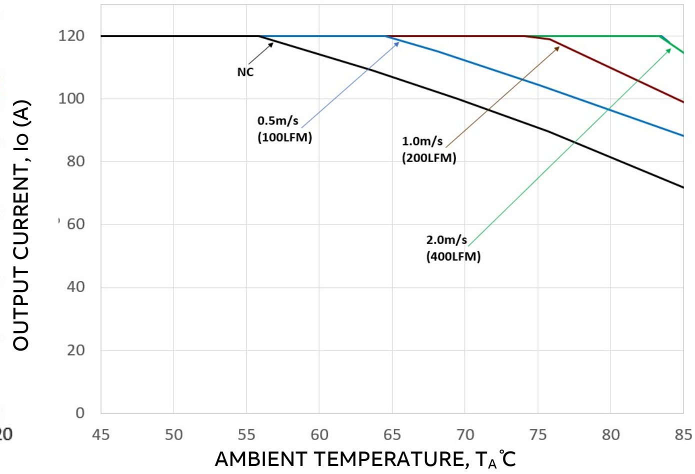

Figure 20. Derating Output Current versus Ambient Temperature and Airflow.

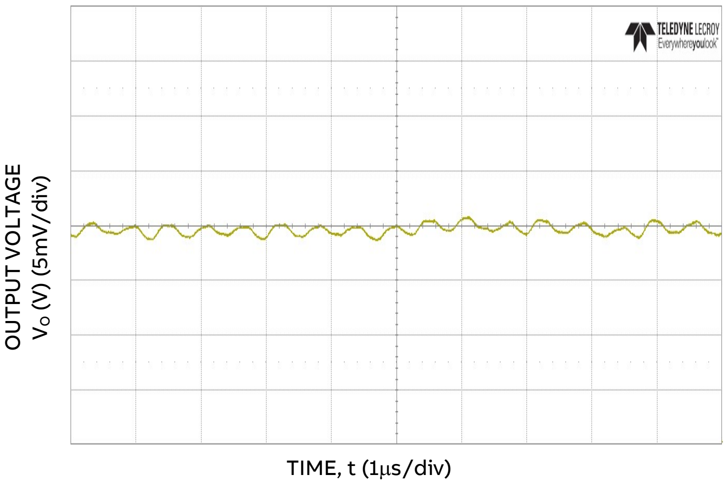

Figure 21. Typical output ripple (C_O=4x0.047µF +4x0.1µF +

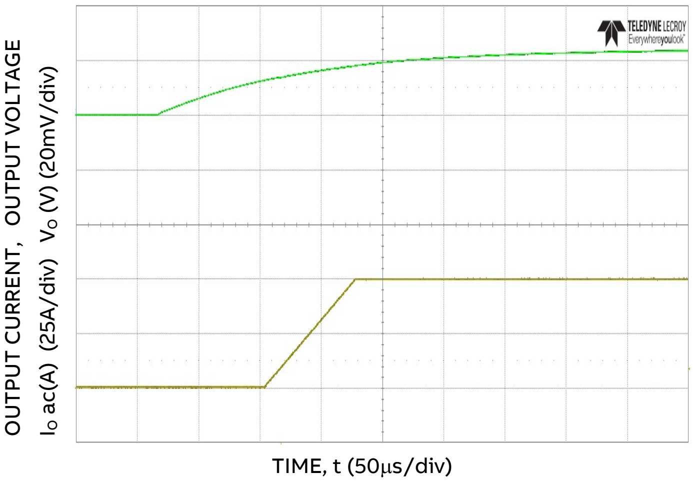

Figure 22. Trans. Resp. to 10A/µs Load Change from 25% to 75% at $12V_{IN}$, Co=4x0.047µF +4x0.1µF + 15x22µF + 73x47µF + 6x470µF polymer

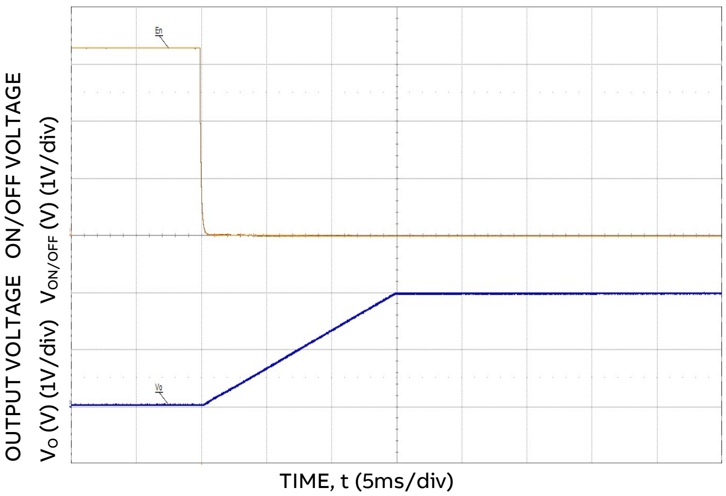

Figure 23. Typical Start-up Using On/Off Voltage ($I_o = I_{o,max}$).

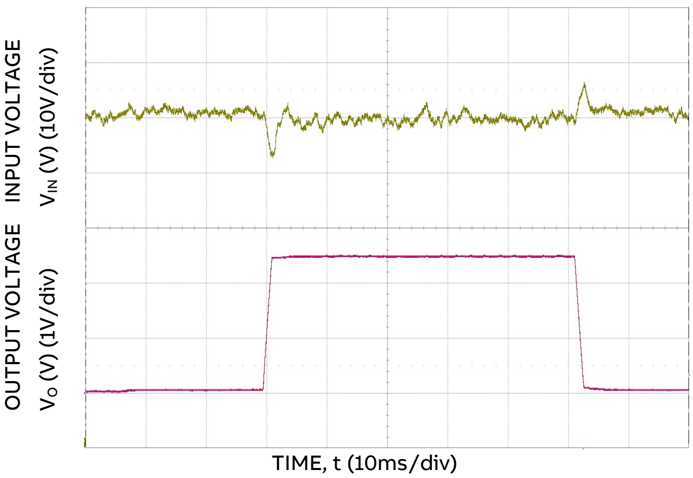

Figure 24. Typical Start-up Using Input Voltage (V_{IN} = 12V, $I_o = I_{o,max}$).

Technical Specifications

Design Considerations

Input Filtering

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Figure 25 shows the input ripple voltage for various output voltages at 100% of load current with different input capacitor combinations to achieve 1.5 % and lower input ripple. Since voltage used was $12V_{IN}$, all the curves stayed below the 180mV(1.5%) threshold

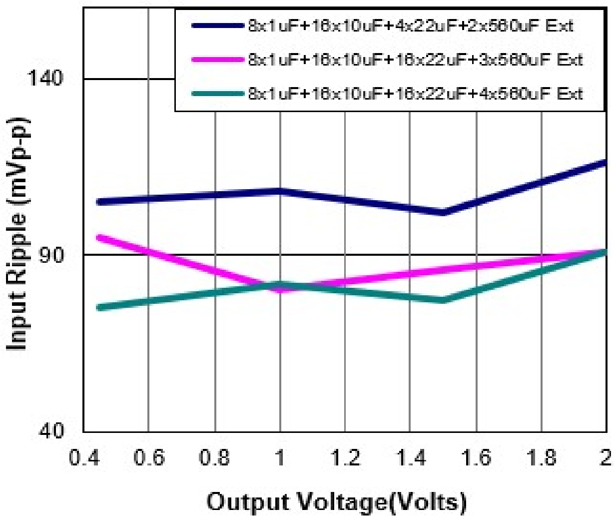

Figure 25. Input ripple voltage for various output voltages with three input capacitor combinations at full load. Input voltage is 12V.

These caps were placed at the bottom of the board and directly under each of the phases as shown in the layout of the evaluation board (Fig. 31). Each phase had a minimum of 2x1uF and 3x10uF closest to the pins.

Output Filtering

These modules are designed for low output ripple voltage and will meet stringent output ripple.

Figure 26 provides output ripple information various output voltages and full load current for different levels of capacitance. Ceramic capacitance will reduce output ripple and improve the transient performance of the module.

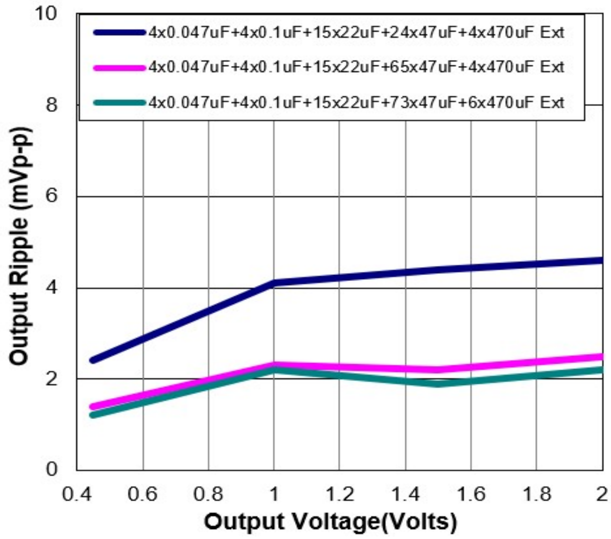

Figure 26. Peak to peak output ripple voltage for various output voltages with external capacitors at the output (120A load). Input voltage is 12V.

Transient Testing

Module performance for different transient conditions at rated output capacitance.

Voltage Rail (volts)	Step Load (%) of full load	Load Slew Rate (A/ µsec)	ΔV Variation (%)
0.45V[1]	50	10	-2.95% to 2.15%
1V[2]	50	10	-1.44% to 0.88%
1.5V[3]	50	10	-0.77% to 0.74%
2.0V[4]	50	10	-0.73% to 0.66%

[1] Kp=43, Ki=24,Kd=58,Kpole1=5,Kpole2=7

[2] Kp=41, Ki=26,Kd=56,Kpole1=5,Kpole2=7

[3] Kp=41, Ki=24,Kd=56,Kpole1=5,Kpole2=7

[4] Kp=40, Ki=24,Kd=56,Kpole1=5,Kpole2=7

Technical Specifications (continued)

Safety Considerations

For safety agency approval, the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL* 62368-1, 3rd Ed. Recognized, and VDE (EN62368-1, 3nd Ed.) Licensed.

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV) or ES1, the input must meet SELV/ES1 requirements. The power module has extra low voltage (ELV) outputs when all inputs are ELV.

The MLX120A0X model was tested using an external Littelfuse 456 series 60A and two 40A, fast-acting fuses in the ungrounded input. Two 40A fuses are recommended for input voltages <8Vdc. The maximum hot spot temperature on IC200/C202 shall not exceed 120/115°C.

Remote On/Off

The MLX120 module can be turned ON and OFF either by using the ON/OFF pin (Analog interface) or through the PMBus interface (Digital). The module can be configured in a number of ways through the PMBus interface to react to the ON/OFF input:

- Module ON/OFF can controlled only through the analog interface (digital interface ON/OFF commands are ignored).
- Module ON/OFF can controlled only through the PMBus interface (analog interface is ignored).
- Module ON/OFF can be controlled by either the analog or digital interface.

The default state of the module (as shipped from the factory) is to be controlled by the PMBus interface and analog interface. Module control through the digital interface must be made through PMBus. These changes can be made and written to non-volatile memory on the module so that it is remembered for subsequent use.

The ON/OFF pin should not be left floating and must be pulled either high or low .

Digital On/Off

Please see the Digital Feature Descriptions section.

Monotonic Start-up and Shutdown

The module has monotonic start-up and shutdown behavior on the output for any combination of rated input voltage, output current, and operating temperature range.

Startup into Pre-biased Output

The module will start into a pre biased output on output as long as the pre bias voltage is 15% less than the set output voltage.

Remote Sense

The power module has a differential Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-) for the output. The voltage drop between the sense pins and the VOUT and GND pins of the module should not exceed 100mV.

Technical Specifications (continued)

Overcurrent Protection (OCP)

To provide protection in a fault (output overload) condition, the unit is equipped with internal current limiting circuitry on the output and can endure current limiting continuously. The module's overcurrent response is to hiccup forever. OCP response can be changed with a PMBus command.

Overtemperature Protection

To provide protection in a fault condition, the unit has a thermal shutdown circuit. The unit will shut down if the overtemperature threshold of 125°C (typ) is exceeded at the thermal reference point Tref . Once the unit goes into thermal shutdown, it will wait to cool down to 97% of set limit before attempting to restart.

Power Good

Power good needs external pull up resistor. The pins are called VRRDY1 and VRRDY2 (loop1/loop2) and their thresholds are specified via PMbus.

An example of Power Good / VRRDY behavior is shown below. The top green waveform is the slowly rising input voltage and the bottom brown waveform is the output voltage. As soon as the output voltage crosses the VRRDY1 threshold, the pin is pulled high as seen in the scope capture.

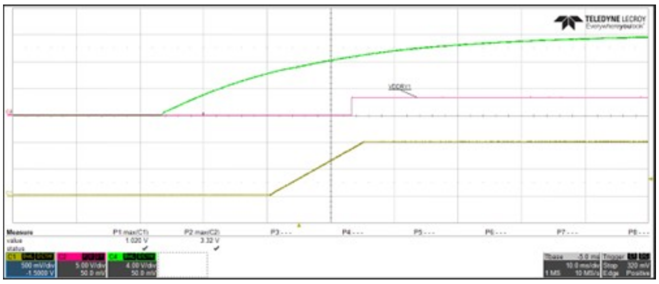

Figure 27. V_{IN}, VRRDY1 and Vout1 waveform.

Start-up procedure

ON/OFF

The MLX120A0XY3-SRZ is a programmable ON/OFF logic power module. The default state of the module is Negative Logic The module is ON when the ON/OFF pin is at a "logic low" state, and OFF when it is at "logic high" state. Positive ON/OFF logic can be implemented through PMBus control.

The module could be turned ON and OFF from an external enable signal or by the OPERATION 0x01 command. Desired behavior is set by ON_OFF_CONFIG 0x02 command.

Input overvoltage and undervoltage protections

The input overvoltage and undervoltage protections prevent the MLX120A0XY3-SRZ from operating when the input is above or falls below preset thresholds.

Customers are strongly advised not to increase the preset input overvoltage limit or decrease input undervoltage limit as it may result in compromising product safety. This is a violation of the module's absolute maximum and minimum ratings which will void the product warranty.

The input overvoltage and undervoltage protections could be adjusted by the following commands:

VIN_OV_FAULT_RESPONSE 0x56, VIN_OV_FAULT_LIMIT 0x55 and
VIN_UV_WARN_LIMIT 0x58.

See commands description for more details.

Output overvoltage and undervoltage protections

The MLX120A0XY3-SRZ offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits.

The MLX120A0XY3-SRZ overvoltage and undervoltage behavior ca be configured through the following commands:
VOUT_OV_FAULT_RESPONSE 0x41,
VOUT_UV_FAULT_RESPONSE 0x45,
VOUT_OV_FAULT_LIMIT 0x40, VOUT_OV_WARN_LIMIT 0x42, VOUT_UV_WARN_LIMIT 0x43, and
VOUT_UV_FAULT_LIMIT 0x44.
See Application Note for more details.

Output overcurrent protection

Output overcurrent protection prevents excessive forward current through the module and the load during abnormal operation. Overcurrent protection is cycle-by-cycle in nature. This is managed by IOUT_OC_FAULT_LIMIT 0x46.

Customers are strongly advised not to increase the preset output overcurrent limits or decrease output undercurrent limits as it may result in compromising product safety. This is a violation of the module's absolute maximum and minimum ratings which will void the product warranty.

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Technical Specifications (continued)

The output overcurrent warning limits and fault response is managed by the following commands

IOUT_OC_WARN_LIMIT 0x4A,
IOUT_OC_FAULT_RESPONSE 0X47.

Overtemperature protection

The MLX120A0XY3-SRZ overtemperature protection ensures that the temperature inside the module is below all the component's temperature maximum limit.

The overtemperature protections are managed by the following commands: OT_FAULT_RESPONSE 0x50, OT_WARN_LIMIT 0x51.

Monitoring through SMBAlert or SALERT pin

The MLX120A0XY3-SRZ controller can report fault conditions by changing the state of the SMBALERT pin, which is asserted when any number of preconfigured fault conditions occur. The module can also be monitored continuously for any number of power conversion parameters. Some of most useful fault monitoring commands are: STATUS_BYTE 0x78, STATUS_WORD 0x79, STATUS_VOUT 0x7A, STATUS_IOUT 0x7B, STATUS_INPUT 0x7C, STATUS_TEMPERATURE 0x7D.

Control loop tuning

The heart of MLX120A0XY3-SRZ is a fully digital controller IC with state-of-the-art PID Control. By default, this control loop is stable for recommended output capacitance and loads. However, it may be further tuned to achieve higher performance under more specific application requirements. Since the control scheme is digital from end to end, there is no dependence upon external compensation networks. This simplifies the design process by removing such considerations as temperature and process variation of passive components. Control parameters are set through the 0xD0 PMBus command

Non-volatile memory management

The MLX120A0XY3-SRZ has internal non-volatile memory where the module's configurations are stored.

During the initialization process, the MLX120A0XY3-SRZ checks for stored values contained in its internal non-volatile memory. The MLX120 offers up to 24 writes to configure basic module parameters such as output voltage setpoint, fault operation settings, etc. It also allows loading of pre-installed configuration file from up to 15 options to help set multiple MLX modules powering different rails on a common PMBus.

Layout considerations

The evaluation board layout and schematic files are available for interested users. These can be downloaded through the webpage or by contacting ABB through the web request or helpline.

Technical Specifications (continued)

Digital Compensator

The MLX120 module uses digital control to regulate the output voltage. As with all POL modules, external capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes.

The MLX120 comes with default compensation values programmed into the non-volatile memory of the module. These digital compensation values can be adjusted externally to optimize transient response and ensure stability for a wide range of external capacitance and with different types of output capacitance.

Table 1

Output Capacitors	KPole1	KPole2	Kp	Ki	Kd
15x22uF + 24x47uF + 4x470uF	5	7	42	22	58
15x22uF + 65x47uF + 4x470uF	5	7	42	22	58
15x22uF + 73x47uF + 6x470uF	5	7	42	22	58

Power Module Wizard

Designers can access a free, web-based, easy to use tool that helps users simulate and tune the MLX120A0XY3-SRZ feedback loop parameters. Go to http://abb.transim.com and sign up for a free account to use the module selector tool. The tool also offers online Simplis/Simetrix models that can be used to assess transient performance, module stability, etc.

Digital Power Insight (DPI)

DPI is a software tool that helps users evaluate and simulate the PMBus performance of the MLX120A0XY3A modules without the need to write software. The software can be downloaded for free from our webpage. A USB to I^2C adapter and associated cable set are required for proper functioning of the software suite. For first time users, we recommend using the DPI Evaluation Kit, which can be purchased from any of the leading distributors. Please ensure that the USB to I^2C adapter being used/purchased is Version 2.2 or higher. Part Numbers are available in the last few pages of this datasheet

PMBus use guidelines

An I^2C or PMBus interface is used to communicate with the module. These two-wire serial interfaces consist of clock and data signals and operate as fast as 1 MHz with proper signal integrity. 400kHz is the typical operating frequency. The bus provides read and write access to the internal registers for configuration and monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters. To ensure operation with multiple devices on the bus, an exclusive address for the module is programmed into MTP. To protect customer configuration and information, the I^2C interface can be configured for either limited access or locked with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers. The module supports the Packet Error Checking (PEC) protocol and a number of PMBus commands to monitor voltages and currents.

PMBus data format

Linear-11

The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X). The formula to calculate the real world decimal value is: $X = Y \cdot 2^N$.

Linear-16

The L16u data format uses a fixed exponent (hard-coded to N = -xxh) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The formula to calculate the real world decimal value is: $X = Y \cdot 2^{-xx}$.

Linear-16 Signed

The L16s data format uses a fixed exponent (hard-coded to N = -xxh) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X). The formula to calculate the real world decimal value is: $X = Y \cdot 2^{-xx}$.

Bit Field

A description of the Bit Field format is provided in each command details.

Custom

A description of the Custom data format is provided in each command details. A combination of Bit Field and integer are common type of Custom data format.

ASCII (ASC)

A variable length string of text characters in the ASCII data format.

PMBus Addressing

The power module is addressed through the PMBus using a device address. The default module address is 0x40. The module supports 15 possible offset addresses (0x40 to 0x55). If multiple modules are used on the same bus, user must power up each module individually, change the module address, and then move on to the next module to repeat the process. If this is not possible, a pre-defined resistor can be connected to the PROG pin to provide an offset to the default address yielding a different address for each module on the same bus as described later in this document.

Technical Specifications (continued)

PMBus Addressing

The module simultaneously supports I^2C and PMBus through the use of exclusive addressing. By using a 7-bit address, the user can configure the device to any one of 127 different I^2C/PMBus addresses. Once the address of is set, it can be locked to protect it from being overridden. Optionally, a resistor can be tied to the PROG pin to generate an offset as shown in Table below (note that a 0.01 µF capacitor is required across the resistor). The base I2C address is 0x10 and Base PMBus address Is 0x40. For default programmed devices, the I2C/PMBus address can be temporarily forced to 0x0A for I^2C and 0x0D for PMBus by driving the PROG pin high (3.3 V).

The module supports 15 possible offset addresses (0x40 to 0x55) through resistor connection to the PROG pin. If multiple modules are used on the same bus without different PROG pin resistors, user must power up each module individually, change the module address and then move on to the next module and repeat the process. (See Quick Start Process in this datasheet). 0xD0 sub-commands are used to set and lock PMBus address and offset.

Example for 3 MLX modules on the same PMBus channel. Select a 0.845K ohm resistor on program pin of module 1 , 1.3kohm resistor on module 2 and a 1.78kohm resistor on module 3.

This results in:
Module 1 : I2C address is 10h+0h=10h, PMBus address is 40h+0h=40h
Module 2 : I2C address is 10h+1h=11h, PMBus address is 40h+1h=41h
Module 3 : I2C address is 10h+2h=12h, PMBus address is 40h+2h=42h

PROG RESISTOR	I2C Address Offset
0.845kΩ	+0
1.3kΩ	+1
1.78kΩ	+2
2.32kΩ	+3
2.87kΩ	+4
3.48kΩ	+5
4.12kΩ	+6
4.75kΩ	+7
5.49kΩ	+8
6.19kΩ	+9
6.98kΩ	+10
7.87kΩ	+11
8.87kΩ	+12
10.00kΩ	+13
11.00kΩ	+14
12.10kΩ	+15

Technical Specifications (continued)

Summary of Supported PMBus Commands

This section provides a summary of the MLX120A0XY3 commands followed by their detailed description. The commands are outlined in the order of increasing command codes. Since there are 2 Loops, the commands are presented for each Loop for completeness.

Table 2 - LOOP 1 / OUTPUT 1 Commands

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	DEFAULT VALUE	MIN/MAX VALUES or RANGE
PAGE	0x00	1	bit field		R/W	00	01 / FF
OPERATION	0x01	1	bit field		R/W	80	00/40/80/94/98/A4/A8
ON_OFF_CONFIG	0x02	1	bit field		R/W	1C	02/14/15/16/17/18/1C/1D/1E /1F
CLEAR_FAULTS	0x03	0			W		
WRITE_PROTECT	0x10	1	Bit field		W	0x00	
RESTORE_DEFAULT_ALL	0x12	0			W		
STORE_USER_ALL	0x15	0			W	CAN USE ONLY 24 TIMES	
RESTORE_USER_ALL	0x16	0			W		
CAPABILITY	0x19	1	bit field		R	0xB0	
SMBALERT_MASK	0x1B	2	Bit field		R/W	000100000100	
VOUT_MODE	0x20	1	mode + exp		R/W	0x18 (-8 Expo-nent)	-8, -9 , -12
VOUT_COMMAND	0x21	2	16-bit linear	V	R/W	0073 (0.449V)	0.45 –2.0
VOUT_TRIM	0x22	2	16-bit linear	V	R/W*	0.000V	-2 to 2
VOUT_MAX	0x24	2	16-bit linear	V	R/W	021A (2.102V)	0.45 to 2.102
VOUT_MARGIN_HIGH	0x25	2	16-bit linear	V	R/W+	0000	0 to 2.102
VOUT_MARGIN_LOW	0x26	2	16-bit linear	V	R/W+	0000	0 to 2.102
VOUT_TRANSITION_RATE	0x27	2	11-bit linear	V/ms	R/W	0xE808 (1mV/µs)	0 to 127.875mV/usec
VOUT_DROOP	0x28	2	11-bit linear	V	R/W	0000	0 to 9.98mΩ
VOUT_MIN	0x2B	2	11-bit linear	V	R/W	0040 (0.25V)	0 to 2.102
FREQUENCY_SWITCH	0x33	2	11-bit linear	kHz	R/W	0244 (580kHz)	
POWER_MODE	0x34	2	bit field		R/W	0x0003 (Max Power)	0, 3, 4, 5
VIN_ON	0x35	2	11-bit linear	V	R/W	F019 (6.25)	6.25—14
VIN_OFF	0x36	2	11-bit linear	V	R/W	F017 (5.75)	5.75—14
IOUT_CAL_GAIN	0x38	2	11-bit linear	mΩ	R/W	Vary	
IOUT_CAL_OFFSET	0x39	2	11-bit linear	A	R/W	Vary	
VOUT_OV_FAULT_LIMIT	0x40	2	16-bit linear	V	R/W	010D (1.051V)	0.45—2.102
VOUT_OV_FAULT_RESPONSE	0x41	1	bit field		R/W	80 (Shutdown)	Ignore (00), Sdown(80)
VOUT_OV_WARN_LIMIT	0x42	2	16-bit linear	V	R/W	0200 (2.000)	0.45—2.102
VOUT_UV_WARN_LIMIT	0x43	2	16-bit linear	V	R/W	0073 (0.449)	0.45—2.102
VOUT_UV_FAULT_LIMIT	0x44	2	16-bit linear	V	R	009A (0.602)	50mV to 400mV from Vout
VOUT_UV_FAULT_RESPONSE	0x45	1	bit field		R/W	80 (shutdown)	Ignore (00), Sdown(80)
IOUT_OC_FAULT_LIMIT	0x46	2	11-bit linear	A	R/W	0848 (144)	0 to 510
IOUT_OC_FAULT_RESPONSE	0x47	1	Bit field		r/W	F8 (Hiccup forever)	Sdown(C0), hiccup 6 then Sdown (F0),(F8)
IOUT_OC_WARN_LIMIT	0x4A	2	11-bit linear	A	R/W	104	0 to 510
OT_FAULT_LIMIT	0x4F	2	11-bit linear	°C	R/W	007D (125)	0 to 255
OT_FAULT_RESPONSE	0x50	1	bit field		R/W	C0 (Autorestart)	Ignore (00), Sdown(80), (C0)
OT_WARN_LIMIT	0x51	2	11-bit linear	°C	R/W	006E (110)	64 to 255
VIN_OV_FAULT_LIMIT	0x55	2	11-bit linear	V	R/W	E0E9 (14.563)	0 to 63.9375
VIN_OV_FAULT_RESPONSE	0x56	1	bit field		R/W	80 (Shutdown)	Ignore (00), Sdown(80)
VIN_UV_WARN_LIMIT	0x58	2	11-bit linear	V	R/W	E068 (6.5)	0 to 63.9375
IIN_OC_WARN_LIMIT	0x5D	2	11-bit linear	V	R/W	F83E (31)	0 to 127.5
POWER_GOOD_ON	0x5E	2	11-bit linear	V	R/W	0065 (0.395)	0.395 to 2.102
POWER_GOOD_OFF	0x5F	2	11-bit linear	V	R/W	0065 (0.395)	0.395 to 2.102

* Cannot be stored in NVM. Module will accept Write command but will not transfer to NVM when STORE_USER_ALL is used

+ Cannot be stored in NVM. Module will hold any written value till power cycle. Cannot use RESTORE_USER_ALL to revert to default value

Technical Specifications (continued)

Table 2 - LOOP 1 / OUTPUT 1 Commands (continued)

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	DEFAULT VALUE	MIN/MAX VALUES or RANGE
TON_DELAY	0x60	2	11-bit linear	ms	R/W	F800 (0)	0 to 63.5
TON_RISE	0x61	2	11-bit linear	ms	R/W	F03C (15)	0 to 31.75
TON_MAX_FAULT_LIMIT	0x62	2	11-bit linear	ms	R/W	F000 (0)	0 to 31.75
TON_MAX_FAULT_RESPONSE	0x63	1	11-bit linear	ms	R/W	00 (Ignore)	Ignore (00), Sdown
TOFF_DELAY	0x64	2	11-bit linear	ms	R/W	0ms	0 to 63.5
TOFF_FALL	0x65	2	11-bit linear	ms	R/W	F03C (15)	0 to 31.75
POUT_OP_WARN_LIMIT	0x6A	2	16-bit linear	Watts	R/W	01FF (511)	
POUT_OP_WARN_LIMIT	0x6B	2	16-bit linear	Watts	R/W	01FF (511)	
STATUS_BYTE	0x78	1	bit field		R	Varies (03)	
STATUS_WORD	0x79	2	bit field		R	Varies (A003)	
STATUS_VOUT	0x7A	1	bit field		R	Varies (20)	
STATUS_IOUT	0x7B	1	bit field		R	Varies (00)	
STATUS_INPUT	0x7C	1	bit field		R	Varies (20)	
STATUS_TEMPERATURE	0x7D	1	bit field		R	Varies (00)	
STATUS_CML	0x7E	1	bit field		R	Varies (02)	
STATUS_MFR_SPECIFIC	0x80	1	bit field		R	Varies (00)	
READ_VIN	0x88	2	11-bit linear	V	R	Varies	
READ_IIN	0x89	2	11-bit linear	A	R	Varies, 63.9A max register limit	
READ_VOUT	0x8B	2	11-bit linear	V	R	Varies	
READ_IOUT	0x8C	2	11-bit linear	A	R	Varies	
READ_TEMPERATURE_1	0x8D	2	11-bit linear	°C	R	Varies	
READ_DUTY_CYCLE	0x94	2	11-bit linear	%	R	Varies	
READ_POUT	0x96	2	11-bit linear	W	R	Varies	
READ_PIN	0x97	2	11-bit linear	W	R	Varies	
PMBUS_REVISION	0x98	1	bit field		R	33	
MFR_ID	0x99	2	bit field		R	4952	
MFR_MODEL	0x9A	2	bit field		R	0078	
MFR_REVISION	0x9B	2	bit field		R	Varies (0012)	
MFR_DATE	0x9D	2	bit field		R	Varies	
IC_DEVICE_ID	0xAD	1	bit field		R	6C	
IC_DEVICE_REV	0xAE	1	bit field		R	01	
MFR_READ_VAUX	0xC4	32	bit field	V	R/W	Varies	
MFR_VIN_PEAK	0xC5	32	bit field	V	R/W	Varies	
MFR_VOUT_PEAK	0xC6	32	bit field	V	R/W	Varies	
MFR_IOUT_PEAK	0xC7	2	bit field	A	R/W	Varies	
MFR_TEMP_PEAK	0xC8	2	bit field	C	R/W	Varies	
MFR_VIN_VALLEY	0xC9	2	bit field	V	R/W	Varies	
MFR_VOUT_VALLEY	0xCA	2	bit field	V	R/W	Varies	
MFR_IOUT_VALLEY	0xCB	2	bit field	A	R/W	Varies	
MFR_TEMP_VALLEY	0xCC	2	bit field	C	R/W	Varies	
MFR_REG_ADDRESS	0xD0	7	bit field		R-2/W-5*	Varies	
MFR_I²C_ADDRESS	0xD6	7	bit field		R/W	10 (10)	

*R-2/W-5 refers to the number of data bytes in the command, 5 data bytes for a Write and 2 data bytes for a Read

Technical Specifications (continued)

Table 3 - LOOP 2 / OUTPUT 2 – USE ONLY WHEN SATELLITE IS USED

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	DEFAULT VALUE	MIN/MAX VALUES or RANGE
PAGE	0x01	1	bit field		R/W	01	01/FF
OPERATION	0x01	1	bit field		R/W	80	00/40/80/94/98/A4/A8
ON_OFF_CONFIG	0x02	1	bit field		R/W	1C	02/14/15/16/17/18/1C/1D/1E /1F
CLEAR_FAULTS	0x03	0			W		
WRITE_PROTECT	0x10	1	Bit field		W	0x00	
RESTORE_DEFAULT_ALL	0x12	0			W		
STORE_USER_ALL	0x15	0			W		
RESTORE_USER_ALL	0x16	0			W		
CAPABILITY	0x19	1	bit field		R	0xB4	
SMBALERT_MASK	0x1B	2	Bit field		R/W	000100000100	
VOUT_MODE	0x20	1	mode + exp		R/W	0x18 (-8 Exponent)	-8,-9,-12
VOUT_COMMAND	0x21	2	16-bit linear	V	R/W	0073 (0.449V)	0.45 –2.0
VOUT_TRIM	0x22	2	16-bit linear	V	R/W*	0.000V	-2 to 2
VOUT_MAX	0x24	2	16-bit linear	V	R/W	021A (2.102V)	0.45 to 2.102
VOUT_MARGIN_HIGH	0x25	2	16-bit linear	V	R/W+	0000	0 to 2.102
VOUT_MARGIN_LOW	0x26	2	16-bit linear	V	R/W+	0000	0 to 2.102
VOUT_TRANSITION_RATE	0x27	2	11-bit linear	V/ms	R/W	0xE808 (1mV/µs)	0 to 127.875mV/usec
VOUT_DROOP	0x28	2	11-bit linear	V	R/W	0000	0 to 9.98mΩ
VOUT_MIN	0x2B	2	11-bit linear	V	R/W	0040 (0.25V)	0 to 2.102
FREQUENCY_SWITCH	0x33	2	11-bit linear	kHz	R/W	0244 (580kHz)	
POWER_MODE	0x34	2	bit field		R/W	0x0003 (Max Pow-er)	0, 3, 4, 5
VIN_ON	0x35	2	11-bit linear	V	R/W	F019 (6.25)	6.25—14
VIN_OFF	0x36	2	11-bit linear	V	R/W	F017 (5.75)	5.75—14
IOUT_CAL_GAIN	0x38	2	11-bit linear	mΩ	R/W	Vary	
IOUT_CAL_OFFSET	0x39	2	11-bit linear	A	R/W	Vary	
VOUT_OV_FAULT_LIMIT	0x40	2	16-bit linear	V	R/W	010D (1.051V)	0.45—2.102
VOUT_OV_FAULT_RESPONSE	0x41	1	bit field		R/W	80 (Shutdown)	Ignore (00), Sdown(80)
VOUT_OV_WARN_LIMIT	0x42	2	16-bit linear	V	R/W	0200 (2.000)	0.45—2.102
VOUT_UV_WARN_LIMIT	0x43	2	16-bit linear	V	R/W	0073 (0.449)	0.45—2.102
VOUT_UV_FAULT_LIMIT	0x44	2	16-bit linear	V	R	009A (0.602)	50mV to 400mV from Vout
VOUT_UV_FAULT_RESPONSE	0x45	1	bit field		R/W	80 (shutdown)	Ignore (00), Sdown(80)
IOUT_OC_FAULT_LIMIT	0x46	2	11-bit linear	A	R/W	081A (52)	0 to 510
IOUT_OC_FAULT_RESPONSE	0x47	1	Bit field		r/W	F8 (Hiccup forever)	Sdown(C0), hiccup 6 then Sdown (F0),(F8)
IOUT_OC_WARN_LIMIT	0x4A	2	11-bit linear	A	R/W	0812 (36)	0 to 510
OT_FAULT_LIMIT	0x4F	2	11-bit linear	°C	R/W	007D (125)	0 to 255
OT_FAULT_RESPONSE	0x50	1	bit field		R/W	C0 (Autorestart)	Ignore (00), Sdown(80), (C0)
OT_WARN_LIMIT	0x51	2	11-bit linear	°C	R/W	006E (110)	64 to 255
VIN_OV_FAULT_LIMIT	0x55	2	11-bit linear	V	R/W	E0E9 (14.563)	0 to 63.9375
VIN_OV_FAULT_RESPONSE	0x56	1	bit field		R/W	80 (Shutdown)	Ignore (00), Sdown(80)
VIN_UV_WARN_LIMIT	0x58	2	11-bit linear	V	R/W	E068 (6.5)	0 to 63.9375
IIN_OC_WARN_LIMIT	0x5D	2	11-bit linear	V	R/W	F814 (10)	0 to 127.5
POWER_GOOD_ON	0x5E	2	11-bit linear	V	R/W	0065 (0.395)	0.395 to 2.102
POWER_GOOD_OFF	0x5F	2	11-bit linear	V	R/W	0065 (0.395)	0.395 to 2.102
TON_DELAY	0x60	2	11-bit linear	ms	R/W	F800 (0)	O to 63.5
TON_RISE	0x61	2	11-bit linear	ms	R/W	F03C (15)	0 to 31.75
TON_MAX_FAULT_LIMIT	0x62	2	11-bit linear	ms	R/W	F000 (0)	0 to 31.75
TON_MAX_FAULT_RESPONSE	0x62	1	11-bit linear	ms	R/W	00 (Ignore)	Ignore (00), Sdown(80)
TOFF_DELAY	0x64	2	11-bit linear	ms	R/W	0ms	0 to 63.5
TOFF_FALL	0x65	2	11-bit linear	ms	R/W	F03C (15)	0 to 31.75

* Cannot be stored in NVM. Module will accept Write command but will not transfer to NVM when STORE_USER_ALL is used

+ Cannot be stored in NVM. Module will hold any written value till power cycle. Cannot use RESTORE_USER_ALL to revert to default value

Technical Specifications (continued)

Table 3 - LOOP 2 / OUTPUT 2 – USE ONLY WHEN SATELLITE IS USED (continued)

PMBUS CMD	CMD CODE	DATA BYTES	DATA FORMAT	DATA UNITS	TRANSFER TYPE	DEFAULT VALUE	MIN/MAX VALUES or RANGE
POUT_OP_WARN_LIMIT	0x6A	2	16-bit linear	Watts	R/W	01FF (511)	
POUT_OP_WARN_LIMIT	0x6B	2	16-bit linear	Watts	R/W	01FF (511)	
STATUS_BYTE	0x78	1	bit field		R	Varies (03)	
STATUS_WORD	0x79	2	bit field		R	Varies (A003)	
STATUS_VOUT	0x7A	1	bit field		R	Varies (20)	
STATUS_IOUT	0x7B	1	bit field		R	Varies (00)	
STATUS_INPUT	0x7C	1	bit field		R	Varies (20)	
STATUS_TEMPERATURE	0x7D	1	bit field		R	Varies (00)	
STATUS_CML	0x7E	1	bit field		R	Varies (02)	
STATUS_MFR_SPECIFIC	0x80	1	bit field		R	Varies (00)	
READ_VIN	0x88	2	11-bit linear	V	R	Varies	
READ_IIN	0x89	2	11-bit linear	A	R	Varies, 63.9A max register limit	
READ_VOUT	0x8B	2	11-bit linear	V	R	Varies	
READ_IOUT	0x8C	2	11-bit linear	A	R	Varies	
READ_TEMPERATURE_1	0x8D	2	11-bit linear	°C	R	Varies	
READ_DUTY_CYCLE	0x94	2	11-bit linear	%	R	Varies	
READ_POUT	0x96	2	11-bit linear	W	R	Varies	
READ_PIN	0x97	2	11-bit linear	W	R	Varies	
PMBUS_REVISION	0x98	1	bit field		R	33	
MFR_ID	0x99	2	bit field		R/W	4952	
MFR_MODEL	0x9A	2	bit field		R/W	0078	
MFR_REVISION	0x9B	2	bit field		R/W	Varies (0012)	
MFR_DATE	0x9D	2	bit field		R/W	Varies	
IC_DEVICE_ID	0xAD	1	bit field		R	6C	
IC_DEVICE_REV	0xAE	1	bit field		R	01	
MFR_READ_VAUX	0xC4	32	bit field	V	R/W	Varies	
MFR_VIN_PEAK	0xC5	32	bit field	V	R/W	Varies	
MFR_VOUT_PEAK	0xC6	32	bit field	V	R/W	Varies	
MFR_IOUT_PEAK	0xC7	2	bit field	A	R/W	Varies	
MFR_TEMP_PEAK	0xC8	2	bit field	C	R/W	Varies	
MFR_VIN_VALLEY	0xC9	2	bit field	V	R/W	Varies	
MFR_VOUT_VALLEY	0xCA	2	bit field	V	R/W	Varies	
MFR_IOUT_VALLEY	0xCB	2	bit field	A	R/W	Varies	
MFR_TEMP_VALLEY	0xCC	2	bit field	C	R/W	Varies	
MFR_REG_ACCESS	0xD0	7	bit field		R-2/W-5	Varies	
MFR_I^{2}C_ADDRESS	0xD6	7	bit field		R/W	10 (10)	

Technical Specifications (continued)

Quick Start process—Single MLX120 on PMBus

1. Power up module
2. Configure required output voltage through PAGE 0x00 and VOUT_COMMAND 0x21

3. Configure the following if needed

- VOUT_OV_FAULT_RESPONSE 0x41
- VOUT_OV_FAULT_LIMIT 0x40
- VOUT_OV_WARN_LIMIT 0x42

4. If Changes are final and Configuration has to be stored in NVM use

- STORE_USER_ALL 0x15

If Module has to be turned on using ON/OFF command use ON_OFF_CONFIG 0x02 to change setting

Quick Start process—Multiple MLX modules on same PMBus, same fixed offset resistor—0.845kΩ

Command Name and explanation in parenthesis	Address Offset	Application: Common, Loop1 or Loop2	Description, Range	Default Value
I^{2}C_device_addr (Sets the I2C device address. If set to 0, the I2C interface is effectively disabled. In test mode, the chip also accepts a default value of 0x14. Locked by register i2c_pmb_addr_lock)	D0 0020 [14:8]	COMMON	Sets the I^{2}C device address. If set to 0, the I^{2}C interface is effectively disabled. In test mode, the chip also accepts a default value of 0x14. Locked by register I^{2}C_pmb_addr_lock. Reserved I^{2}C addresses:(0x00 to 0x07), 0x08, 0x0c, 0x28, 0x37, 0x61, (0x78 to 0x7F).	10 (16)
pmb_device_addr (Sets the PMBus device address. If set to 0, the PMBus interface is effectivelydisabled)	D0 0020 [6:0]	COMMON	Set this bit to lock I^{2}C and PMBus address registers 0-->Unlock I^{2}C and PMBus address 1-->Lock I^{2}Cand PMBus address	40 (64)
I^{2}C/PMBUS Adress lock (Set this bit to lock I2C and PMBus address registers)	D0 0094 [2:2]	COMMON	Set this bit to lock I^{2}C and PMBus address registers 0-->Unlock I^{2}C and PMBus address 1-->Lock I^{2}C and PMBus address	01 (1)

Above screenshot is from PMBus Applications Note for this family. It is available on Webpage

Example for 3 modules on same PMBus Channel

1. Power up module 1.

2. Configure address using advanced D0 command also explained in MLX/SLX PMBus application note. Set register 0x0020[14:18]=12h and register 0x0020[6:0]=42h, to assign module 1 with I2C address=12h and PMBus address =42h.

3. Configure required output voltage through PAGE 0x00 and VOUT_COMMAND 0x21.

4. Configure the following if needed.

- VOUT_OV_FAULT_RESPONSE 0x41
- VOUT_OV_FAULT_LIMIT 0x40
- VOUT_OV_WARN_LIMIT 0x42

5. If Module default ON/OFF operation has to be changed, use ON_OFF_CONFIG 0x02 to change setting

6. If Changes are final and Configuration has to be stored in NVM use, STORE_USER_ALL 0x15.

7. Power up module 2.

Module 2—set register 0x0020[14:18]=11h and register 0x0020[6:0]=41h, to assign module 2 with I2C address=11h and PMBus address =41h.

8. Configure required output voltage through PAGE 0x00 and VOUT_COMMAND 0x21.

9. Configure the following if needed

- VOUT_OV_FAULT_RESPONSE 0x41 .
- VOUT_OV_FAULT_LIMIT 0x40.
- VOUT_OV_WARN_LIMIT 0x42.

10.If Module default ON/OFF operation has to be changed, use ON_OFF_CONFIG 0x02 to change setting.

11. If Changes are final and Configuration has to be stored in NVM, use STORE_USER_ALL 0x15

12. Power up module 3.

Keep default I2C address=10h and PMBus address =40h.

13. Configure required output voltage through PAGE 0x00 and VOUT_COMMAND 0x21.

14. Configure the following if needed

- VOUT_OV_FAULT_RESPONSE 0x41 ,
- VOUT_OV_FAULT_LIMIT 0x40,
- VOUT_OV_WARN_LIMIT 0x42

15. If Changes are final and Configuration has to be stored in NVM, use STORE_USER_ALL 0x15

Technical Specifications (continued)

Layout considerations

The evaluation board layout and schematic files are available for interested users. These can be downloaded through the webpage or by contacting our Field Applications Engineer through the help section of the webpage. The electrical and the thermal characterization of the MLX120A0XY3-SRZ module has been done on evaluation boards with layout as shown in Fig28.

The entire MLX series has a central controller section and symmetrical power switching sections on each side of the controller depending on the power rating. Layout guidelines are provided based on the full rated MLX160. For MLX120 modules only the controller and power sections (three) present on the modules should be considered. Even the pin numbering is based on the MLX160 which is controller section + 4 power phases. For the power section that is not present in the MLX120 those pin numbers have been omitted instead of renumbering the pins. Hence there may be a jump in the pin numbering table towards the end of this document. Following are the recommendations for this converter.

1. For Thermal and Current Carrying reasons, it is recommended to have four 20 mil heavy plated filled vias on each of the power pins. Copper plating of vias should be 2 mils if possible.
2. 12 mil vias are recommended for all Signal Pins
3. Additional thermal vias can be placed on ground plane around module and signal pins

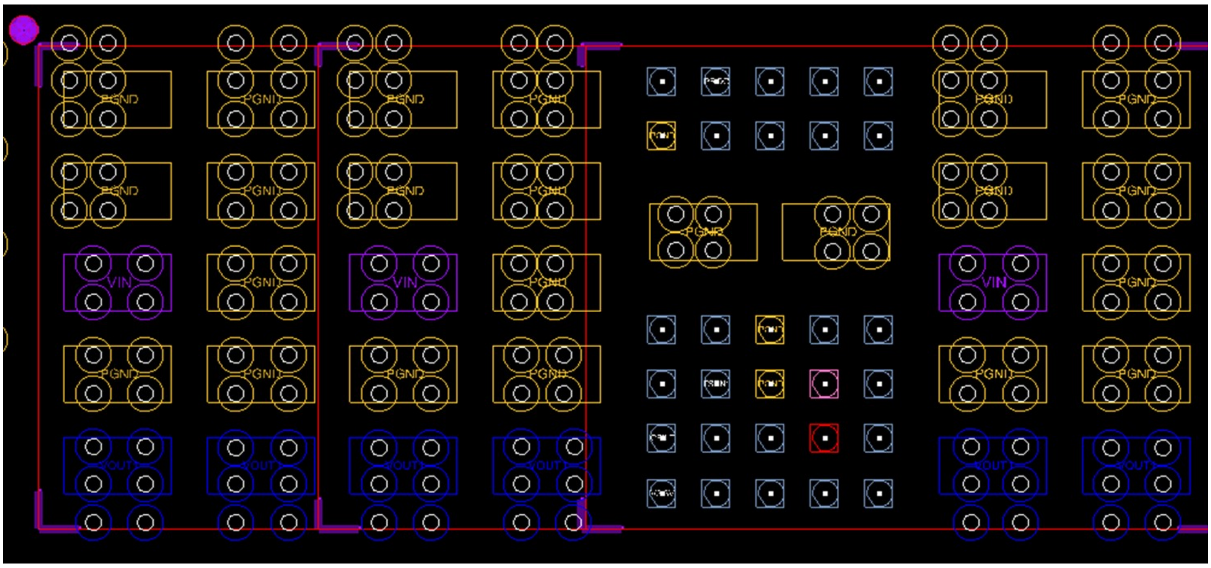


Figure 28. Example of Pad Layout with Vias

4. Input Voltage for each of the phases can be laid out on the same layer as shown below:

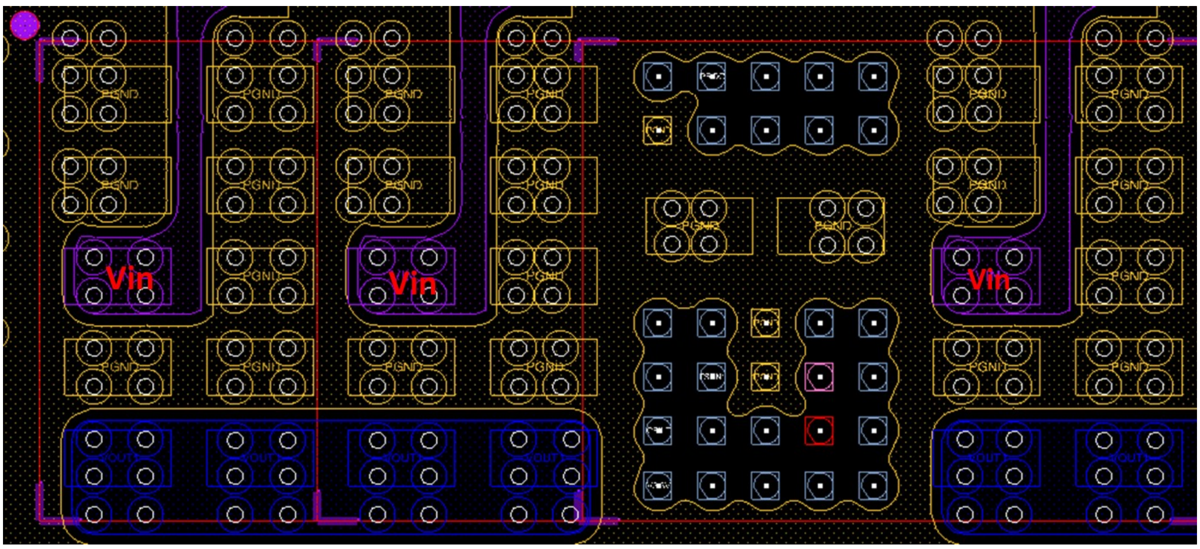


Figure 29. Example of Pad Layout with Vias

Technical Specifications (continued)

Layout considerations (continued)

5. It is possible to split the grounds at this location based on customer design layout practices; the POL module has a single ground

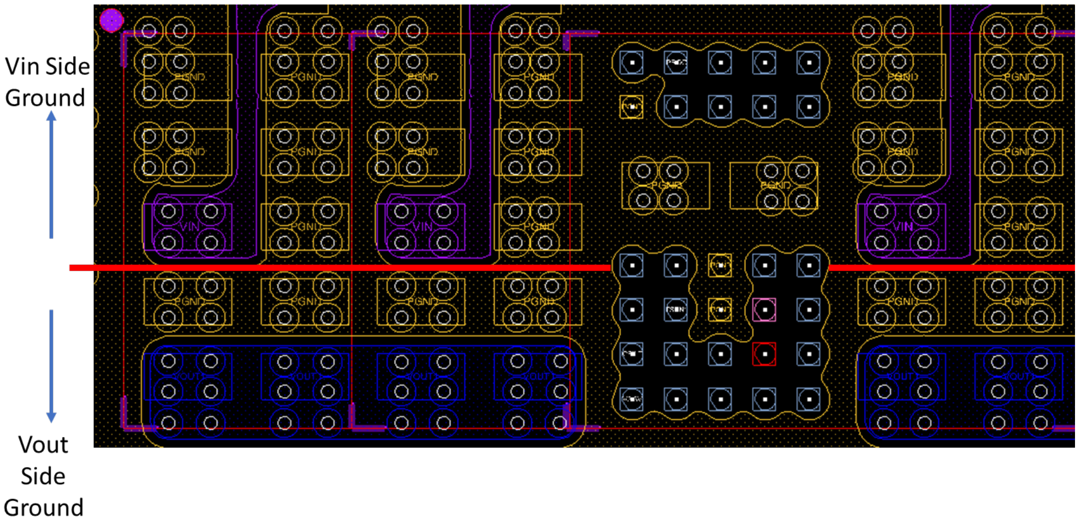


Figure 30. Example of split input-output ground

6. Place a minimum of 10uf and 1uf input capacitor on the bottom side of the customer board directly under Vin and keep additional input capacitance as close to Vinunder each of the phases. Additional input capacitance can be placed on top surface of board. All phases need to have same amount of input capacitance.

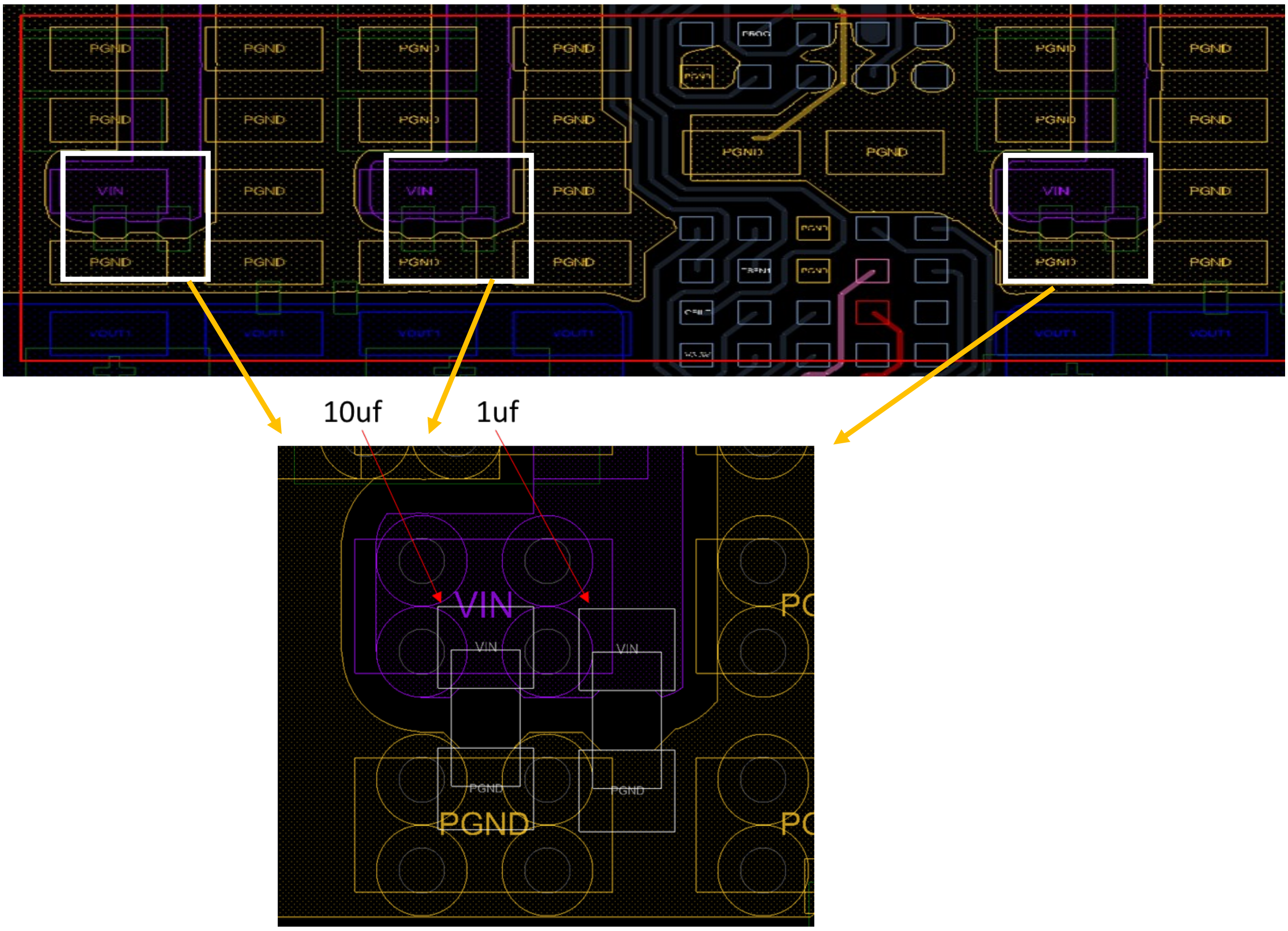


Figure 31. Example of Input capacitor placement and routing

Technical Specifications (continued)

Layout considerations (continued)

7. Input capacitance for each of the phases is recommended to be as close as possible to the Vin of the module.

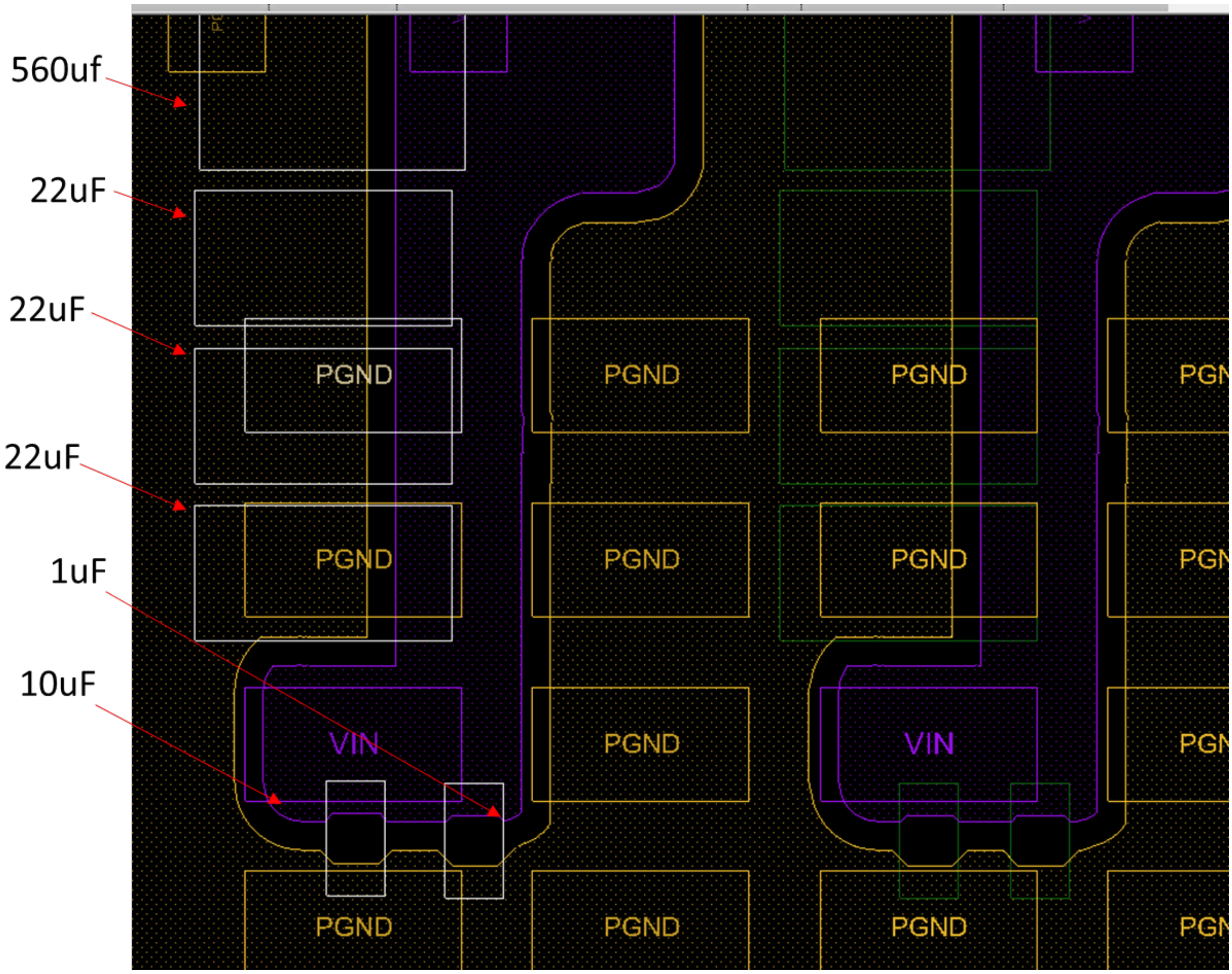


Figure 32. Input capacitor placing

Technical Specifications (continued)

Layout considerations (continued)

8. Sense traces must be routed differentially with a 5mil air gap spacing. Also provide ground plane under remote sensing pairs.

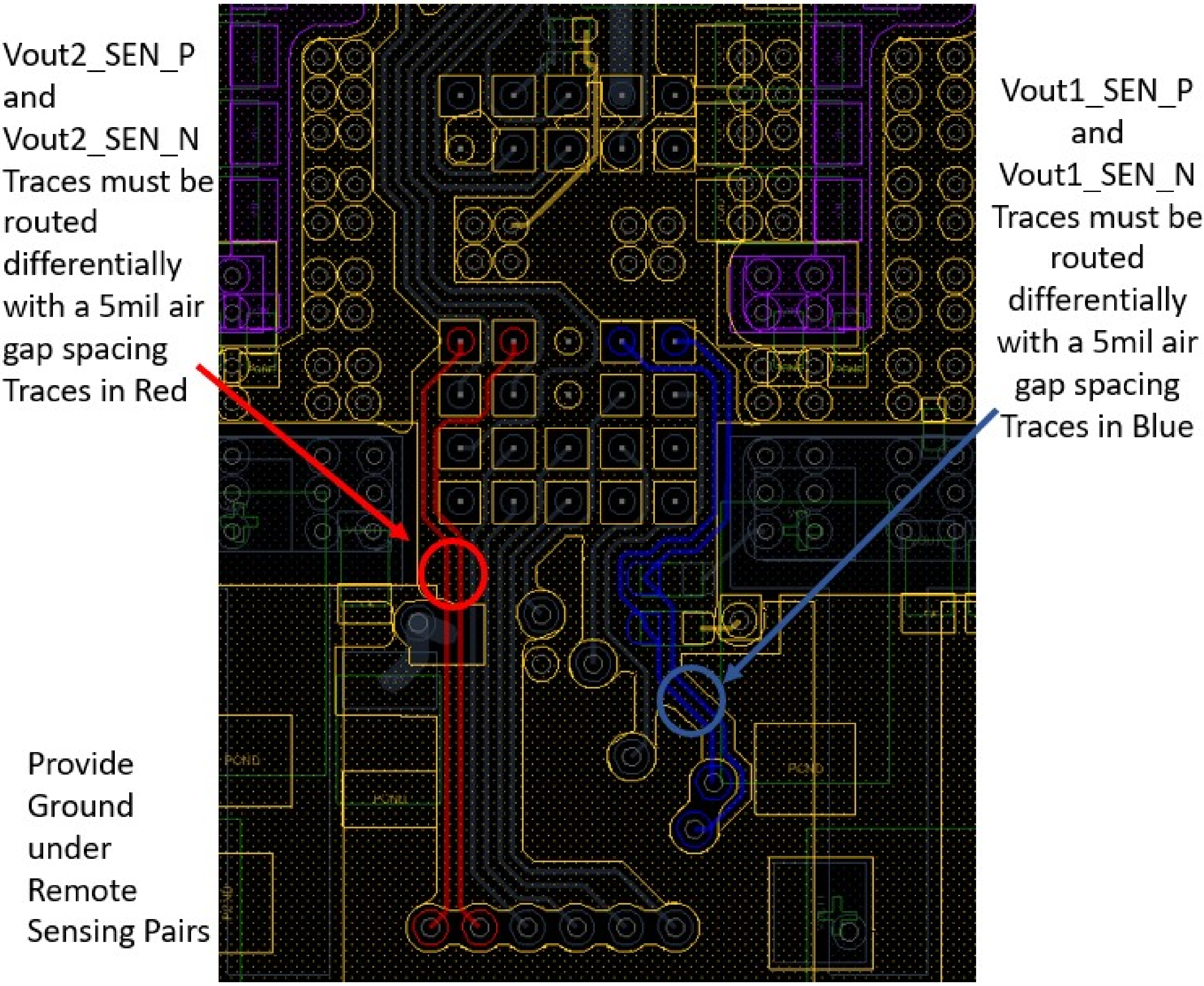
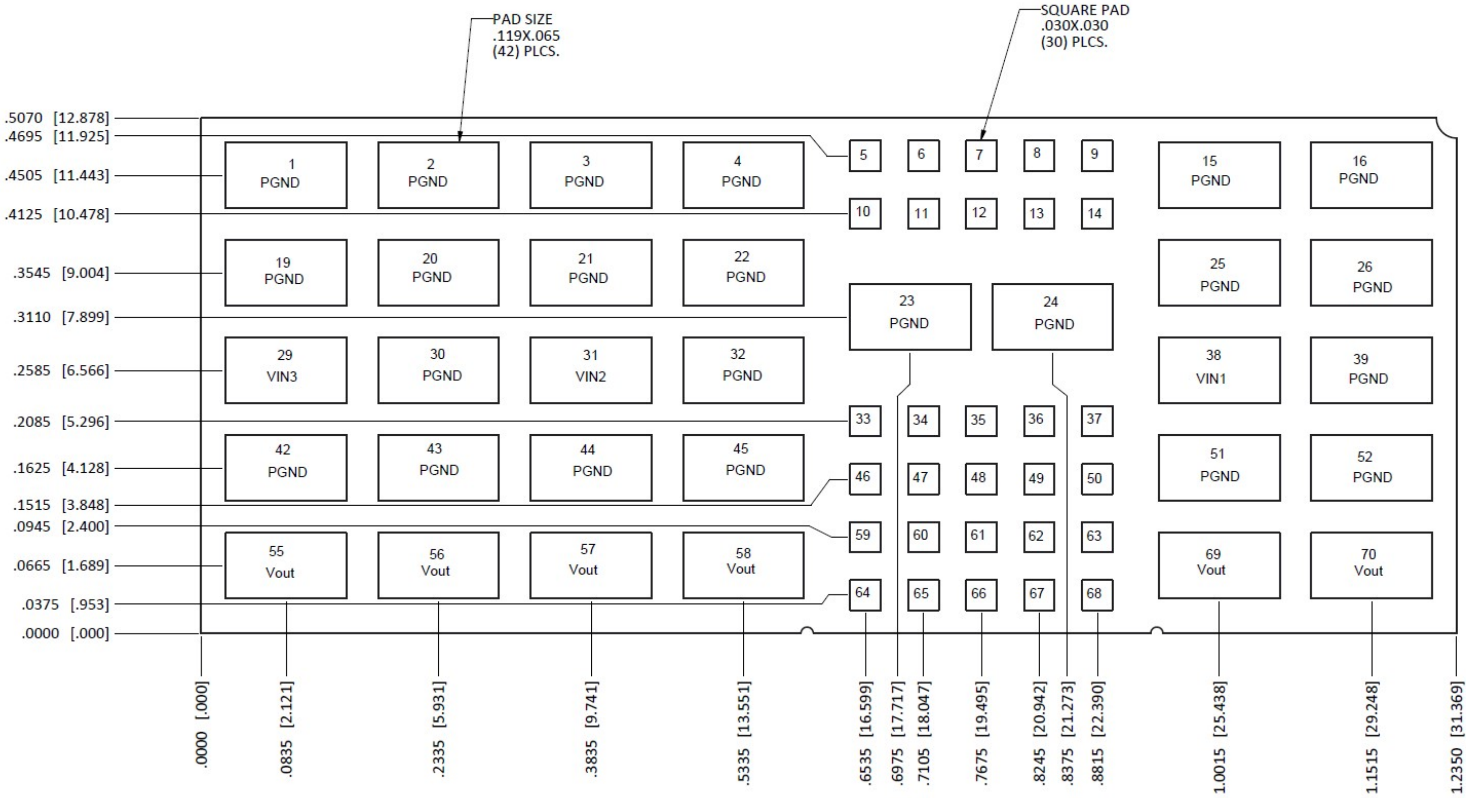


Figure 33. VSense Traces

Technical Specifications (continued)

Recommended Pad Layout and Pin Description



PIN	FUNCTION	PIN	FUNCTION
1	PGND	36	VOUT1_SEN_N
2	PGND	37	VOUT1_SEN_P
3	PGND	38	VIN1
4	PGND	39	PGND
5	WARN#/GP	42	PGND
6	PROG	43	PGND
7	IMON7_SAT_L1/IMON2_SAT_L2	44	PGND
8	V5V	45	PGND
9	VRRDY2	46	TSEN_SAT_L2
10	PGND	47	TSEN1
11	IMON8_SAT_L1/IMON1_SAT_L2	48	PGND
12	IMON6_SAT_L1/IMON3_SAT_L2	49	VR_EN1
13	IMON5_SAT_L1/IMON4_SAT_L2	50	VRHOT
14	VR_EN2	51	PGND
15	PGND	52	PGND
16	PGND	55	VOUT
19	PGND	56	VOUT
20	PGND	57	VOUT
21	PGND	58	VOUT
22	PGND	59	CFILT
23	PGND	60	PWM7_SAT_L1/PWM2_SAT_L2
24	PGND	61	PWM6_SAT_L1/PWM3_SAT_L2
25	PGND	62	SM_DAT
26	PGND	63	VRRDY1
29	VIN3	64	V3.3V
30	PGND	65	PWM8_SAT_L1/PWM1_SAT_L2
31	VIN2	66	PWM5_SAT_L1/PWM4_SAT_L2
32	PGND	67	SM_CLK
33	VOUT2_SAT_L2_SEN_P	68	SM_ALERT
34	VOUT2_SAT_L2_SEN_N	69	VOUT
35	PGND	70	VOUT

Technical Specifications (continued)

Pin Assignment Table

Pin	Label	Type	Description
1	PGND	PWR	Ground Reference for the module, Rail Return.
2	PGND	PWR	Ground Reference for the module, Rail Return.
3	PGND	PWR	Ground Reference for the module, Rail Return.
4	PGND	PWR	Ground Reference for the module, Rail Return.
5	WARN#/GP	Alarm	Open-drain active low alert pin to indicate Output Over-current Warning. Can use V3.3V from module to pullup using a resistor.
6	PROG	Analog	Configuration Pointer: A resistor to ground on this pin points to the specific configuration file to be loaded into the OTP during power up (along with a 0.01 µF cap in parallel with the resistor).
7	IMON7_SAT_L1/ IMON2_SAT_L2	I	Imon: (Analog output current monitor): This pin provides an analog output voltage proportional to the average output current. The full-scale IMON voltage is 2.55 V. 0A corresponds to 5 mV voltage at IMON.
8	V5V	O	Auxiliary 5V low power bus.
9	VRRDY2	Alarm	Voltage Regulator Ready Output (Loop #2). Open-drain output that asserts high when the VR has completed soft-start to Loop #2 boot voltage. Pull up to an external voltage through a resistor.
10	PGND	PWR	Ground Reference for the module, Rail Return.
11	IMON8_SAT_L1 /IMON1_SAT_L2	O	Imon: (Analog output current monitor): This pin provides an analog output voltage proportional to the average output current. The full-scale IMON voltage is 2.55 V. 0 A corresponds to 5 mV voltage at IMON.
12	IMON6_SAT_L1 / IMON3_SAT_L2	O	Imon: (Analog output current monitor): This pin provides an analog output voltage proportional to the average output current. The full-scale IMON voltage is 2.55 V. 0 A corresponds to 5 mV voltage at IMON.
13	IMON5_SAT_L1/ IMON4_SAT_L2	O	Imon: Analog output current monitor. This pin provides an analog output voltage proportional to the average output current. The full-scale IMON voltage is 2.55 V. 0 A corresponds to 5 mV voltage at IMON.
14	VR_EN2	Input	Enable Input for Loop #2. Cannot be left floating. Must be pulled high or low.
15	PGND	PWR	Ground Reference for the module, Rail Return.
16	PGND	PWR	Ground Reference for the module, Rail Return.
19	PGND	PWR	Ground Reference for the module, Rail Return.
20	PGND	PWR	Ground Reference for the module, Rail Return.
21	PGND	PWR	Ground Reference for the module, Rail Return.
22	PGND	PWR	Ground Reference for the module, Rail Return.
23	PGND	PWR	Ground Reference for the module, Rail Return.
24	PGND	PWR	Ground Reference for the module, Rail Return.
25	PGND	PWR	Ground Reference for the module, Rail Return.
26	PGND	PWR	Ground Reference for the module, Rail Return.
29	VIN3	Input	Input voltage rail. Recommended total input capacitance 4 x 560uF (electrolytic), 16 x 22 µF, 16x 10µF, 8x 1 µF.
30	PGND	PWR	Ground Reference for the module, Rail Return
31	VIN2	Input	Input voltage rail. Recommended total input capacitance 4 x 560uF (electrolytic), 16 x 22 µF, 16x 10µF, 8x 1 µF.
32	PGND	PWR	Ground Reference for the module, Rail Return.
33	VOUT2_SAT_L2 _SEN_P	Input	Differential remote sense input for Loop 2/Satellite. Connect to positive output regulation point for Loop2/Satellite output if used. Route differentially with VOUT2_SAT_L2_SEN_N.
34	VOUT2_SAT_L2 _SEN_N	Input	Differential remote sense input for Loop 2/Satellite. Connect to negative output regulation point for Loop2/Satellite if used. Route differentially with VOUT2_SAT_L2_SEN_N.
35	PGND	PWR	Ground Reference for the module, Rail Return.
36	VOUT1_SEN_N	Input	Differential remote sense input for Loop 1. Connect to negative output regulation point. Route differentially with VOUT1_SEN_P.
37	VOUT1_SEN_P	Input	Differential remote sense input for Loop 1. Connect to positive output regulation point. Route differentially with VOUT1_SEN_N.
38	VIN1	Input	Input voltage rail. Recommended total input capacitance 4 x 560uF (electrolytic), 16 x 22 µF, 16x 10µF, 8x 1 µF.

See Application Circuit and Layout Guidelines in this Datasheet for more information

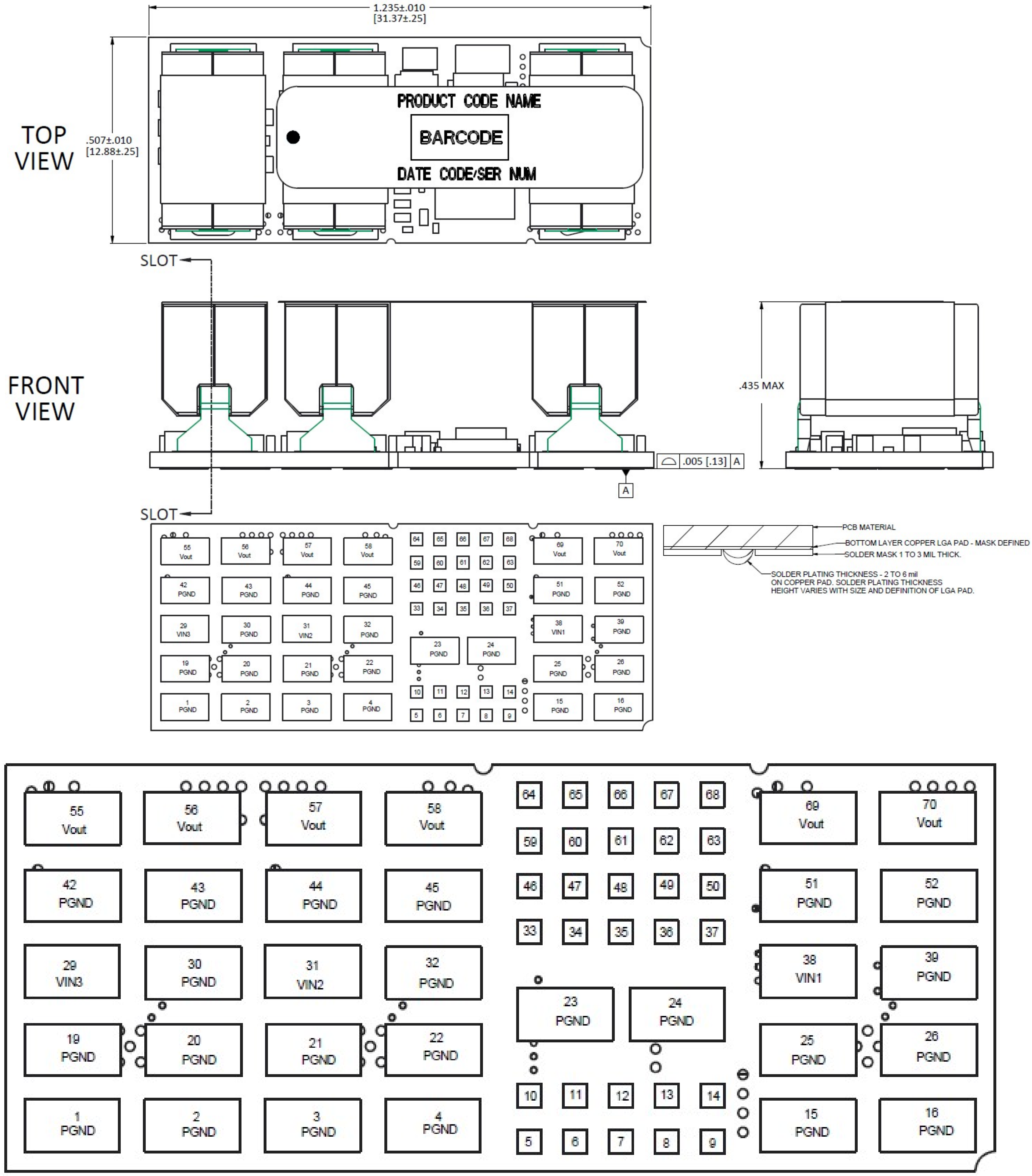
Technical Specifications (continued)

Pin	Label	Type	Description
39	PGND	PWR	Ground Reference for the module, Rail Return.
42	PGND	PWR	Ground Reference for the module, Rail Return.
43	PGND	PWR	Ground Reference for the module, Rail Return.
44	PGND	PWR	Ground Reference for the module, Rail Return.
45	PGND	PWR	Ground Reference for the module, Rail Return.
46	TSEN_SAT_L2	Input	External Temperature sense input(NTC network) for Satellite Unit / Loop 2. Ground if no satellite connected.
47	TSEN1	Input	External Temperature sense input (NTC network) for Satellite Unit on Loop 1. Leave floating if no satellites are connected. If Satellite present on Loop1 connect this pin to TSEN_SAT in satellite.
48	PGND	PWR	Ground Reference for the module, Rail Return.
49	VR_EN1	Input	VR Enable Input (Loop #1). VR ENABLE is used to power-on the regulator. Cannot be left floating. Must be pulled high or low. Can use 3.3V from module to pullup using a resistor.
50	VRHOT	Output	VRHOT# Output. Active low alert pin that can be programmed to assert if temperature exceeds threshold. Can use 3.3V from module to pullup using a resistor.
51	PGND	PWR	Ground Reference for the module, Rail Return.
52	PGND	PWR	Ground Reference for the module, Rail Return.
55	VOUT	Output	Output voltage rail. Connect to output filter capacitors. Recommended total output capacitance 6 x 470µF (polymer),73x 47 µF, 15x 22 µF, 4x 0.1µF, 4x 0.047µF, 1 x 0.022µF, 1 x 2200pF, 1 x 1500pF.
56	VOUT	Output	Output voltage rail. Connect to output filter capacitors. Recommended total output capacitance 6 x 470µF (polymer),73x 47 µF, 15x 22 µF, 4x 0.1µF, 4x 0.047µF, 1 x 0.022µF, 1 x 2200pF, 1 x 1500pF.
57	VOUT	Output	Output voltage rail. Connect to output filter capacitors. Recommended total output capacitance 6 x 470µF (polymer),73x 47 µF, 15x 22 µF, 4x 0.1µF, 4x 0.047µF, 1 x 0.022µF, 1 x 2200pF, 1 x 1500pF.
58	VOUT	Output	Output voltage rail. Connect to output filter capacitors. Recommended total output capacitance 6 x 470µF (polymer),73x 47 µF, 15x 22 µF, 4x 0.1µF, 4x 0.047µF, 1 x 0.022µF, 1 x 2200pF, 1 x 1500pF.
59	CFILT	Output	1.8 V Decoupling. A 1 µF capacitor on this pin provides decoupling for the internal 1.8 V supply.
60	PWM7_SAT_L1/ PWM2_SAT_L2	Output	Pulse Width Modulation Output for external Power stage in Satellite. Use as Loop 2 Phase 2 or Loop 1 Phase 7.
61	PWM6_SAT_L1/ PWM3_SAT_L2	Output	Pulse Width Modulation Output for external Power stage in Satellite. Use as Loop 2 Phase 3 or Loop 1 Phase 6.
62	SM_DAT	Output	Serial data. Connect to external host and/or to other devices. Requires a pull-up resistor to a V3.3V or 5V source. Can use V3.3V from module to pullup using a resistor.
63	VRRDY1	Output	Voltage Regulator Ready Output (Loop #1). Open-drain output that asserts high when the module has completed soft-start to Loop #1 setpoint voltage. Can use V3.3V from module to pullup using a resistor.
64	V3.3V	Output	Auxiliary V3.3V low power bus.
65	PWM8_SAT_L1/ PWM1_SAT_L2	Output	Pulse Width Modulation Output for external Power stage in Satellite. Use as Loop 2 Phase 1 or Loop 1 Phase 8.
66	PWM5_SAT_L1/ PWM4_SAT_L2	Output	Pulse Width Modulation Output for external Power stage in Satellite. Use as Loop 2 Phase 4 or Loop 1 Phase 5.
67	SM_CLK	I/O	Serial clock. Connect to external host and/or to other modules. Can use V3.3V from module to pullup using a resistor.
68	SM_ALERT	I/O	Serial alert. Connect to external host if desired. Can use V3.3V from module to pullup using a resistor. If not used, GND this pin
69	VOUT	Output	Output voltage rail. Connect to output filter capacitors. Recommended total output capacitance 6 x 470µF (polymer),73x 47 µF, 15x 22 µF, 4x 0.1µF, 4x 0.047µF, 1 x 0.022µF, 1 x 2200pF, 1 x 1500pF.
70	VOUT	Output	Output voltage rail. Connect to output filter capacitors. Recommended total output capacitance 6 x 470µF (polymer) || 73x 47 µF || 15x 22 µF || 4x 0.1µF|| 4x 0.047µF|| 1 x 0.022µF|| 1 x 2200pF|| 1 x 1500pF

See Application Circuit and Layout Guidelines in this Datasheet for more information

Technical Specifications (continued)

Physical dimensions

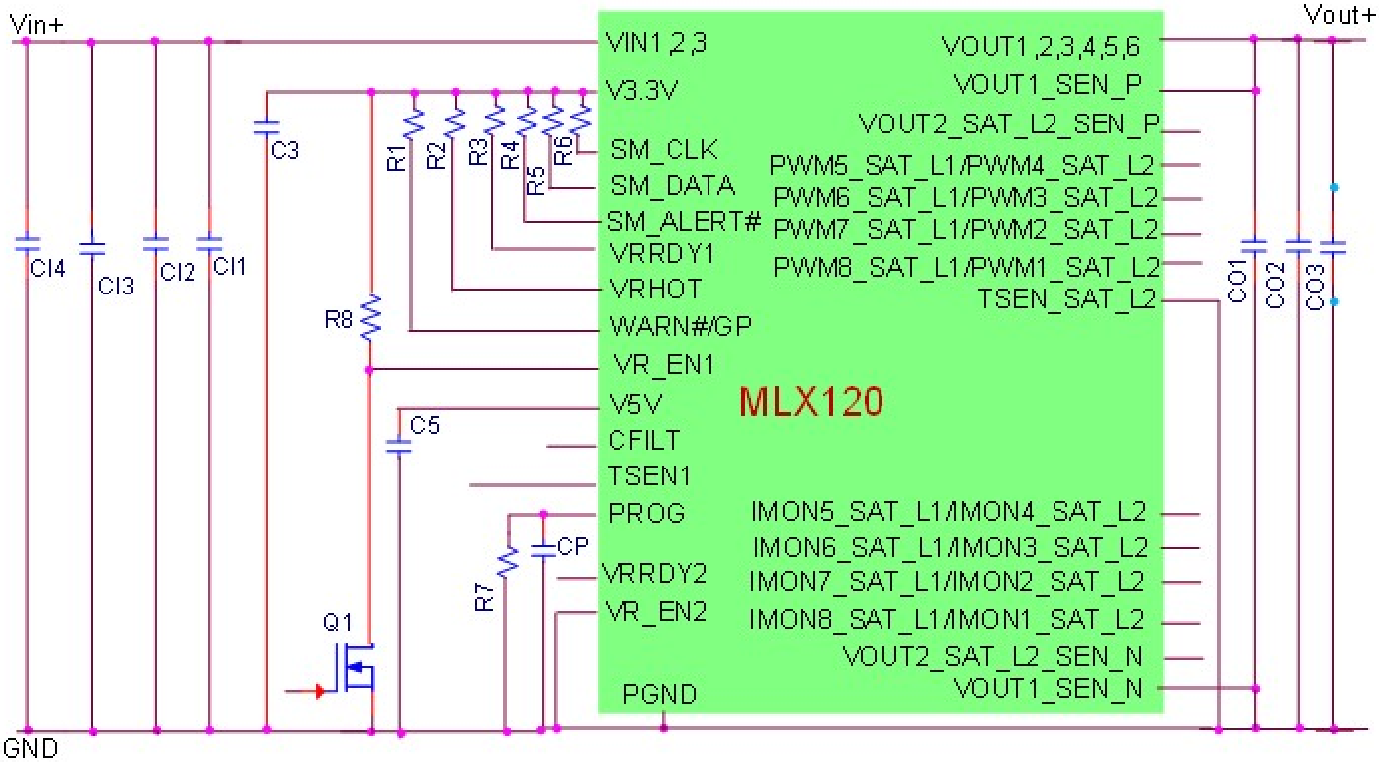


BOTTOM VIEW (ENLARGED for READABILITY)

Application Circuit (Based on Evaluation Board)

V_{IN} = 12V

V_{out} = 1V_{out}



CI1 – 4 banks (1µF + 1µF ceramic) – 8 caps total
CI2 – 4 Banks (4 x 10µF ceramic) – 16 caps total
CI3 – 4 Banks (4 x 22µF ceramic) – 16 caps total
CI4 – 4 Banks (1 x 560µF electrolytic) – 4 caps total
CO1 – 4 x 0.047µF+ 4 x 0.1µF - ceramic
CO2 – 15 x 22µFceramic + 73 x 47µFceramic + 6x470µF polymer or electrolytic
CO3 – 1 x 1500pF(0402) + 1 x 2200pF(0402) +1 x 0.022µF(0402) + 1 x 0.1uF(0402) - all ceramic
R8 based on Q1
R1, R2, R3 = 10K
R4,R5,R6 – based on PMBus controller / dongle being used
R7 – 845Ω—See PMBus addressing section
C5 – 1x10µF + 1x 22µF
CP – 0.01µF
TSEN1 is to be left floating if no Satellite on Loop 1
TSEN_SAT_L2 to be connected to Ground if no Satellite on Loop 2
SM_ALERT to be connected to Ground if not being used/monitored
PWMx_SATx_ are to be used only if Satellite is being used
IMONx_SATx are to be used only if Satellite is being used
VOUT2_SAT_L2_SEN_x are to be used only if Satellite is being used
CFILT, VR_EN2 are to be used only if Satellite is being used
VR_EN1 and VR_EN2 cannot be left floating

Technical Specifications (continued)

Thermal Considerations

Power modules operate in a variety of thermal environments; however, sufficient cooling should always be provided to help ensure reliable operation. Considerations include ambient temperature, airflow, module power dissipation, and the need for increased reliability. A reduction in the operating temperature of the module will result in an increase in reliability. The thermal data presented here is based on physical measurements taken in a wind tunnel. The test set-up is shown in Figure 34. The preferred airflow direction for cooling the module and the thermal reference points, Tref used in the specifications are shown in Figure 35. For reliable operation the temperatures at these points should not exceed 120°C (IC300) and 115°C (C202). The output power of the module should not exceed the rated power of the module (Vo,set x Io,max). Please refer to the Application Note "Thermal Characterization Process for Open-Frame Board-Mounted Power Modules" for a detailed discussion of thermal aspects including maximum device temperatures. Increased airflow over the module enhances the heat transfer via convection. The thermal derating of figures 2, 8, 14 and 20 show the maximum output current that can be delivered by each module in the indicated orientation without exceeding the maximum Tref temperature versus local ambient temperature (TA) for several air flow conditions. The thermal derating curves were generated using a 12 layer evaluation board with 3oz copper in inner layers and 2 oz in outer layers.

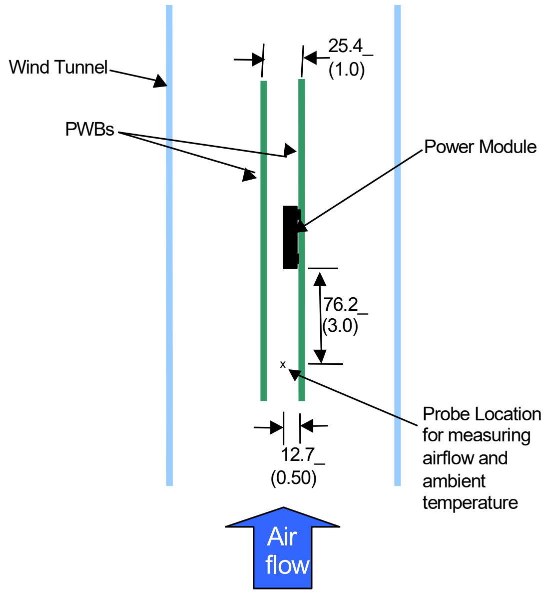


Figure 34. Thermal Test Setup.

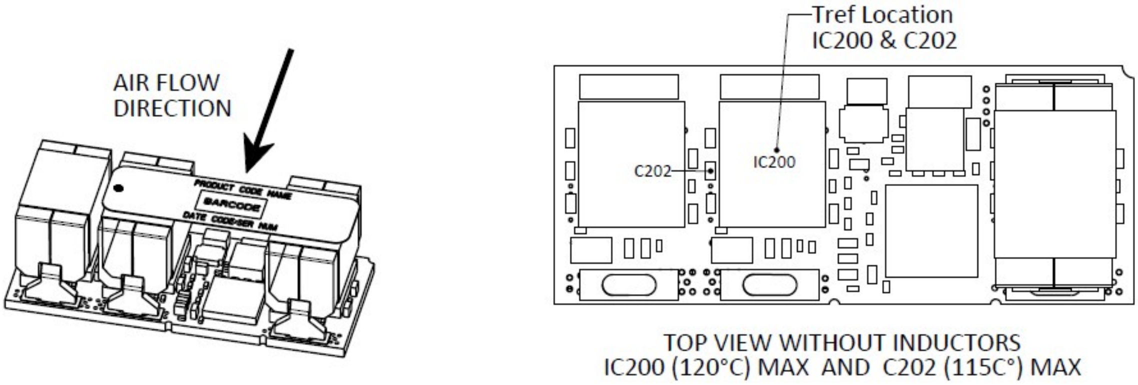


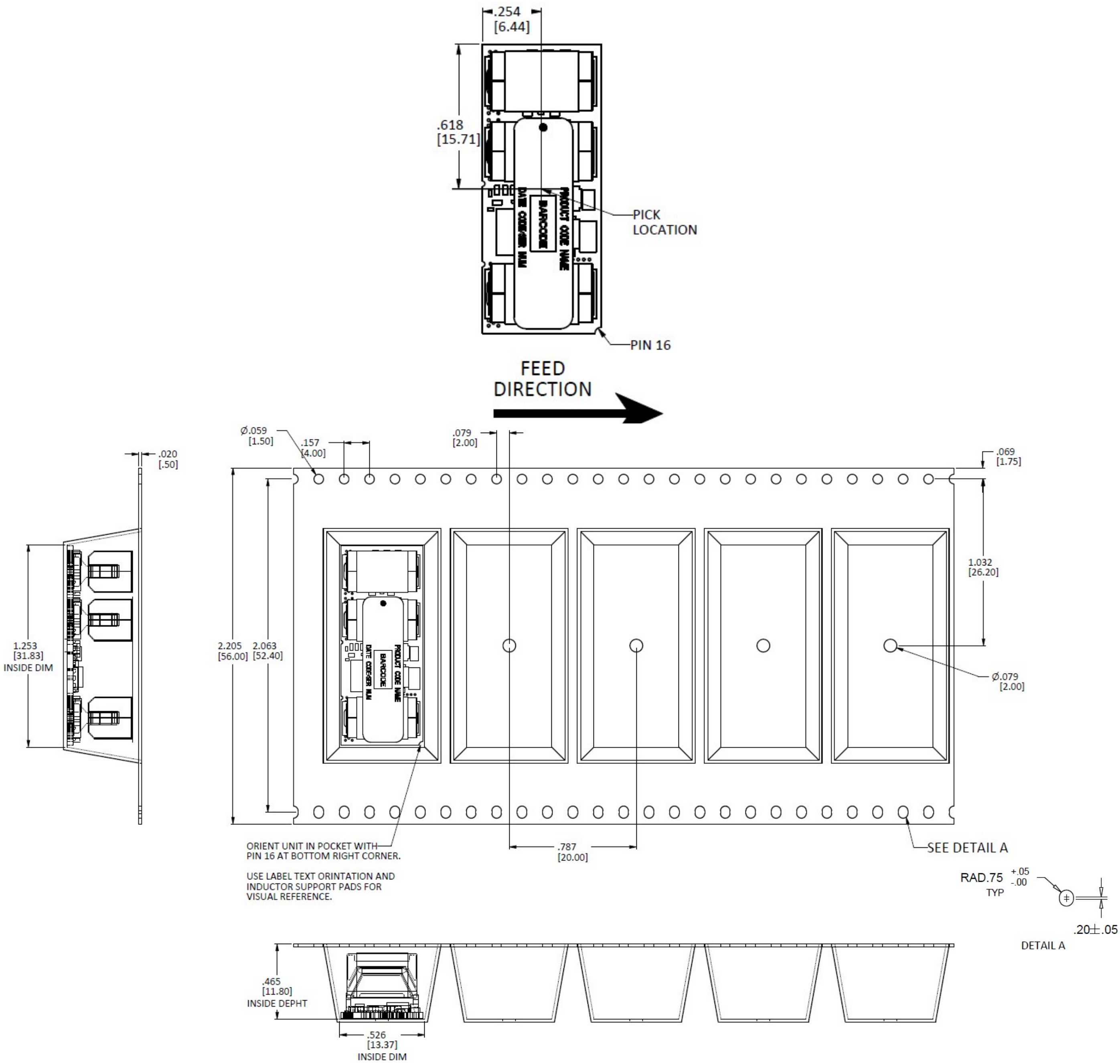
Figure 35. Preferred airflow direction and the location of the thermal reference points

Technical Specifications (continued)

Packaging Details

The MLX120 Open Frame modules are supplied in tape & reel as standard. Modules are shipped in quantities of 160 modules per reel. All Dimensions are in millimeters and (in inches).

Pick and Place Location



Reel Dimensions:

Outside Dimensions: 330.2mm (13”)

Inside Dimensions: 177.8 mm (7”)

Tape Width: 56.00mm (2.205”)

Technical Specifications (continued)

Surface Mount Information

Pick and Place

The MLX120 Open Frame modules use an open frame construction and are designed for a fully automated assembly process. The modules are fitted with a label designed to provide a large surface area for pick and place operations. The label meets all the requirements for surface mount processing, as well as safety standards, and is able to withstand reflow temperatures of up to 300 °C. The label also carries product information such as product code, serial number and the location of manufacture.

Nozzle Recommendations

Stencil thickness of 7 mils minimum must be used for this product. The module weight has been kept to a minimum by using open frame construction. Variables such as nozzle size, tip style, vacuum pressure and placement speed should be considered to optimize this process. The minimum recommended inside nozzle diameter for reliable operation is 3mm. The maximum nozzle outer diameter, which will safely fit within the allowable component spacing, is 7 mm.

Bottom Side / First Side Assembly

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Lead Free Soldering

The modules are lead-free (Pb-free) and RoHS compliant and fully compatible in a Pb-free soldering process. Failure to observe the instructions below may result in the failure of or cause damage to the modules and can adversely affect long-term reliability.

Pb-free Reflow Profile

Power Systems will comply with J-STD-020 Rev. D (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices) for both Pb-free solder profiles and MSL classification procedures. This standard provides a recommended forced-air-convection reflow profile based on the volume and thickness of the package (table 4-2). The suggested Pb-free solder paste is Sn/Ag/Cu (SAC). The recommended linear reflow profile using Sn/Ag/Cu solder is shown in Fig. 36. Soldering outside of the recommended profile requires testing to verify results and performance.

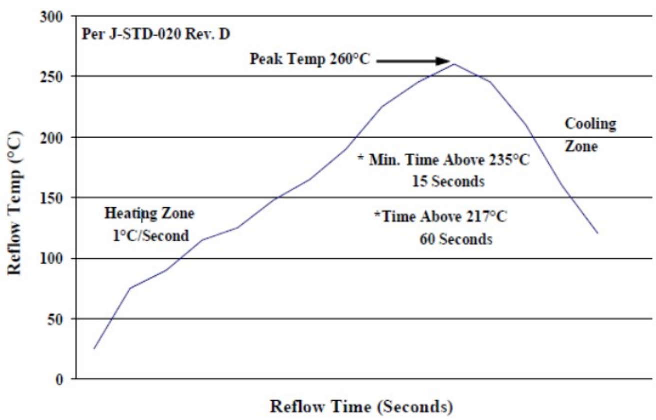


Figure 36. Recommended linear reflow profile using Sn/Ag/Cu solder

Technical Specifications (continued)

Surface Mount Information (continued)

MSL Rating

The MLX120A0XY3-SRZ Open Frame modules have a MSL rating of 2A.

Storage and Handling

The recommended storage environment and handling procedures for moisture-sensitive surface mount packages is detailed in J-STD-033 Rev. A (Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices). Moisture barrier bags (MBB) with desiccant are required for MSL ratings of 2 or greater. These sealed packages should not be broken until time of use. Once the original package is broken, the floor life of the product at conditions of 30°C and 60% relative humidity varies according to the MSL rating (see J-STD-033A). The shelf life for dry packed SMT packages will be a minimum of 12 months from the bag seal date, when stored at the following conditions: < 40° C, < 90% relative humidity.

Post Solder Cleaning and Drying Considerations

Post solder cleaning is usually the final circuit-board assembly process prior to electrical board testing. The result of inadequate cleaning and drying can affect both the reliability of a power module and the testability of the finished circuit-board assembly. For guidance on appropriate soldering, cleaning and drying procedures, refer to Board Mounted Power Modules: Soldering and Cleaning Application Note (AN04-001).

Technical Specifications (continued)

Ordering Information

Please contact your ABB Sales Representative for pricing, availability, and optional features.

Table 5. Device Codes

Device Code	Type	Input Voltage Range	Output Voltage	Output Current	On/Off Logic	Ordering code
MLX120A0XY3-SRZ	Master	7 – 14V_{DC}	0.45 – 2 V_{DC}	120A	Programmable	1600399279A

Table 6. Coding Scheme

Module type Identifier	Family	Sequencing Option	Output current	Output voltage	On/Off logic	Remote Sense	Options	ROHS Compliance
M	L	X	120A0	X	Y	3	-SR	Z
M=master S=satellite	L = DLynx III	T=with EZ Sequence X=without sequencing	120A	X = programmable output	Y = programmable enable logic	3 = Remote Sense	S = Surface Mount R = Tape & Reel	Z = ROHS Compliant

Table 7 Orderable Accessories

Manufacturer Part Number	Ordering Code	Description
EVAL MLX120	1600399280A	Evaluation Board with MLX120 module
DIGITAL_POL_EVAL_KIT	CC109164430	Digital Power Insights (DPI) it with USB dongle, needed cables, and a digital POL evaluation board (PDT012 or PJT020) and quick guide
I2C_USB_DONGLE_2.x	1600218857A	USB dongle required for use of Digital Power Insights software. Other contents of the DIGITAL_POL_EVAL_KIT are not included

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Change History (excludes grammar & clarifications)

Version	Date	Description of the change
1.6	4/17/ 2023	Updated typos and formatting

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