# UCC21530-Q1 4-A, 6-A, 5.7-kV$_{RMS}$ Isolated Dual-Channel Gate Driver with 3.3-mm Channel-to-Channel Spacing

## 1 Features

- AEC-Q100 qualified with:
  - Device temperature grade 1
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C6
- Functional Safety Quality-Managed
  - Documentation available to aid functional safety system design
- Universal: dual low-side, dual high-side or half-bridge driver
- Wide body SOIC-14 (DWK) package
- 3.3-mm spacing between driver channels
- Switching parameters:
  - 19-ns typical propagation delay
  - 10-ns minimum pulse width
  - 5-ns maximum delay matching
  - 6-ns maximum pulse-width distortion
- Common-mode transient immunity (CMTI) greater than 100-V/ns
- Isolation barrier life >40 years
- 4-A peak source, 6-A peak sink output
- TTL and CMOS compatible inputs
- 3-V to 18-V input VCCI range
- Up to 25-V VDD output drive supply
  - 8-V and 12-V VDD UVLO options
- Programmable overlap and dead time
- Rejects input pulses and noise transients shorter than 5 ns
- Operating temperature range –40 to +125°C
- Safety-related certifications:
  - 8000-V$_{PK}$ isolation per DIN V VDE V 0884-11 :2017-01
  - 5.7-kV$_{RMS}$ isolation for 1 minute per UL 1577
  - CSA certification per IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 end equipment standards
  - CQC certification per GB4943.1-2011

## 2 Applications

- HEV and BEV battery chargers
- Solar string and central inverters
- AC-to-DC and DC-to-DC charging piles
- AC inverter and servo drive
- AC-to-DC and DC-to-DC power delivery
- Energy storage systems

## 3 Description

The UCC21530-Q1 is an isolated dual-channel gate driver with 4-A source and 6-A sink peak current. It is designed to drive IGBTs, Si MOSFETs, and SiC MOSFETs up to 5-MHz with best-in-class propagation delay and pulse-width distortion.

The input side is isolated from the two output drivers by a 5.7-kV$_{RMS}$ reinforced isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI). Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1850 V.

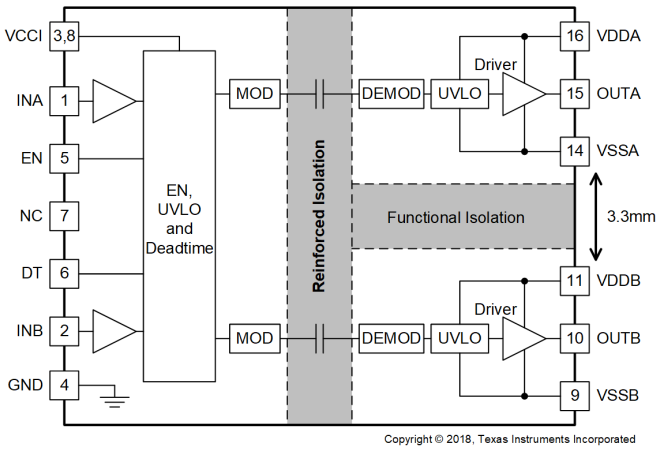
This driver can be configured as two low-side drivers, two high-side drivers, or a half-bridge driver with programmable dead time (DT). The EN pin pulled low shuts down both outputs simultaneously and allows for normal operation when left open or pulled high. As a fail-safe measure, primary-side logic failures force both outputs low.

The device accepts VDD supply voltages up to 25 V. A wide input VCCI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers. All the supply voltage pins have under voltage lock-out (UVLO) protection.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| UCC21530-Q1 | DWK SOIC (14) | 10.30 mm × 7.50 mm |
| UCC21530B-Q1 | DWK SOIC (14) | 10.30 mm × 7.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Functional Block Diagram**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (November 2018) to Revision C (March 2019) | Page |
|---|---|
| • Initial release | 1 |

| Changes from Revision C (March 2019) to Revision D (April 2021) | Page |
|---|---|
| • Added 8-V UVLO option to features, description, and device information sections | 1 |
| • Added information to pin 7 in Pin function table | 3 |
| • Added VDE certification, CSA master contract, and CQC certificate numbers to Safety-Related Certifications table | 7 |
| • Added 8-V UVLO thresholds to EC table | 8 |
| • Added 8-V UVLO thresholds and hysteresis across temperature | 11 |

# 5 Pin Configuration and Functions

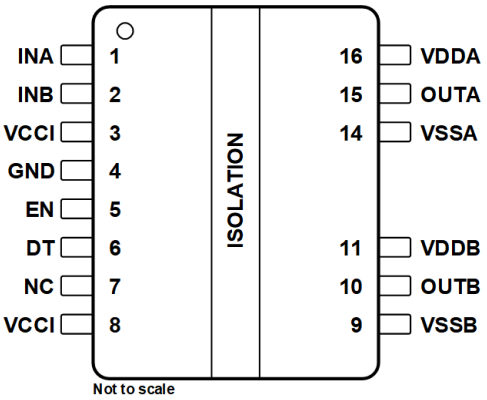



**Figure 5-1. DWK Package 14-Pin SOIC Top View**

## Pin Functions

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DT | 6 | I | DT pin configuration:<br>• Tying DT to VCCI disables the DT feature and allows the outputs to overlap.<br>• Placing a resistor ($R_{DT}$) between DT and GND adjusts dead time according to the equation: DT (in ns) = 10 × $R_{DT}$ (in kΩ). TI recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, close to DT pin to achieve better noise immunity. |
| EN | 5 | I | Enable both driver outputs if asserted high, disable the output if set low. It is recommended to tie this pin to VCCI if not used to achieve better noise immunity. Bypass using a ≈ 1-nF low ESR/ESL capacitor close to EN pin when connecting to a micro controller with distance. |
| GND | 4 | P | Primary-side ground reference. All signals in the primary side are referenced to this ground. |
| INA | 1 | I | Input signal for A channel. INA input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. |
| INB | 2 | I | Input signal for B channel. INB input has a TTL/CMOS compatible input threshold. This pin is pulled low internally if left open. It is recommended to tie this pin to ground if not used to achieve better noise immunity. |
| NC | 7 | – | No internal connection. This pin can be left floating, tied to VCCI, or tied to GND. |
| OUTA | 15 | O | Output of driver A. Connect to the gate of the A channel FET or IGBT. |
| OUTB | 10 | O | Output of driver B. Connect to the gate of the B channel FET or IGBT. |
| VCCI | 3 | P | Primary-side supply voltage. Locally decoupled to GND using a low ESR/ESL capacitor located as close to the device as possible. |
| VCCI | 8 | P | Primary-side supply voltage. This pin is internally shorted to pin 3. |
| VDDA | 16 | P | Secondary-side power for driver A. Locally decoupled to VSSA using a low ESR/ESL capacitor located as close to the device as possible. |
| VDDB | 11 | P | Secondary-side power for driver B. Locally decoupled to VSSB using low ESR/ESL capacitor located as close to the device as possible. |
| VSSA | 14 | P | Ground for secondary-side driver A. Ground reference for secondary side A channel. |
| VSSB | 9 | P | Ground for secondary-side driver B. Ground reference for secondary side B channel. |

(1) P =Power, I= Input, O= Output

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input bias pin supply voltage | VCCI to GND | –0.5 | 20 | V |
| Driver bias supply | VDDA-VSSA, VDDB-VSSB | –0.5 | 30 | V |
| Output signal voltage | OUTA to VSSA, OUTB to VSSB | –0.5 | $V_{VDDA}$+0.5, $V_{VDDB}$+0.5 | V |
| | OUTA to VSSA, OUTB to VSSB, Transient for 200 ns | –2 | $V_{VDDA}$+0.5, $V_{VDDB}$+0.5 | V |
| Input signal voltage | INA, INB, EN, DT to GND | –0.5 | $V_{VCCI}$+0.5 | V |
| | INA, INB Transient for 200ns | –2 | $V_{VCCI}$+0.5 | V |
| Channel to channel internal isolation voltage | \|VSSA-VSSB\| | | 1850 | V |
| Junction temperature, $T_J$ (2) | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) To maintain the recommended operating conditions for $T_J$, see the *Section 6.4*.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| VCCI | VCCI Input supply voltage | | 3 | 18 | V |
| VDDA-VSSA, VDDB-VSSB | Driver output bias supply refer to Vss | 8-V UVLO version - UCC21530B-Q1 | 9.2 | 25 | V |
| | | 12-V UVLO version - UCC21530-Q1 | 14.7 | 25 | V |
| $T_A$ | Ambient Temperature | | –40 | 125 | °C |
| $T_J$ | Junction Temperature | | –40 | 130 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | UCC21530-Q1 | UNIT |
|---|---|---|---|
| | | DWK-14 (SOIC) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 68.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 31.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 27.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 17.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 27 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Power Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $P_D$ | Power dissipation by UCC21530-Q1 | VCCI = 18 V, VDDA/B = 15 V, INA/B = 3.3 V, 3.9 MHz 50% duty cycle square wave 1-nF load | 1810 | mW |
| $P_{DI}$ | Power dissipation by transmitter side of UCC21530-Q1 | | 50 | mW |
| $P_{DA}$, $P_{DB}$ | Power dissipation by each driver side of UCC21530-Q1 | | 880 | mW |

## 6.6 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| CLR | External clearance(1) | Shortest pin-to-pin distance through air | > 8 | mm |
| CPG | External creepage(1) | Shortest pin-to-pin distance across the package surface | > 8 | mm |
| DTI | Distance through insulation | Minimum internal gap (internal clearance) of the double insulation (2 × 10.5 µm) | >21 | µm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | > 600 | V |
| | Material group | According to IEC 60664-1 | I | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 600 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 1000 $V_{RMS}$ | I-III | |
| **DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01(2)** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 2121 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum working isolation voltage | AC voltage (sine wave); time dependent dielectric breakdown (TDDB), test (See Figure 6-1) | 1500 | $V_{RMS}$ |
| | | DC voltage | 2121 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST}$ = $V_{IOTM}$, t = 60 sec (qualification)<br>$V_{TEST}$ = 1.2 × $V_{IOTM}$, t = 1 s (100% production) | 8000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 62368-1, 1.2/50 µs waveform,<br>$V_{TEST}$ = 1.6 × $V_{IOSM}$ = 12800 $V_{PK}$ (qualification) | 8000 | $V_{PK}$ |
| $q_{pd}$ | Apparent charge(4) | Method a, After Input/Output safety test subgroup 2/3.<br>$V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60s;<br>$V_{pd(m)}$ = 1.2 X $V_{IORM}$ = 2545 $V_{PK}$, $t_m$ = 10s | <5 | pC |
| | | Method a, After environmental tests subgroup 1.<br>$V_{ini}$ = $V_{IOTM}$, $t_{ini}$ = 60s;<br>$V_{pd(m)}$ = 1.6 X $V_{IORM}$ = 3394 $V_{PK}$, $t_m$ = 10s | <5 | |
| | | Method b1; At routine test (100% production) and preconditioning (type test)<br>$V_{ini}$ = 1.2 × $V_{IOTM}$; $t_{ini}$ = 1s;<br>$V_{pd(m)}$ = 1.875 * $V_{IORM}$ = 3977 $V_{PK}$ , $t_m$ = 1s | <5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.4 sin (2πft), f =1 MHz | 1.2 | pF |
| $R_{IO}$ | Isolation resistance, input to output(5) | $V_{IO}$ = 500 V at $T_A$ = 25°C | > $10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V at 100°C ≤ $T_A$ ≤ 125°C | > $10^{11}$ | |
| | | $V_{IO}$ = 500 V at $T_S$ =150°C | > $10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST}$ = $V_{ISO}$ = 5700 $V_{RMS}$, t = 60 sec. (qualification),<br>$V_{TEST}$ = 1.2 × $V_{ISO}$ = 6840$V_{RMS}$, t = 1 sec (100% production) | 5700 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Safety-Related Certifications

| VDE | CSA | UL | CQC |
|---|---|---|---|
| Certified according to DIN V VDE V 0884-11:2017-01 and DIN EN 60950-1 (VDE 0805 Tiel 1):2014-08 | Certified according to IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB 4943.1-2011 |
| Reinforced Insulation Maximum Transient Isolation voltage, 8000 VPK; Maximum Repetitive Peak Isolation Voltage, 2121 VPK; Maximum Surge Isolation Voltage, 8000 VPK | Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2, 800 VRMS maximum working voltage (pollution degree 2, material group I) Reinforced insulation per CSA 62368-1-14 and IEC 62368-1 2nd Ed., 800 VRMS maximum working voltage (pollution degree 2, material group I); Basic insulation per CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed., 600 VRMS maximum working voltage (pollution degree 2, material group III); 2 MOPP (Means of Patient Protection) per CSA 60601- 1:14 and IEC 60601-1 Ed.3+A1, 250 VRMS maximum working voltage | Single protection, 5700 $V_{RMS}$ | Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate 660 VRMS maximum working voltage |
| Certification number: 40040142 | Master contract number: 220991 | File number: E181974 | Certificate number: CQC16001155011 |

## 6.8 Safety-Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | SIDE | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_S$ | Safety output supply current | $R_{\theta JA}$ = 68.3°C/W, VDDA/B = 15 V, $T_A$ = 25°C, $T_J$ = 150°C See Figure 6-2 | DRIVER A, DRIVER B | | | 58 | mA |
| | | $R_{\theta JA}$ = 68.3°C/W, VDDA/B = 25 V, $T_A$ = 25°C, $T_J$ = 150°C See Figure 6-2 | DRIVER A, DRIVER B | | | 35 | mA |
| $P_S$ | Safety supply power | $R_{\theta JA}$ = 68.3°C/W, $T_A$ = 25°C, $T_J$ = 150°C See Figure 6-3 | INPUT | | | 50 | mW |
| | | | DRIVER A | | | 880 | |
| | | | DRIVER B | | | 880 | |
| | | | TOTAL | | | 1810 | |
| $T_S$ | Safety temperature(1) | | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power respectively. The maximum limits of $I_S$ and $P_S$ should not be exceeded. These limits vary with the ambient temperature, $T_A$.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Section 6.4* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$ , where $V_I$ is the maximum input voltage.

## 6.9 Electrical Characteristics

$V_{VCCI}$ = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12V or 15V(1), 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, DT pin tied to VCCI, $C_L$ = 0 pF, $T_A$ = –40°C to +125°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{VCCI}$ | VCCI quiescent current | $V_{INA}$ = 0 V, $V_{INB}$ = 0 V | | 1.5 | 2.0 | mA |
| $I_{VDDA}$, $I_{VDDB}$ | VDDA and VDDB quiescent current | $V_{INA}$ = 0 V, $V_{INB}$ = 0 V | | 1.0 | 1.8 | mA |
| $I_{VCCI}$ | VCCI per operating current | (f = 500 kHz) current per channel | | 2.0 | | mA |
| $I_{VDDA}$, $I_{VDDB}$ | VDDA and VDDB operating current | (f = 500 kHz) current per channel, $C_{OUT}$ = 100 pF, $V_{VDDA}$, $V_{VDDB}$ = 15 V | | 3.0 | | mA |
| **VCCI TO GND UNDERVOLTAGE THRESHOLDS** | | | | | | |
| $V_{VCCI\_ON}$ | UVLO Rising threshold | | 2.55 | 2.7 | 2.85 | V |
| $V_{VCCI\_OFF}$ | UVLO Falling threshold | | 2.35 | 2.5 | 2.65 | V |
| $V_{VCCI\_HYS}$ | UVLO Threshold hysteresis | | | 0.2 | | V |
| **UCC21530B-Q1 VDD to VSS UNDERVOLTAGE THRESHOLDS** | | | | | | |
| $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | UVLO Rising threshold | | 8 | 8.5 | 9 | V |
| $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | UVLO Falling threshold | | 7.5 | 8 | 8.5 | V |
| $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | UVLO Threshold hysteresis | | | 0.5 | | V |
| **UCC21530-Q1 VDD TO VSS UNDERVOLTAGE THRESHOLDS** | | | | | | |
| $V_{VDDA\_ON}$, $V_{VDDB\_ON}$ | UVLO Rising threshold | | 12.5 | 13.5 | 14.5 | V |
| $V_{VDDA\_OFF}$, $V_{VDDB\_OFF}$ | UVLO Falling threshold | | 11.5 | 12.5 | 13.5 | V |
| $V_{VDDA\_HYS}$, $V_{VDDB\_HYS}$ | UVLO Threshold hysteresis | | | 1.0 | | V |
| **INA and INB** | | | | | | |
| $V_{INAH}$, $V_{INBH}$ | Input high threshold voltage | | 1.6 | 1.8 | 2 | V |
| $V_{INAL}$, $V_{INBL}$ | Input low threshold voltage | | 0.8 | 1 | 1.2 | V |
| $V_{INA\_HYS}$, $V_{INB\_HYS}$ | Input threshold hysteresis | | | 0.8 | | V |
| $V_{INA}$, $V_{INB}$ | Negative transient, ref to GND, 50 ns pulse | Not production tested, bench test only | –5 | | | V |
| **EN THRESHOLDS** | | | | | | |
| $V_{ENH}$ | Enable high voltage | | 2.0 | | | V |
| $V_{ENL}$ | Enable low voltage | | | | 0.8 | V |

$V_{VCCI}$ = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12V or 15V(1), 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, DT pin tied to VCCI, $C_L$ = 0 pF, $T_A$ = –40°C to +125°C, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | |
| $I_{OA+}$, $I_{OB+}$ | Peak output source current | $C_{VDD}$ = 10 µF, $C_{LOAD}$ = 0.18 µF, f = 1 kHz, bench measurement | | 4 | | A |
| $I_{OA-}$, $I_{OB-}$ | Peak output sink current | $C_{VDD}$ = 10 µF, $C_{LOAD}$ = 0.18 µF, f = 1 kHz, bench measurement | | 6 | | A |
| $R_{OHA}$, $R_{OHB}$ | Output resistance at high state | $I_{OUT}$ = –10 mA, $T_A$ = 25°C, $R_{OHA}$, $R_{OHB}$ do not represent drive pull-up performance. See $t_{RISE}$ in *Section 6.10* and *Section 8.3.4* for details. | | 5 | | Ω |
| $R_{OLA}$, $R_{OLB}$ | Output resistance at low state | $I_{OUT}$ = 10 mA, $T_A$ = 25°C | | 0.55 | | Ω |
| $V_{OHA}$, $V_{OHB}$ | Output voltage at high state | $V_{VDDA}$, $V_{VDDB}$ = 15 V, $I_{OUT}$ = –10 mA, $T_A$ = 25°C | | 14.95 | | V |
| $V_{OLA}$, $V_{OLB}$ | Output voltage at low state | $V_{VDDA}$, $V_{VDDB}$ = 15 V, $I_{OUT}$ = 10 mA, $T_A$ = 25°C | | 5.5 | | mV |
| **DEADTIME AND OVERLAP PROGRAMMING** | | | | | | |
| Dead time | | DT pin tied to VCCI | Overlap determined by INA INB | | | - |
| | | $R_{DT}$ = 20 kΩ | 160 | 200 | 240 | ns |

## 6.10 Switching Characteristics

$V_{VCCI}$ = 3.3 V or 5 V, 0.1-µF capacitor from VCCI to GND, $V_{VDDA}$ = $V_{VDDB}$ = 12V or 15V(1), 1-µF capacitor from VDDA and VDDB to VSSA and VSSB, $T_A$ = –40°C to +125°C, (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{RISE}$ | Output rise time, 20% to 80% measured points | $C_{OUT}$ = 1.8 nF | | 6 | 16 | ns |
| $t_{FALL}$ | Output fall time, 90% to 10% measured points | $C_{OUT}$ = 1.8 nF | | 7 | 12 | ns |
| $t_{PWmin}$ | Minimum pulse width | Output off for less than minimum, $C_{OUT}$ = 0 pF | | | 20 | ns |
| $t_{PDHL}$ | Propagation delay from INx to OUTx falling edges | | 14 | 19 | 30 | ns |
| $t_{PDLH}$ | Propagation delay from INx to OUTx rising edges | | 14 | 19 | 30 | ns |
| $t_{PWD}$ | Pulse width distortion $\lvert t_{PDLH} - t_{PDHL} \rvert$ | | | | 6 | ns |
| $t_{DM}$ | Propagation delays matching between VOUTA, VOUTB | f = 100 kHz | | | 5 | ns |
| $t_{VCCI+ to OUT}$ | VCCI Power-up Delay Time: UVLO Rise to OUTA, OUTB, See *Figure 7-5* | INA or INB tied to VCCI | | 40 | | µs |
| $t_{VDD+ to OUT}$ | VDDA, VDDB Power-up Delay Time: UVLO Rise to OUTA, OUTB See *Figure 7-6* | INA or INB tied to VCCI | | 50 | | µs |
| $\lvert CM_H \rvert$ | High-level common-mode transient immunity (See *Section 7.6*) | Slew rate of GND vs. VSSA/B, INA and INB both are tied to GND or VCCI; $V_{CM}$=1500 V; | 100 | | | V/ns |
| $\lvert CM_L \rvert$ | Low-level common-mode transient immunity (See *Section 7.6*) | Slew rate of GND vs. VSSA/B, INA and INB both are tied to GND or VCCI; $V_{CM}$=1500 V; | 100 | | | V/ns |

## 6.11 Insulation Characteristics Curves

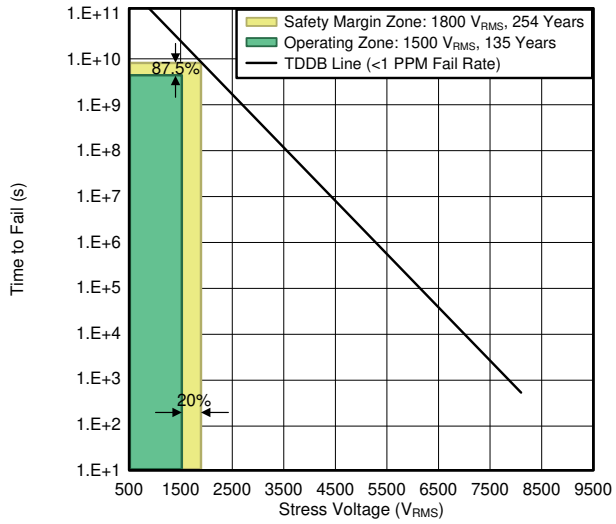



**Figure 6-1. Reinforced Isolation Capacitor Life Time Projection**

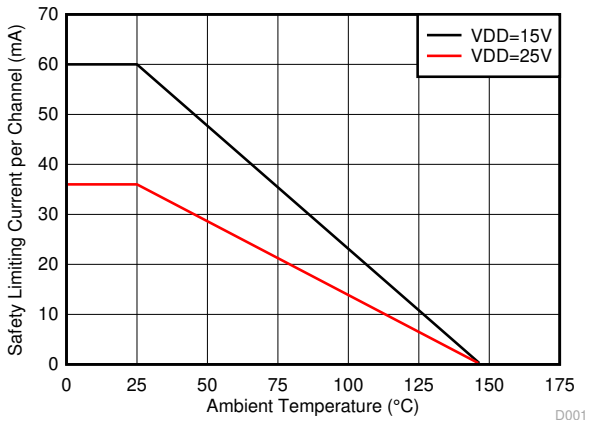



**Figure 6-2. Thermal Derating Curve for Safety-Related Limiting Current (Current in Each Channel with Both Channels Running Simultaneously)**

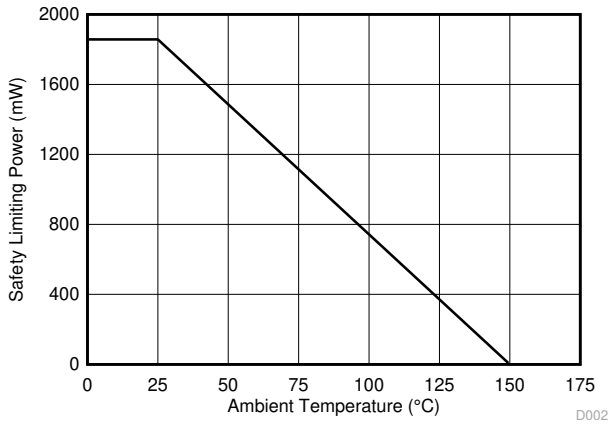



**Figure 6-3. Thermal Derating Curve for Safety-Related Limiting Power**

## 6.12 Typical Characteristics

VDDA = VDDB = 15 V, VCCI = 3.3 V, $T_A$ = 25°C, No load. (unless otherwise noted)

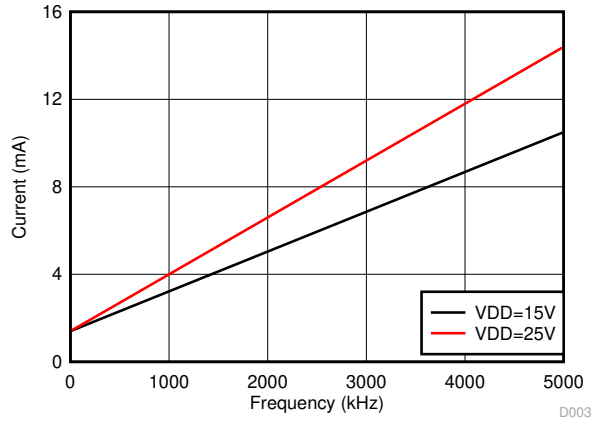



**Figure 6-4. Per Channel Current Consumption vs. Frequency (No Load, VDD = 15 V or 25 V)**

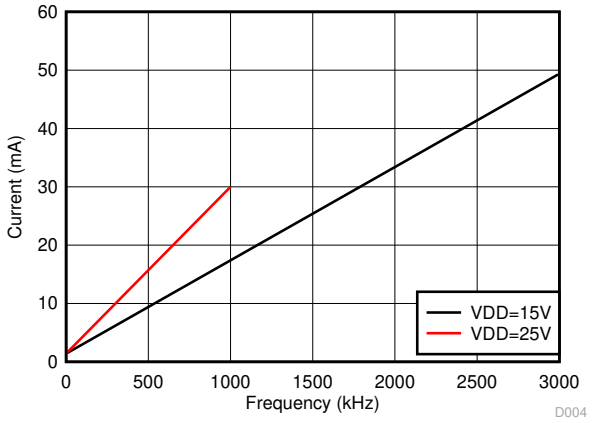



**Figure 6-5. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (1-nF Load, VDD = 15 V or 25 V)**

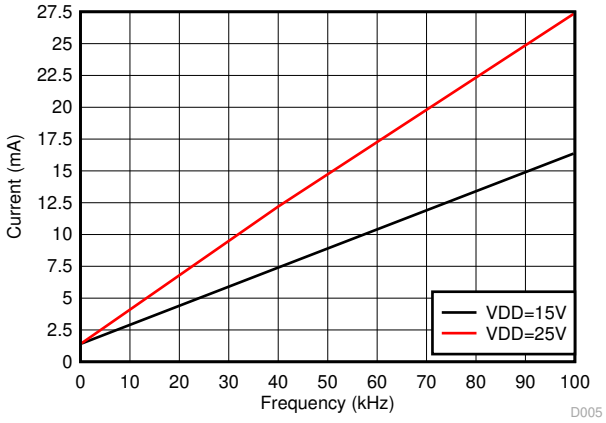



**Figure 6-6. Per Channel Current Consumption ($I_{VDDA/B}$) vs. Frequency (10-nF Load, VDD = 15 V or 25 V)**

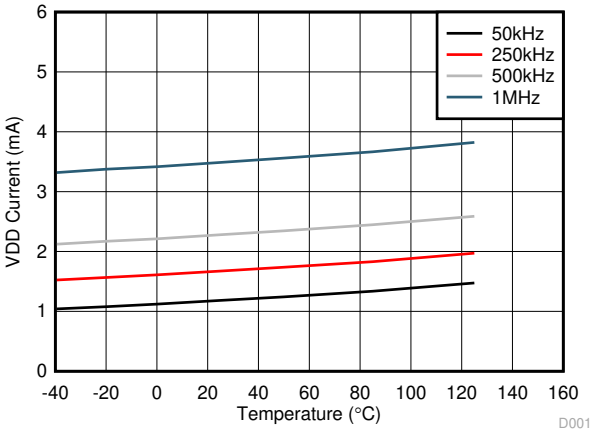



**Figure 6-7. Per Channel ($I_{VDDA/B}$) Supply Current Vs. Temperature (VDD=15V, No Load, Different Switching Frequencies)**

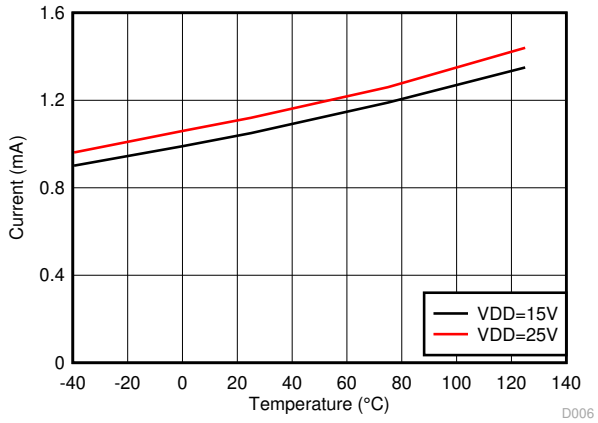



**Figure 6-8. Per Channel ($I_{VDDA/B}$) Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)**

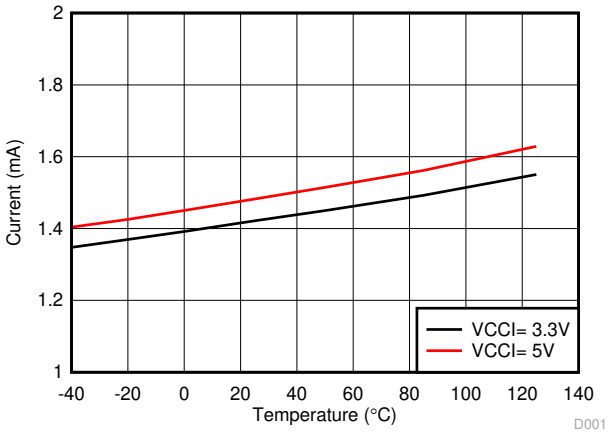



**Figure 6-9. $I_{VCCI}$ Quiescent Supply Current vs Temperature (No Load, Input Low, No Switching)**

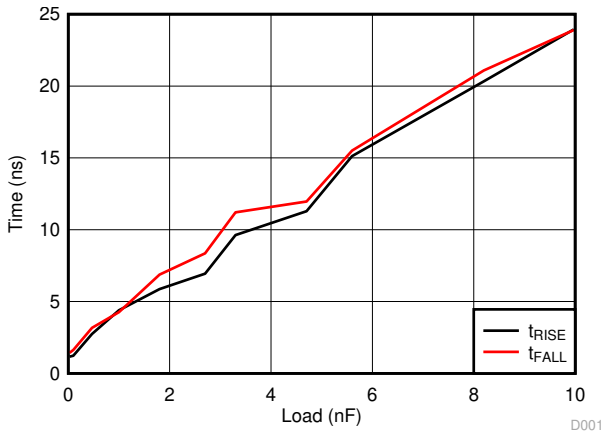



**Figure 6-10. Rising and Falling Times vs. Load**

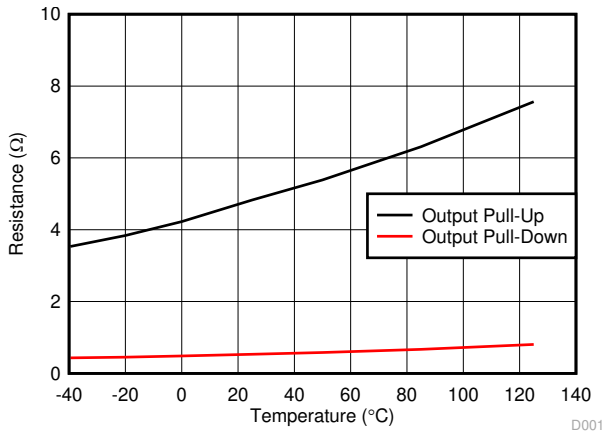



**Figure 6-11. Output Resistance vs. Temperature**

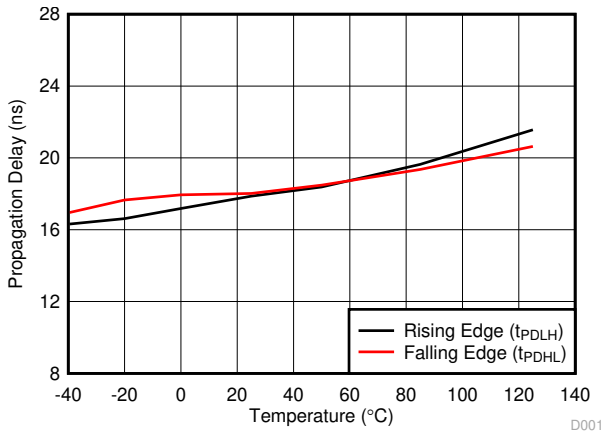



**Figure 6-12. Propagation Delay vs. Temperature**

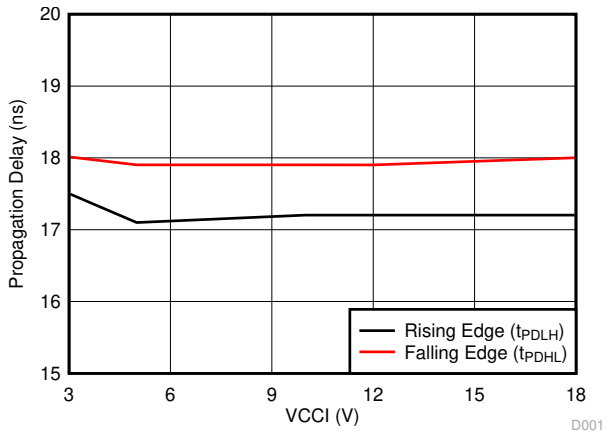



**Figure 6-13. Propagation Delay vs. VCCI**

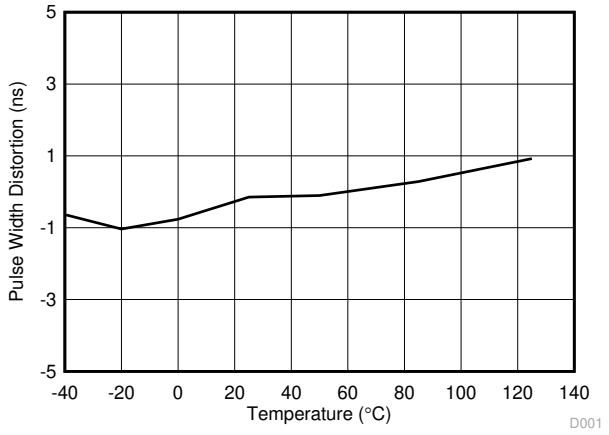



**Figure 6-14. Pulse Width Distortion vs. Temperature**

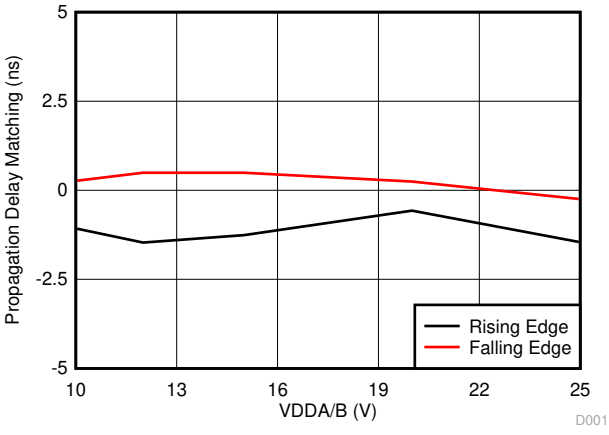



**Figure 6-15. Propagation Delay Matching ($t_{DM}$) vs. VDD**

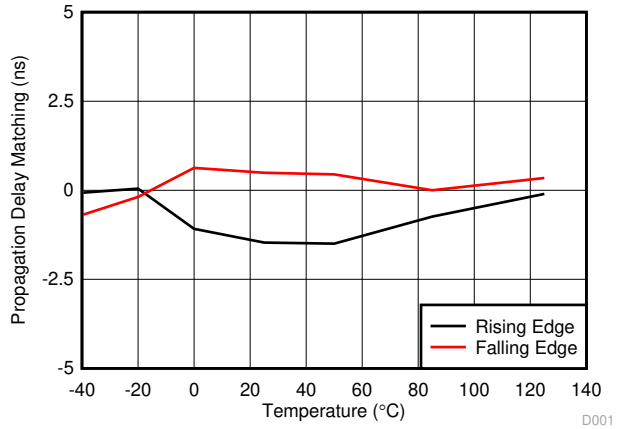



**Figure 6-16. Propagation Delay Matching ($t_{DM}$) vs. Temperature**

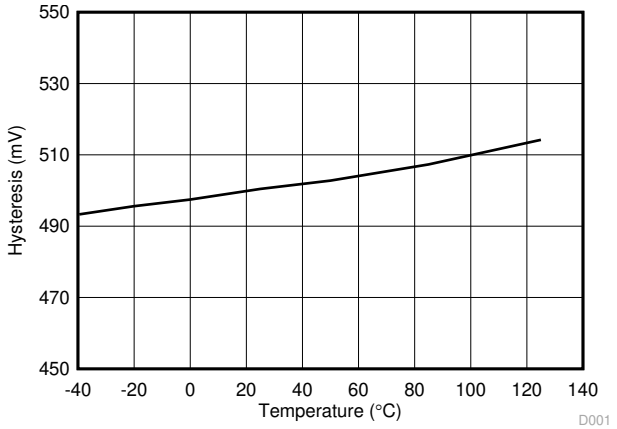



**Figure 6-17. 8-V UVLO Hysteresis vs. Temperature**

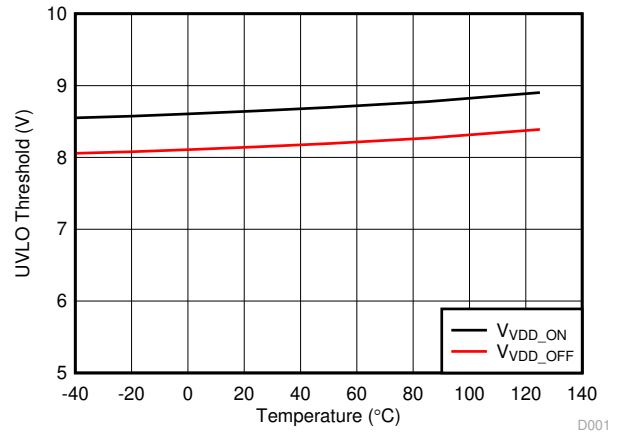



**Figure 6-18. 8-V UVLO Threshold vs. Temperature**

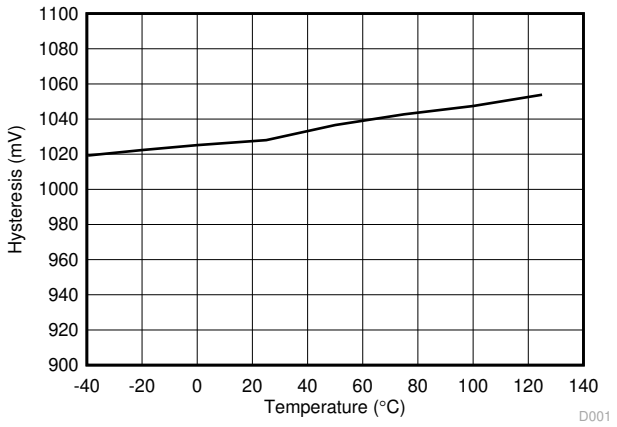



**Figure 6-19. 12-V UVLO Hysteresis vs. Temperature**

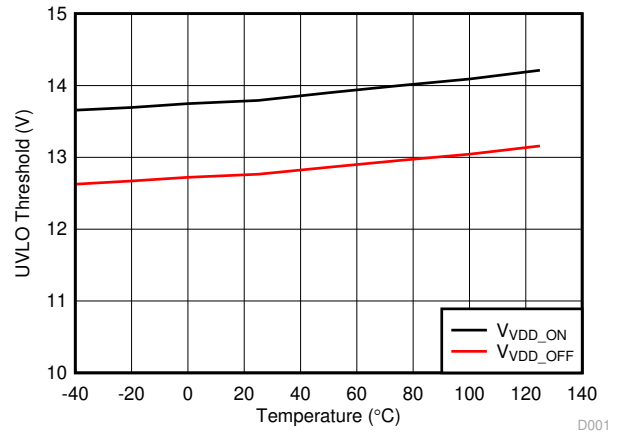



**Figure 6-20. 12-V UVLO Threshold vs. Temperature**

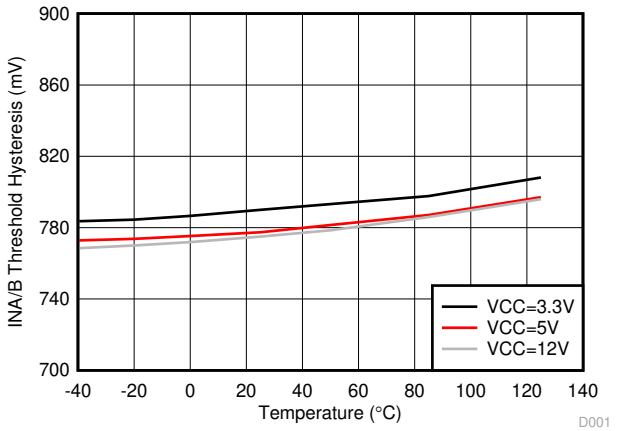



**Figure 6-21. INA/B Hysteresis vs. Temperature**

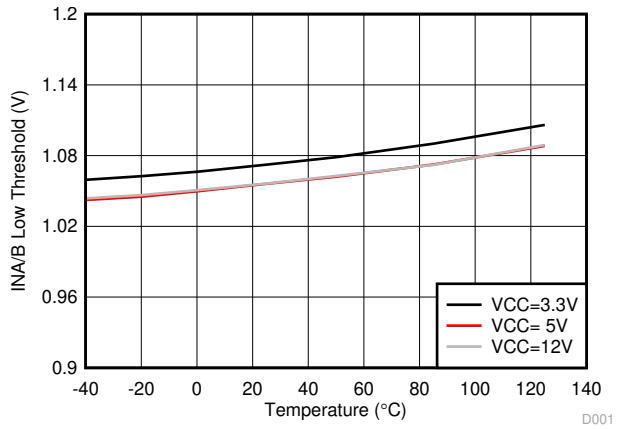



**Figure 6-22. INA/B Low Threshold**

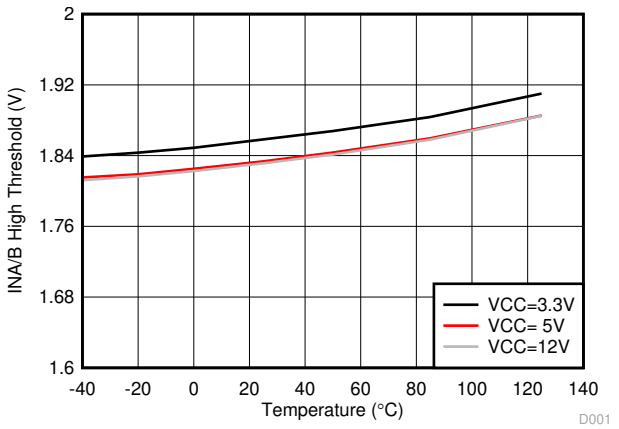



**Figure 6-23. INA/B High Threshold**

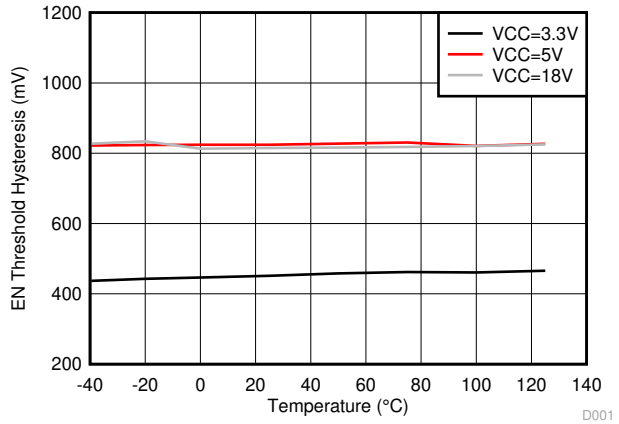



**Figure 6-24. EN Threshold Hysteresis vs. Temperature**

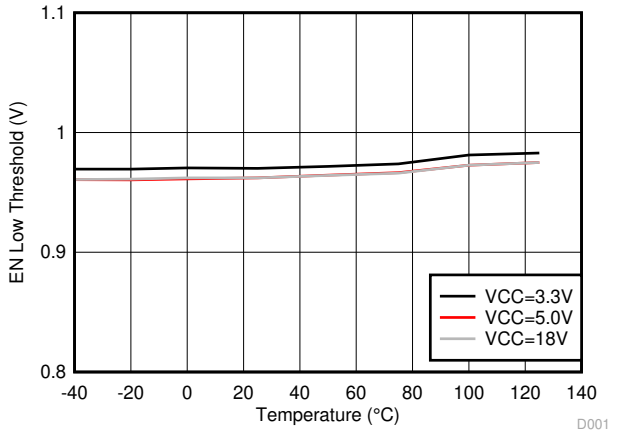



**Figure 6-25. EN Low Threshold**

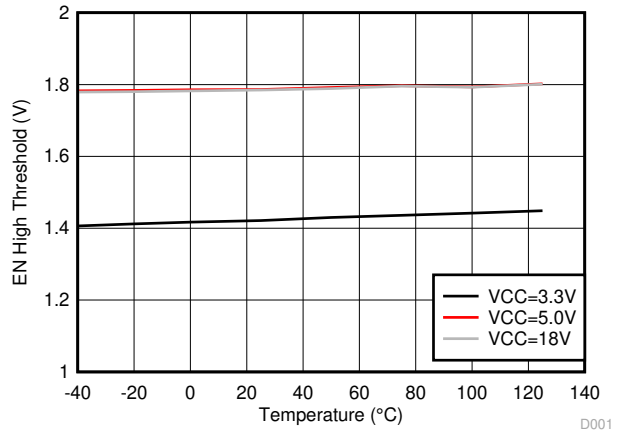



**Figure 6-26. EN High Threshold**

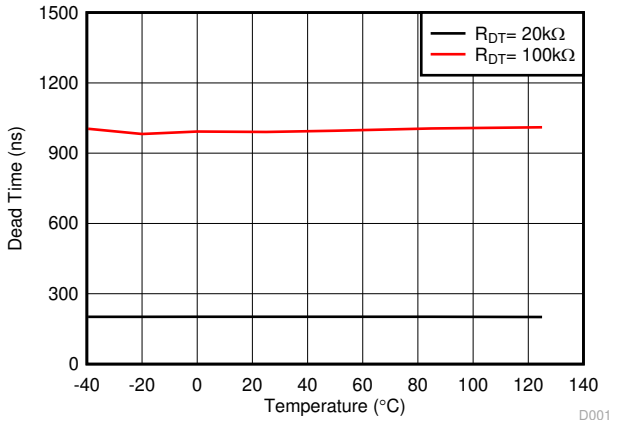



**Figure 6-27. Dead Time vs. Temperature (with $R_{DT}$ = 20 kΩ and 100 kΩ)**

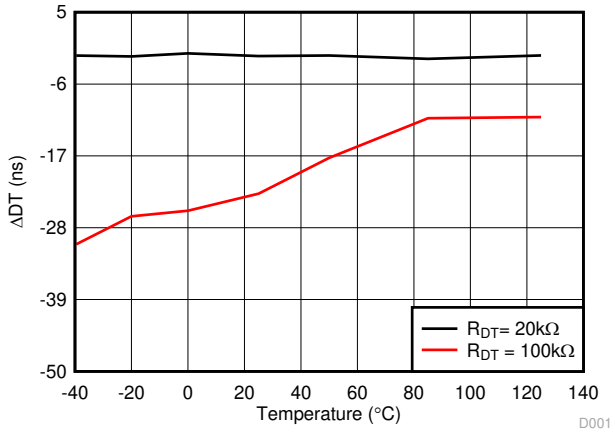



**Figure 6-28. Dead Time Matching vs. Temperature (with $R_{DT}$ = 20 kΩ and 100 kΩ)**

# 7 Parameter Measurement Information

## 7.1 Propagation Delay and Pulse Width Distortion

Figure 7-1 shows how one calculates pulse width distortion ($t_{PWD}$) and delay matching ($t_{DM}$) from the propagation delays of channels A and B. It can be measured by ensuring that both inputs are in phase and disabling the dead time function by shorting the DT Pin to VCC.

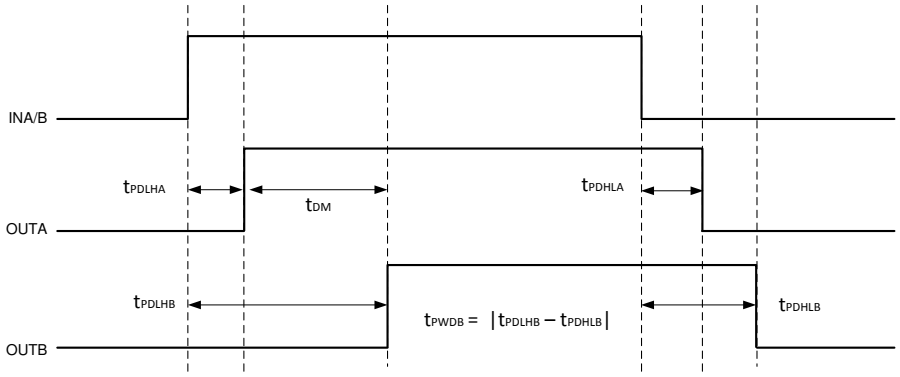



**Figure 7-1. Overlapping Inputs, Dead Time Disabled**

## 7.2 Rising and Falling Time

*Figure 7-2* shows the criteria for measuring rising ($t_{RISE}$) and falling ($t_{FALL}$) times. For more information on how short rising and falling times are achieved see *Section 8.3.4*.

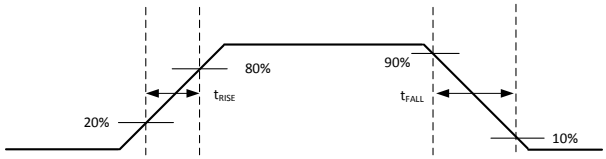



**Figure 7-2. Rising and Falling Time Criteria**

## 7.3 Input and Enable Response Time

*Figure 7-3* shows the response time of the enable function. For more information, see *Section 8.4.1* .

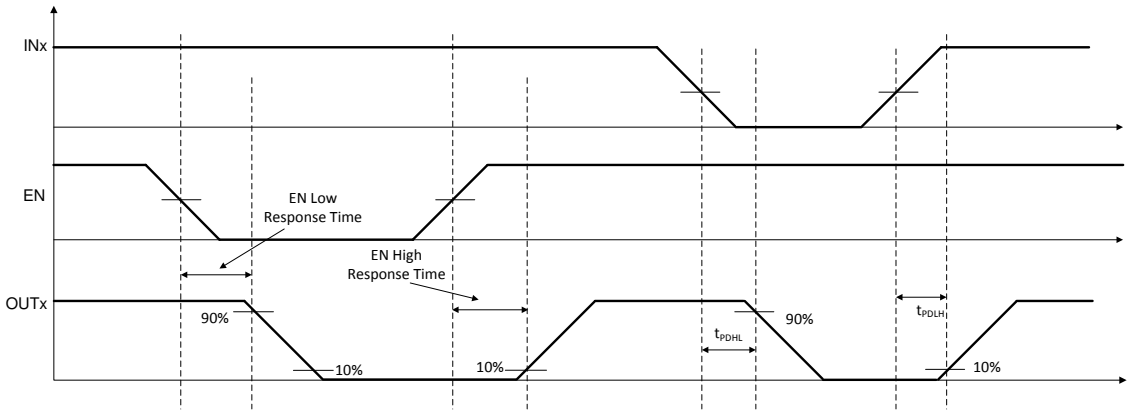



**Figure 7-3. Enable Pin Timing**

## 7.4 Programable Dead Time

Tying DT to VCCI disables DT feature and allows the outputs to overlap. Placing a resistor ($R_{DT}$) between DT pin and GND can adjust the dead time. For more details on dead time, refer to *Section 8.4.2* .

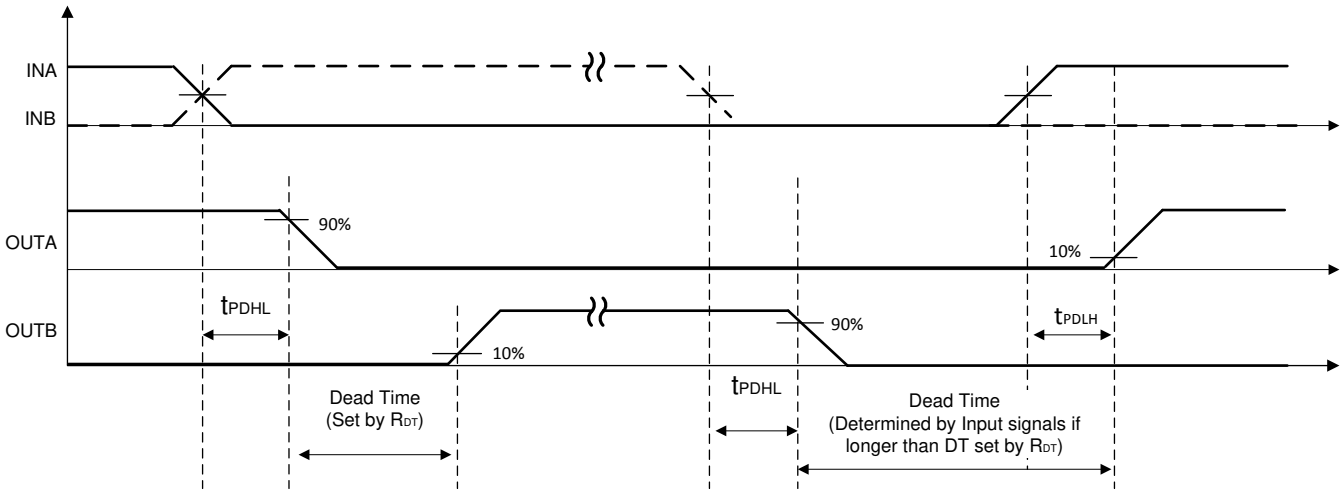



**Figure 7-4. Dead-Time Switching Parameters**

## 7.5 Power-Up UVLO Delay to OUTPUT

Whenever the supply voltage VCCI crosses from below the falling threshold $V_{VCCI\_OFF}$ to above the rising threshold $V_{VCCI\_ON}$, and whenever the supply voltage VDDx crosses from below the falling threshold $V_{VDDx\_OFF}$ to above the rising threshold $V_{VDDx\_ON}$, there is a delay before the outputs begin responding to the inputs. For VCCI UVLO this delay is defined as $t_{VCCI+ \text{ to } OUT}$, and is typically 40 µs. For VDDx UVLO this delay is defined as $t_{VDD+ \text{ to } OUT}$, and is typically 50 µs. TI recommends allowing some margin before driving input signals, to ensure the driver VCCI and VDD bias supplies are fully activated. *Figure 7-5* and *Figure 7-6* show the power-up UVLO delay timing diagram for VCCI and VDD.

Whenever the supply voltage VCCI crosses below the falling threshold $V_{VCCI\_OFF}$, or VDDx crosses below the falling threshold $V_{VDDx\_OFF}$, the outputs stop responding to the inputs and are held low within 1 µs. This asymmetric delay is designed to ensure safe operation during VCCI or VDDx brownouts.

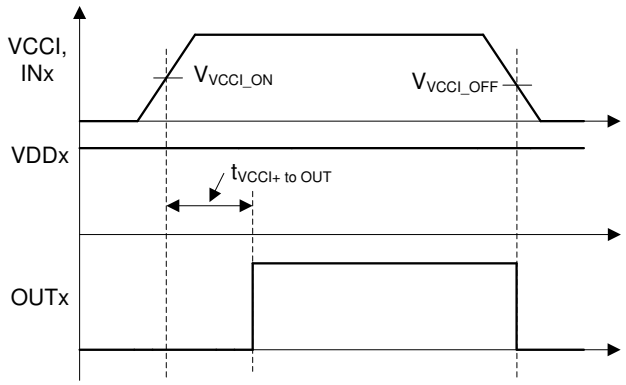



**Figure 7-5. VCCI Power-Up UVLO Delay**

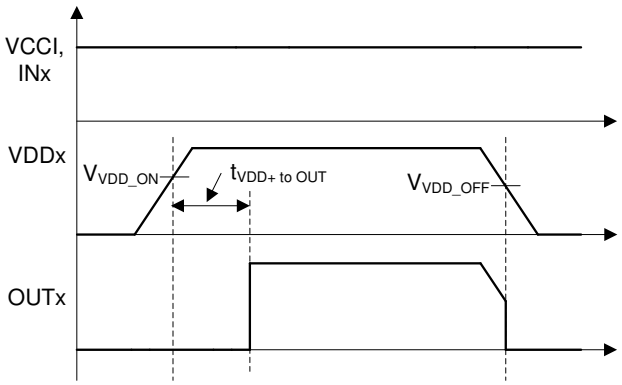



**Figure 7-6. VDDA/B Power-Up UVLO Delay**

## 7.6 CMTI Testing

*Figure 7-7* is a simplified diagram of the CMTI testing configuration.

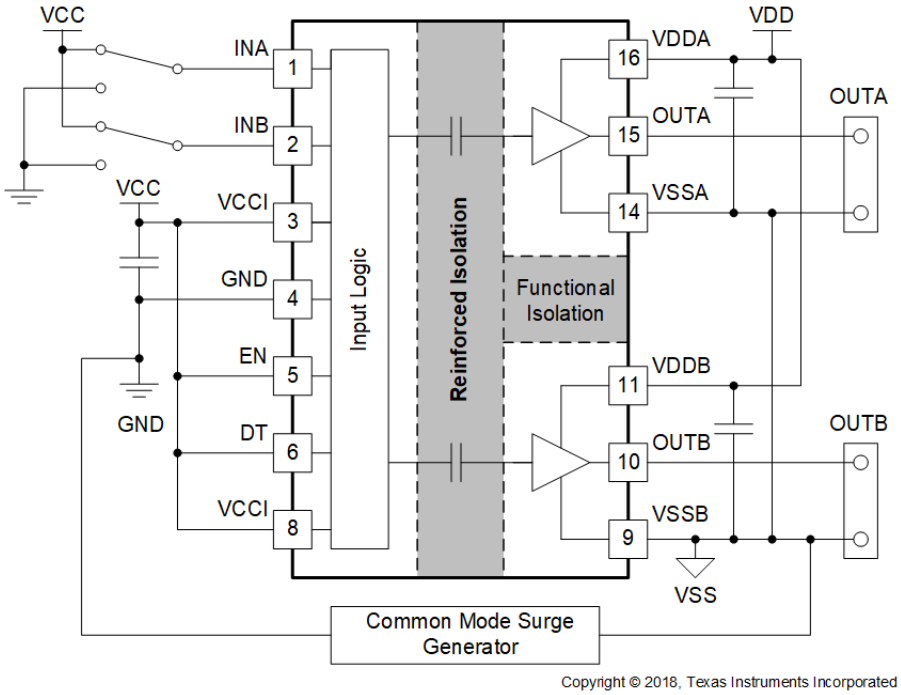



**Figure 7-7. Simplified CMTI Testing Setup**

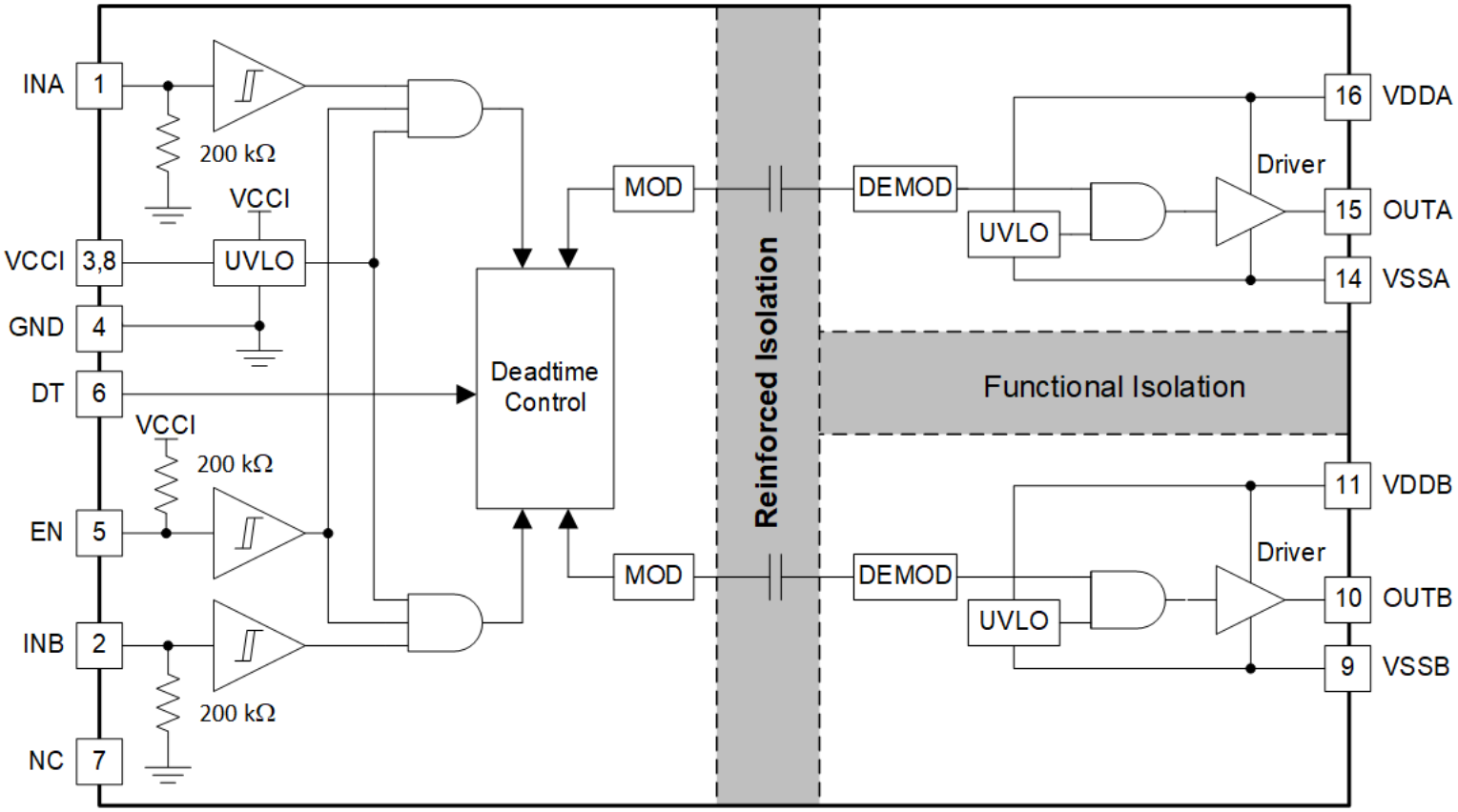
# 8 Detailed Description

## 8.1 Overview

In order to switch power transistors rapidly and reduce switching power losses, high-current gate drivers are often placed between the output of control devices and the gates of power transistors. There are several instances where controllers are not capable of delivering sufficient current to drive the gates of power transistors. This is especially the case with digital controllers, since the input signal from the digital controller is often a 3.3-V logic signal capable of only delivering a few mA.

The UCC21530-Q1 is a flexible dual gate driver which can be configured to fit a variety of power supply and motor drive topologies, as well as drive several types of transistors, including SiC MOSFETs. UCC21530-Q1 has many features that allow it to integrate well with control circuitry and protect the transistors it drives such as: resistor-programmable dead time (DT) control, an EN pin, and under voltage lock out (UVLO) for both input and output voltages. The UCC21530-Q1 also holds its outputs low when the inputs are left open or when the input pulse is not wide enough. The driver inputs are CMOS and TTL compatible for interfacing to digital and analog power controllers alike. Each channel is controlled by its respective input pins (INA and INB), allowing full and independent control of each of the outputs.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 VDD, VCCI, and Under Voltage Lock Out (UVLO)

The UCC21530-Q1 has an internal under voltage lock out (UVLO) protection feature on the supply circuit blocks between the VDD and VSS pins for both outputs. When the VDD bias voltage is lower than $V_{VDD\_ON}$ at device start-up or lower than $V_{VDD\_OFF}$ after start-up, the VDD UVLO feature holds the effected output low, regardless of the status of the input pins (INA and INB).

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs (Illustrated in *Figure 8-1*). In this condition, the upper PMOS is resistively held off by $R_{Hi-Z}$ while the lower NMOS gate is tied to the driver output through $R_{CLAMP}$. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, typically less than 1.5V, when no bias power is available.

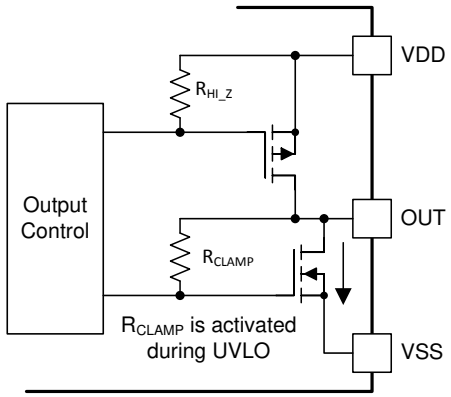



**Figure 8-1. Simplified Representation of Active Pull Down Feature**

The VDD UVLO protection has a hysteresis feature ($V_{VDD\_HYS}$). This hysteresis prevents chatter when there is ground noise from the power supply. Also this allows the device to accept small drops in bias voltage, which is bound to happen when the device starts switching and operating current consumption increases suddenly.

The input side of the UCC21530-Q1 also has an internal under voltage lock out (UVLO) protection feature. The device isn't active unless the voltage, VCCI, is going to exceed $V_{VCCI\_ON}$ on start up. The signal will cease to be delivered once the pin receives a voltage less than $V_{VCCI\_OFF}$. In the same way as the VDD UVLO, there is hysteresis ($V_{VCCI\_HYS}$) to ensure stable operation.

UCC21530-Q1 can withstand an absolute maximum of 30 V for VDD, and 20 V for VCCI.

**Table 8-1. UCC21530-Q1 VCCI UVLO Feature Logic**

| CONDITION | INPUTS | | OUTPUTS | |
|---|---|---|---|---|
| | INA | INB | OUTA | OUTB |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | H | L | L | L |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | L | H | L | L |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | H | H | L | L |
| VCCI-GND < $V_{VCCI\_ON}$ during device start up | L | L | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | H | L | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | L | H | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | H | H | L | L |
| VCCI-GND < $V_{VCCI\_OFF}$ after device start up | L | L | L | L |

**Table 8-2. UCC21530-Q1 VDD UVLO Feature Logic**

| CONDITION | INPUT: INx | OUTPUT: OUTx |
|---|---|---|
| VDDx-VSSx < $V_{VDD\_ON}$ during device start up | L | L |
| VDDx-VSSx < $V_{VDD\_ON}$ during device start up | H | L |

**Table 8-2. UCC21530-Q1 VDD UVLO Feature Logic (continued)**

| CONDITION | INPUT: INx | OUTPUT: OUTx |
|---|---|---|
| VDDx-VSSx < $V_{VDD\_OFF}$ after device start up | L | L |
| VDDx-VSSx < $V_{VDD\_OFF}$ after device start up | H | L |

### 8.3.2 Input and Output Logic Table

**Table 8-3. INPUT/OUTPUT Logic Table(1)**

Assume VCCI, VDDA, VDDB are powered up. See *Section 8.3.1* for more information on UVLO operation modes.

| INPUTS | | EN | OUTPUTS | | NOTE |
|---|---|---|---|---|---|
| INA | INB | | OUTA | OUTB | |
| L | L | H or Left Open | L | L | If Dead Time function is used, output transitions occur after the dead time expires. See Section 8.4.2 |
| L | H | H or Left Open | L | H | |
| H | L | H or Left Open | H | L | |
| H | H | H or Left Open | L | L | DT is left open or programmed with $R_{DT}$ |
| H | H | H or Left Open | H | H | DT pin pulled to VCCI |
| Left Open | Left Open | H or Left Open | L | L | - |
| X | X | L | L | L | Bypass using a ≥ 1-nF low ESR/ESL capacitor close to EN pin when connecting to a µC with distance |

(1) "X" means L, H or left open.

### 8.3.3 Input Stage

The input signal pins (INA and INB) of UCC21530-Q1 are based on a TTL and CMOS compatible input-threshold logic that is totally isolated from the VDD supply voltage. The input pins are easy to drive with logic-level control signals (Such as those from 3.3-V micro-controllers), since UCC21530-Q1 has a typical high threshold ($V_{INA/BH}$) of 1.8 V and a typical low threshold of 1 V, which vary little with temperature (see *Figure 6-22*,*Figure 6-23*). A wide hysterisis ($V_{INA/B\_HYS}$) of 0.8 V makes for good noise immunity and stable operation. If any of the inputs are ever left open, internal pull-down resistors force the pin low. These resistors are typically 200 kΩ (See *Section 8.2*). However, it is still recommended to ground an input if it is not being used.

Since the input side of UCC21530-Q1 is isolated from the output drivers, the input signal amplitude can be larger or smaller than VDD, provided that it doesn't exceed the recommended limit. This allows greater flexibility when integrating with control signal sources, and allows the user to choose the most efficient VDD for their chosen gate. That said, the amplitude of any signal applied to INA or INB must *never* be at a voltage higher than VCCI.

### 8.3.4 Output Stage

The UCC21530-Q1's output stages features a pull-up structure which delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power-switch turn on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional *Pull-Up* N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turn on. This is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET ($R_{NMOS}$) is approximately 1.47 Ω when activated.

The $R_{OH}$ parameter is a DC measurement and it is representative of the on-resistance of the P-channel device only. This is because the *Pull-Up* N-channel device is held in the off state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore the effective resistance of the UCC21530-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the $R_{OH}$ parameter.

The pull-down structure in UCC21530-Q1 is simply composed of an N-channel MOSFET. The $R_{OL}$ parameter, which is also a DC measurement, is representative of the impedance of the pull-down state in the device. Both outputs of the UCC21530-Q1 are capable of delivering 4-A peak source and 6-A peak sink current pulses. The output voltage swings between VDD and VSS provides rail-to-rail operation, thanks to the MOS-out stage which delivers very low drop-out.

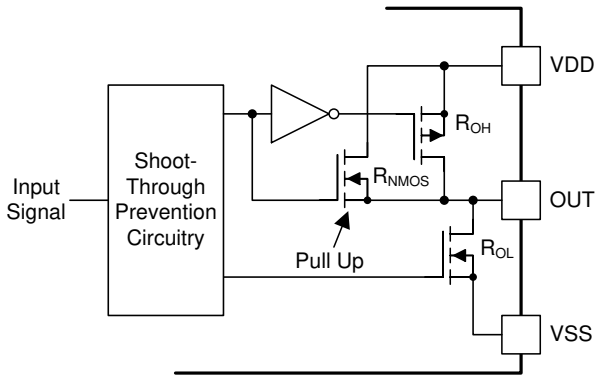



**Figure 8-2. Output Stage**

### 8.3.5 Diode Structure in UCC21530-Q1

*Figure 8-3* illustrates the multiple diodes involved in the ESD protection components of the UCC21530-Q1. This provides a pictorial representation of the absolute maximum rating for the device.

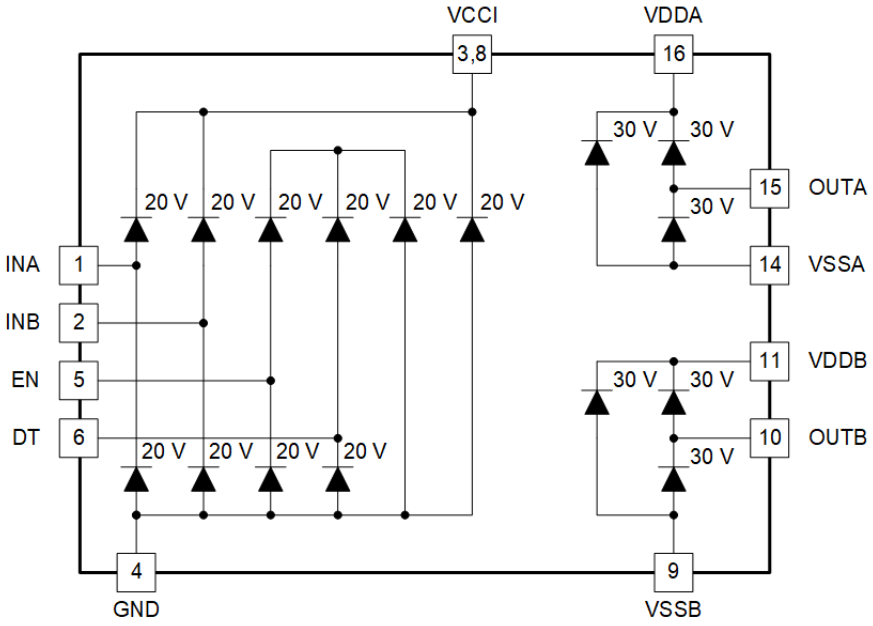



**Figure 8-3. ESD Structure**

## 8.4 Device Functional Modes

### 8.4.1 Enable Pin

Setting the EN pin low, i.e. $V_{EN}$≤0.8V, shuts down both outputs simultaneously. Pull the EN pin high (or left open), i.e. $V_{EN}$≥2.0V, allows UCC21530-Q1 to operate normally. The EN pin is quite responsive, as far as propagation delay and other switching parameters are concerned, the delay between EN are OUTA and OUTB is about 40ns. The EN pin is only functional (and necessary) when VCCI stays above the UVLO threshold. It is highly recommended to tie EN to VCCI directly to achieve better noise immunity.

### 8.4.2 Programmable Dead Time (DT) Pin

UCC21530-Q1 allows the user to adjust dead time (DT) in the following ways:

#### *8.4.2.1 DT Pin Tied to VCC*

Outputs completely match inputs, so no minimum dead time is asserted. This allows outputs to overlap. It is recommended to connect this pin to VCCI directly if it is not used to achieve better noise immunity.

#### *8.4.2.2 DT Pin Connected to a Programming Resistor between DT and GND Pins*

Program $t_{DT}$ by placing a resistor, $R_{DT}$, between the DT pin and GND. TI recommends bypassing this pin with a ceramic capacitor, 2.2 nF or greater, close to DT pin to achieve better noise immunity. The appropriate $R_{DT}$ value can be determined from:

$$t_{DT} \approx 10 \times R_{DT} \quad (1)$$

where

- $t_{DT}$ is the programmed dead time, in nanoseconds.
- $R_{DT}$ is the value of resistance between DT pin and GND, in kilo-ohms.

The steady state voltage at the DT pin is about 0.8 V. $R_{DT}$ programs a small current at this pin, which sets the dead time. As the value of $R_{DT}$ increases, the current sourced by the DT pin decreases. The DT pin current will

be less than 10 µA when $R_{DT}$ = 100 kΩ. For larger values of $R_{DT}$, TI recommends placing $R_{DT}$ and a ceramic capacitor, 2.2 nF or greater, as close to the DT pin as possible to achieve greater noise immunity and better dead time matching between both channels.

The falling edge of an input signal initiates the programmed dead time for the other signal. The programmed dead time is the minimum enforced duration in which both outputs are held low by the driver. The outputs may also be held low for a duration greater than the programmed dead time, if the INA and INB signals include a dead time duration greater than the programmed minimum. If both inputs are high simultaneously, both outputs will immediately be set low. This feature is used to prevent shoot-through in half-bridge applications, and it does not affect the programmed dead time setting for normal operation. Various driver dead time logic operating conditions are illustrated and explained in .

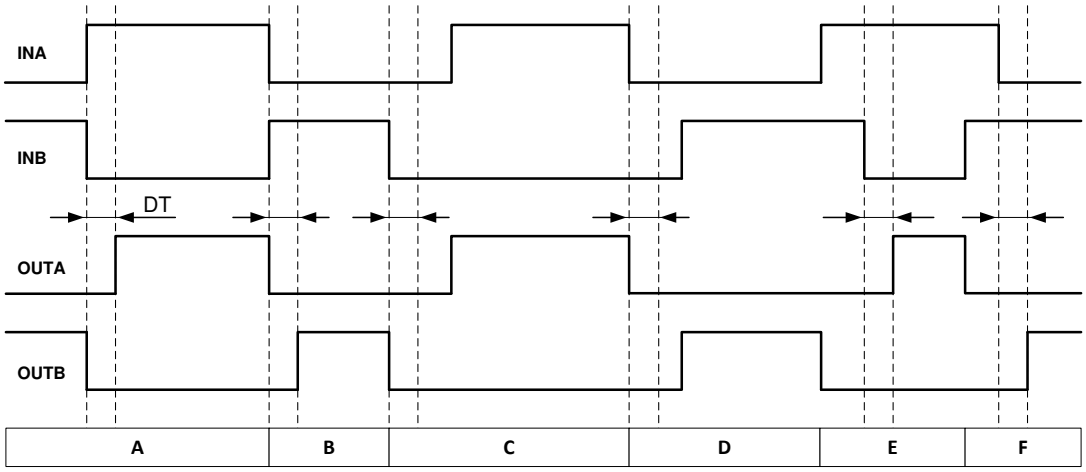



**Figure 8-4. Input and Output Logic Relationship With Input Signals**

**Condition A:** INB goes low, INA goes high. INB sets OUTB low immediately and assigns the programmed dead time to OUTA. OUTA is allowed to go high after the programmed dead time.

**Condition B:** INB goes high, INA goes low. Now INA sets OUTA low immediately and assigns the programmed dead time to OUTB. OUTB is allowed to go high after the programmed dead time.

**Condition C:** INB goes low, INA is still low. INB sets OUTB low immediately and assigns the programmed dead time for OUTA. In this case, the input signal's *own* dead time is longer than the programmed dead time. Thus, when INA goes high, it immediately sets OUTA high.

**Condition D:** INA goes low, INB is still low. INA sets OUTA low immediately and assigns the programmed dead time to OUTB. INB's *own* dead time is longer than the programmed dead time. Thus, when INB goes high, it immediately sets OUTB high.

**Condition E:** INA goes high, while INB and OUTB are still high. To avoid overshoot, INA immediately pulls OUTB low and keeps OUTA low. After some time OUTB goes low and assigns the programmed dead time to OUTA. OUTB is already low. After the programmed dead time, OUTA is allowed to go high.

**Condition F:** INB goes high, while INA and OUTA are still high. To avoid overshoot, INB immediately pulls OUTA low and keeps OUTB low. After some time OUTA goes low and assigns the programmed dead time to OUTB. OUTA is already low. After the programmed dead time, OUTB is allowed to go high.

# Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The UCC21530-Q1 effectively combines both isolation and buffer-drive functions. The flexible, universal capability of the UCC21530-Q1 (with up to 18-V VCCI and 25-V VDDA/VDDB) allows the device to be used as a low-side, high-side, high-side/low-side or half-bridge driver for MOSFETs, IGBTs or SiC MOSFETs. With integrated components, advanced protection features (UVLO, dead time, and enable) and optimized switching performance; the UCC21530-Q1 enables designers to build smaller, more robust designs for enterprise, telecom, automotive, and industrial applications with a faster time to market.

## 9.2 Typical Application

The circuit in *Figure 9-1* shows a reference design with UCC21530-Q1 driving a typical half-bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half-bridge/full bridge isolated topologies, and 3-phase motor drive applications. This circuit uses two supplies (or single-input-double-output power supply). Power supply $V_{A+}$ determines the positive drive output voltage and $V_{A-}$ determines the negative turn-off voltage. The configuration for channel B is the same as channel A.

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. This solution has two separate power supplies for each driver channel, so it provides flexibility when setting the positive and negative rail voltages.

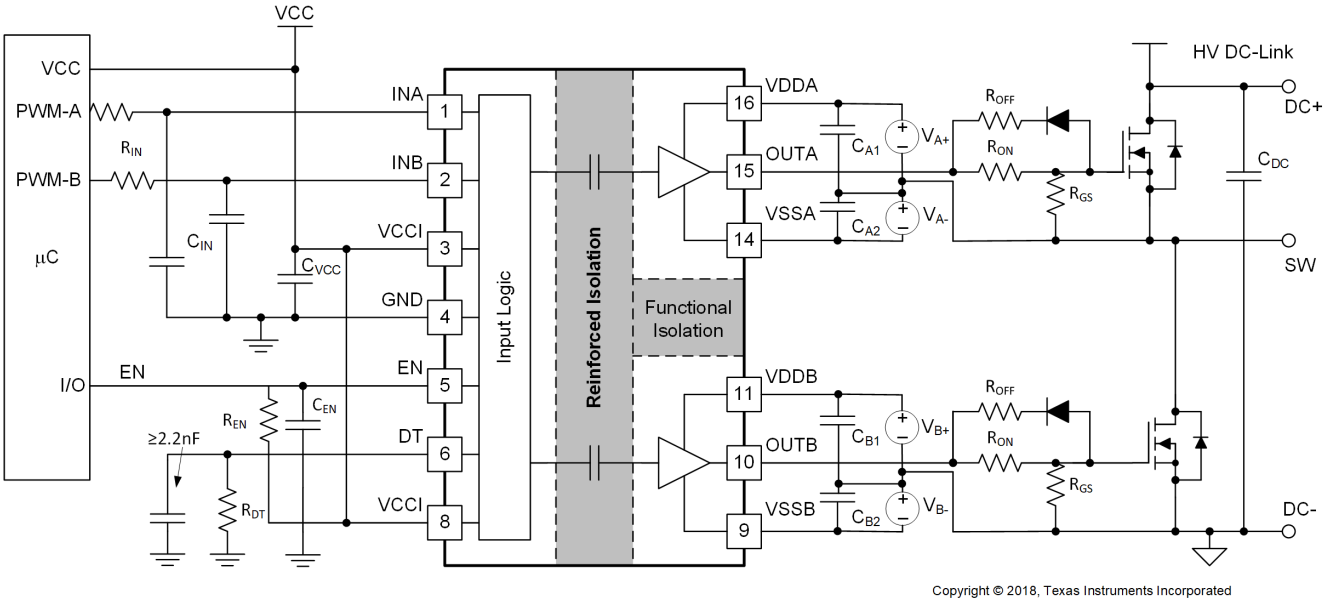



**Figure 9-1. Typical Application Schematic with Dual Power Supplies**

### 9.2.1 Design Requirements

*Table 9-1* lists reference design parameters for the example application: UCC21530-Q1 driving 1000-V SiC-MOSFETs in a high side-low side configuration.

**Table 9-1. UCC21530-Q1 Design Requirements**

| PARAMETER | VALUE | UNITS |
|---|---|---|
| Power transistor | C3M0065100K | – |
| VCC | 5.0 | V |
| VDD | 15 | V |
| VSS | –4 | V |
| $R_{ON}$ | 2.2 | Ω |
| $R_{OFF}$ | 0 | Ω |
| Input signal amplitude | 3.3 | V |
| Switching frequency ($f_s$) | 100 | kHz |
| DC link voltage | 600 | V |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Designing INA/INB Input Filter*

It is recommended that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input $R_{IN}$-$C_{IN}$ filter can be used to filter out the ringing introduced by non-ideal layout or long PCB traces.

Such a filter should use an $R_{IN}$ in the range of 0 Ω to 100 Ω and a $C_{IN}$ between 10 pF and 100 pF. In the example, an $R_{IN}$ = 51 Ω and a $C_{IN}$ = 33 pF are selected, with a corner frequency of approximately 100 MHz.

When selecting these components, it is important to pay attention to the trade-off between good noise immunity and propagation delay.

#### *9.2.2.2 Select Dead Time Resistor and Capacitor*

From *Equation 1*, a 10-kΩ resistor is selected to set the dead time to 100 ns. A 2.2-nF capacitor is placed in parallel close to the DT pin to improve noise immunity.

#### *9.2.2.3 Gate Driver Output Resistor*

The external gate driver resistors, $R_{ON}$/$R_{OFF}$, are used to:

1. Limit ringing caused by parasitic inductances/capacitances.
2. Limit ringing caused by high voltage/current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, i.e. peak sink and source current to optimize the switching loss.
4. Reduce electromagnetic interference (EMI).

As mentioned in *Section 8.3.4*, the UCC21530-Q1 has a pull-up structure with a P-channel MOSFET and an additional *pull-up* N-channel MOSFET in parallel. The combined peak source current is 4 A. Therefore, the peak source current can be predicted with:

$$I_{O+} = \min\left(4A, \frac{V_{DD} - V_{SS}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right) \quad (2)$$

where

- $R_{ON}$: External turn-on resistance,$R_{ON}$=2.2 Ω in this example;.
- $R_{GFET\_INT}$: Power transistor internal gate resistance, found in the power transistor datasheet.
- $I_{O+}$ = Peak source current – The minimum value between 4 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

In this example:

$$I_{O+} = \frac{V_{DD} - V_{SS}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{15V - (-4V)}{1.47\Omega \,||\, 5\Omega + 2.2\Omega + 4.7\Omega} \approx 2.4A \quad (3)$$

Therefore, the driver peak source current is 2.4 A for each channel. Similarly, the peak sink current can be calculated with:

$$I_{O-} = \min\left(6A, \frac{V_{DD} - V_{SS} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}}\right) \quad (4)$$

where

- $R_{OFF}$: External turn-off resistance, $R_{OFF}$=0 in this example;
- $V_{GDF}$: The anti-parallel diode forward voltage drop which is in series with $R_{OFF}$. The diode in this example is an MSS1P4.
- $I_{O-}$: Peak sink current – the minimum value between 6 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

In this example,

$$I_{O-} = \frac{V_{DD} - V_{SS} - V_{GDF}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} = \frac{15V - (-4V) - 0.75V}{0.55\Omega + 0\Omega + 4.7\Omega} \approx 3.5A \quad (5)$$

Therefore, the driver peak sink current is 3.5 A for each channel.

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, it is strongly recommended that the gate driver loop should be minimized. On the other hand, the peak source/sink current is dominated by loop parasitics when the load capacitance ($C_{ISS}$) of the power transistor is very small (typically less than 1 nF), because the rising and falling time is too small and close to the parasitic ringing period.

#### *9.2.2.4 Estimate Gate Driver Power Loss*

The total loss, $P_G$, in the gate driver subsystem includes the power losses of the UCC21530-Q1 ($P_{GD}$) and the power losses in the peripheral circuitry, such as the external gate drive resistor. Bootstrap diode loss is not included in $P_G$ and not discussed in this section.

$P_{GD}$ is the key power loss which determines the thermal safety-related limits of the UCC21530-Q1, and it can be estimated by calculating losses from several components.

The first component is the static power loss, $P_{GDQ}$, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. $P_{GDQ}$ is measured on the bench with no load connected to OUTA and OUTB at a given VCCI, VDDA/VDDB, switching frequency and ambient temperature. *Figure 6-4* shows the per output channel current consumption vs. operating frequency with no load. In this example, $V_{VCCI}$ = 5 V and $V_{VDD}$-$V_{VSS}$ = 19 V. The current on each power supply, with INA/INB switching from 0 V to 3.3 V at 100 kHz is measured to be $I_{VCCI} \approx 2.5$ mA, and $I_{VDDA} = I_{VDDB} \approx 1.5$ mA. Therefore, the $P_{GDQ}$ can be calculated with

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + (V_{VDDA} - V_{VSSA}) \times I_{DDA} + (V_{VDDB} - V_{VSSB}) \times I_{DDB} \approx 70mW \quad (6)$$

The second component is switching operation loss, $P_{GDO}$, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Total dynamic loss due to load switching, $P_{GSW}$, can be estimated with

$$P_{GSW} = 2 \times (V_{DD} - V_{SS}) \times Q_G \times f_{SW} \quad (7)$$

where

- $Q_G$ is the gate charge of the power transistor.

If a split rail is used to turn on and turn off, then VDD is going to be equal to difference between the positive rail to the negative rail.

So, for this example application:

$$P_{GSW} = 2 \times 19V \times 35nC \times 100kHz = 133mW \quad (8)$$

$Q_G$ represents the total gate charge of the power transistor switching 600 V at 20 A, and is subject to change with different testing conditions. The UCC21530-Q1 gate driver loss on the output stage, $P_{GDO}$, is part of $P_{GSW}$. $P_{GDO}$ will be equal to $P_{GSW}$ if the external gate driver resistances are zero, and all the gate driver loss is dissipated inside the UCC21530-Q1. If there are external turn-on and turn-off resistances, the total loss will be distributed between the gate driver pull-up/down resistances and external gate resistances. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 4 A/6 A, however, it will be non-linear if the source/sink current is saturated. Therefore, $P_{GDO}$ is different in these two scenarios.

**Case 1 - Linear Pull-Up/Down Resistor:**

$$P_{GDO} = P_{GSW} \times \left( \frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} \,||\, R_{ON} + R_{GFET\_Int}} \right) \quad (9)$$

In this design example, all the predicted source/sink currents are less than 4 A/6 A, therefore, the UCC21530-Q1 gate driver loss can be estimated with:

$$P_{GDO} = 133mW \times \left( \frac{5\Omega \,||\, 1.47\Omega}{5\Omega \,||\, 1.47\Omega + 2.2\Omega + 4.7\Omega} + \frac{0.55\Omega}{0.55\Omega + 0\Omega + 4.7\Omega} \right) \approx 33mW \quad (10)$$

**Case 2 - Nonlinear Pull-Up/Down Resistor:**

$$P_{GDO} = 2 \times f_{SW} \times \left[ 4A \times \int_0^{T_{R\_Sys}} \left( V_{DD} - V_{OUTA/B}(t) \right) dt + 6A \times \int_0^{T_{F\_Sys}} \left( V_{OUTA/B}(t) - V_{SS} \right) dt \right] \quad (11)$$

where

- $V_{OUTA/B}(t)$ is the gate driver OUTA and OUTB pin voltage during the turn on and off transient, and it can be simplified that a constant current source (4 A at turn-on and 6 A at turn-off) is charging/discharging a load capacitor. Then, the $V_{OUTA/B}(t)$ waveform will be linear and the $T_{R\_Sys}$ and $T_{F\_Sys}$ can be easily predicted.

For some scenarios, if only one of the pull-up or pull-down circuits is saturated and another one is not, the $P_{GDO}$ will be a combination of Case 1 and Case 2, and the equations can be easily identified for the pull-up and pull-down based on the above discussion. Therefore, total gate driver loss dissipated in the gate driver UCC21530-Q1, $P_{GD}$, is:

$$P_{GD} = P_{GDQ} + P_{GDO} \quad (12)$$

which is equal to 103 mW in the design example.

#### 9.2.2.5 Estimating Junction Temperature

The junction temperature of the UCC21530-Q1 can be estimated with:

$$T_J = T_C + \Psi_{JT} \times P_{GD} \tag{13}$$

where

- $T_J$ is the junction temperature.
- $T_C$ is the UCC21530-Q1 case-top temperature measured with a thermocouple or some other instrument.
- $\psi_{JT}$ is the junction-to-top characterization parameter from the *Section 6.4* table.

Using the junction-to-top characterization parameter ($\Psi_{JT}$) instead of the junction-to-case thermal resistance ($R_{\Theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). $R_{\Theta JC}$ can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heatsink is applied to an IC package. In all other cases, use of $R_{\Theta JC}$ will inaccurately estimate the true junction temperature. $\Psi_{JT}$ is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimates can be made accurately to within a few degrees Celsius. For more information, see the Section 9.1 and Semiconductor and IC Package Thermal Metrics application report.

#### 9.2.2.6 Selecting VCCI, VDDA/B Capacitor

Bypass capacitors for VCCI, VDDA, and VDDB are essential for achieving reliable performance. It is recommended that one choose low ESR and low ESL surface-mount multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients and capacitance tolerances. Importantly, DC bias on an MLCC will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15 $V_{DC}$ is applied.

##### 9.2.2.6.1 Selecting a VCCI Capacitor

A bypass capacitor connected to VCCI supports the transient current needed for the primary logic and the total current consumption, which is only a few mA. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power supply output is a relatively long distance from the VCCI pin, a tantalum or electrolytic capacitor, with a value over 1 µF, should be placed in parallel with the MLCC.

### 9.2.2.7 Other Application Example Circuits

When parasitic inductances are introduced by non-ideal PCB layout and long package leads (e.g. TO-220 and TO-247 type packages), there could be ringing in the gate-source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn-on and even shoot-through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Below are a few examples of implementing negative gate drive bias.

Instead of using two separate power for generating positive and negative drive voltage *Figure 9-2* shows the example with negative bias turn-off on the channel-A driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, $V_A$, is equal to 19 V, the turn-off voltage will be –3.9 V and turn-on voltage will be 19 V – 3.9 V ≈ 15 V. The channel-B driver circuit is the same as channel-A, therefore, this configuration needs only one power supply for each driver channel, and there will be steady state power consumption from $R_Z$.

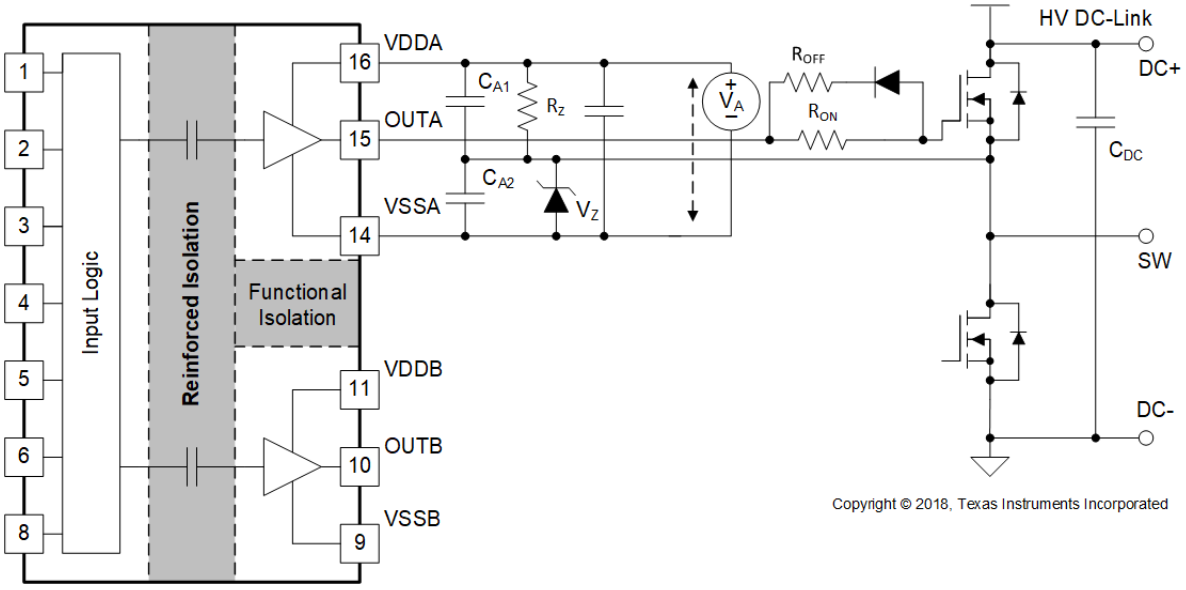



**Figure 9-2. Negative Bias with Zener Diode on Iso-Bias Power Supply Output**

*Figure 9-3* shows another example which uses bootstrap to provide power for the channel A, this solution doesn't have negative rail voltage, it is only suitable for circuits with less ringing or the power device has high threshold voltage.

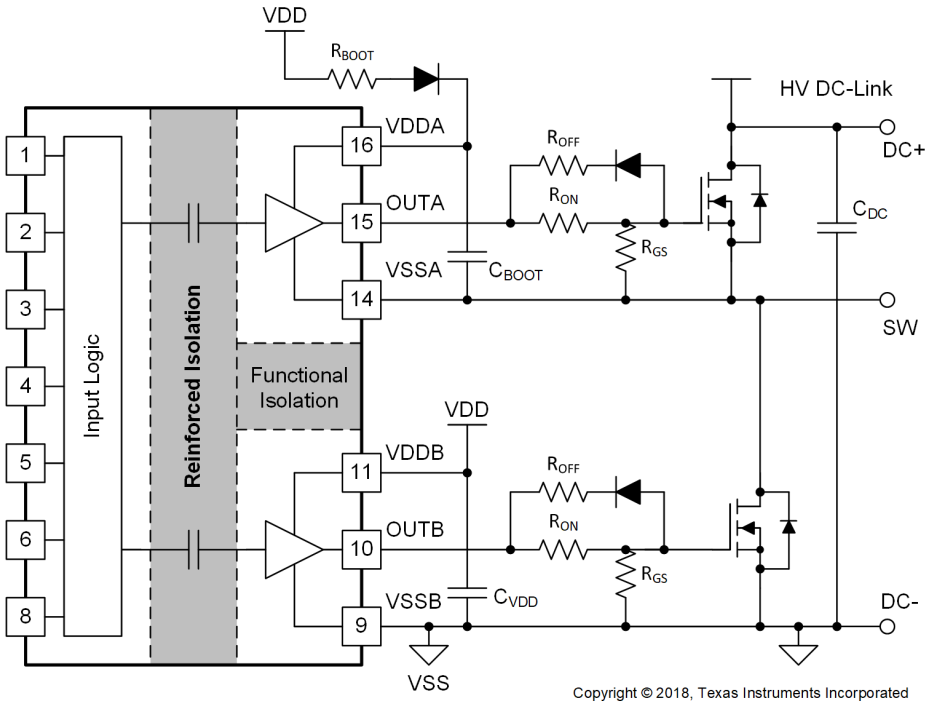



**Figure 9-3. Bootstrap Power Supply for the High Side Device**

The last example, shown in *Figure 9-4*, is a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, this solution has limitations:

1. The negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors which favor this solution.
2. The high side VDDA-VSSA must maintain enough voltage to stay in the recommended power supply range, which means the low side switch must turn-on or have free-wheeling current on the body (or anti-parallel) diode for a certain period during each switching cycle to refresh the bootstrap capacitor. Therefore, a 100% duty cycle for the high side is not possible unless there is a dedicated power supply for the high side, like in the other two example circuits.

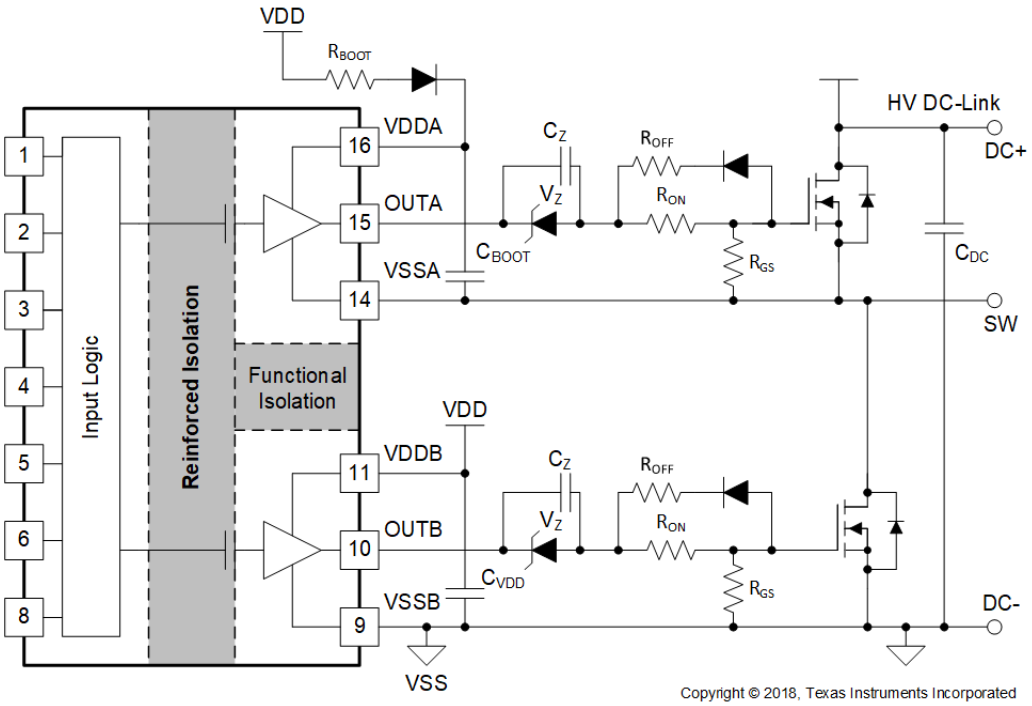



**Figure 9-4. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path**

### 9.2.3 Application Curves

*Figure 9-5*shows a multiple pulses bench test circuit which uses L1 as the inductor load, and a group of control pulses are generated to evaluate driver and SiC MOSFET switching transient under different load conditions. The test conditions are: $V_{DC-Link}$ = 600 V, VCC = 5 V, VDD = 15 V, VSS = –4 V, $f_{SW}$ = 500 kHz, $R_{ON}$ = 5.1 Ω, $R_{OFF}$ = 1.0 Ω. *Figure 9-6* shows the turn on and turn off waveforms at around 20 A current

**Channel 1 (Yellow):** Gate-source voltage signal on the low side MOSFET.

**Channel 2 (Blue):** Gate-source voltage signal on the high side MOSFET.

**Channel 3 (Pink):** Drain-source voltage signal for the low side MOSFET.

**Channel 4 (Green):** Drain-source current signal for the low side MOSFET.

In *Figure 9-6*, the gate drive signals on the high and low power transistor have a 100-ns dead time, and both signals are measured with >= 500 MHz bandwidth probes.

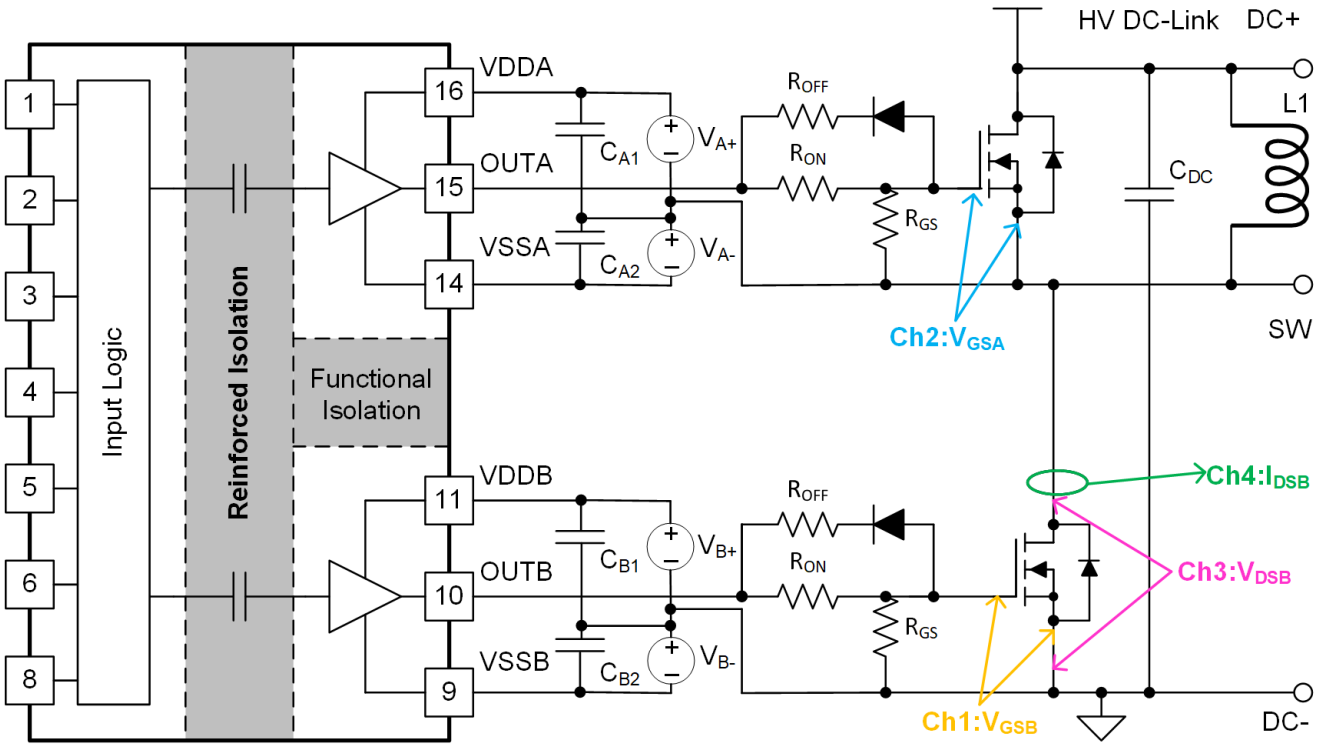



**Figure 9-5. Bench Test Circuit with SiC MOSFET Switching**


**Figure 9-6. SiC MOSFET Switching Waveforms**

## Power Supply Recommendations

The recommended input supply voltage (VCCI) for UCC21530-Q1 is between 3 V and 18 V. The output bias supply voltage (VDDA/VDDB) range depends on which version of UCC21530-Q1 one is using. The lower end of this bias supply range is governed by the internal under voltage lockout (UVLO) protection feature of each device. One mustn't let VDD or VCCI fall below their respective UVLO thresholds (For more information on UVLO see *Section 8.3.1*). The upper end of the VDDA/VDDB range depends on the maximum gate voltage of the power device being driven by UCC21530-Q1. All versions of UCC21530-Q1 have a recommended maximum VDDA/VDDB of 25 V.

A local bypass capacitor should be placed between the VDD and VSS pins. This capacitor should be positioned as close to the device as possible. A low ESR, ceramic surface mount capacitor is recommended. It is further suggested that one place two such capacitors: one with a value of between 220 nF and 10 µF for device biasing, and an additional 100-nF capacitor in parallel for high frequency filtering.

Similarly, a bypass capacitor should also be placed between the VCCI and GND pins. Given the small amount of current drawn by the logic circuitry within the input side of UCC21530-Q1, this bypass capacitor has a minimum recommended value of 100 nF.

# 9 Layout

## 9.1 Layout Guidelines

Consider these PCB layout guidelines for in order to achieve optimum performance for the UCC21530-Q1.

### 9.1.1 Component Placement Considerations

- Low-ESR and low-ESL capacitors must be connected close to the device between the VCCI and GND pins and between the VDD and VSS pins to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the switch node VSSA (HS) pin in bridge configurations, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- To improve noise immunity when driving the EN pin from a distant micro-controller, TI recommends adding a small bypass capacitor, ≥ 1 nF, between the EN pin and GND.
- If the dead time feature is used, TI recommends placing the programming resistor $R_{DT}$ and bypassing capacitor close to the DT pin of the UCC21530-Q1 to prevent noise from unintentionally coupling to the internal dead time circuit. The capacitor should be ≥ 2.2 nF.

### 9.1.2 Grounding Considerations

- It is essential to confine the high peak currents that charge and discharge the transistor gates to a minimal physical area. This will decrease the loop inductance and minimize noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- Pay attention to high current path that includes the bootstrap capacitor, bootstrap diode, local VSSB-referenced bypass capacitor, and the low-side transistor body/anti-parallel diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode by the VDD bypass capacitor. This recharging occurs in a short time interval and involves a high peak current. Minimizing this loop length and area on the circuit board is important for ensuring reliable operation.

### 9.1.3 High-Voltage Considerations

- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout is recommended in order to prevent contamination that may compromise the isolation performance.
- For half-bridge or high-side/low-side configurations, maximize the clearance distance of the PCB layout between the high and low-side PCB traces.

### 9.1.4 Thermal Considerations

- A large amount of power may be dissipated by the UCC21530-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high (refer to *Section 9.2.2.4* for more details). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction to board thermal impedance ($\theta_{JB}$).
- Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB (see *Figure 9-2* and *Figure 9-3*). However, high voltage PCB considerations mentioned above must be maintained.
- If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or copper from different high-voltage planes overlap.

## 9.2 Layout Example

*Figure 9-1*shows a 2-layer PCB layout example with the signals and key components labeled.

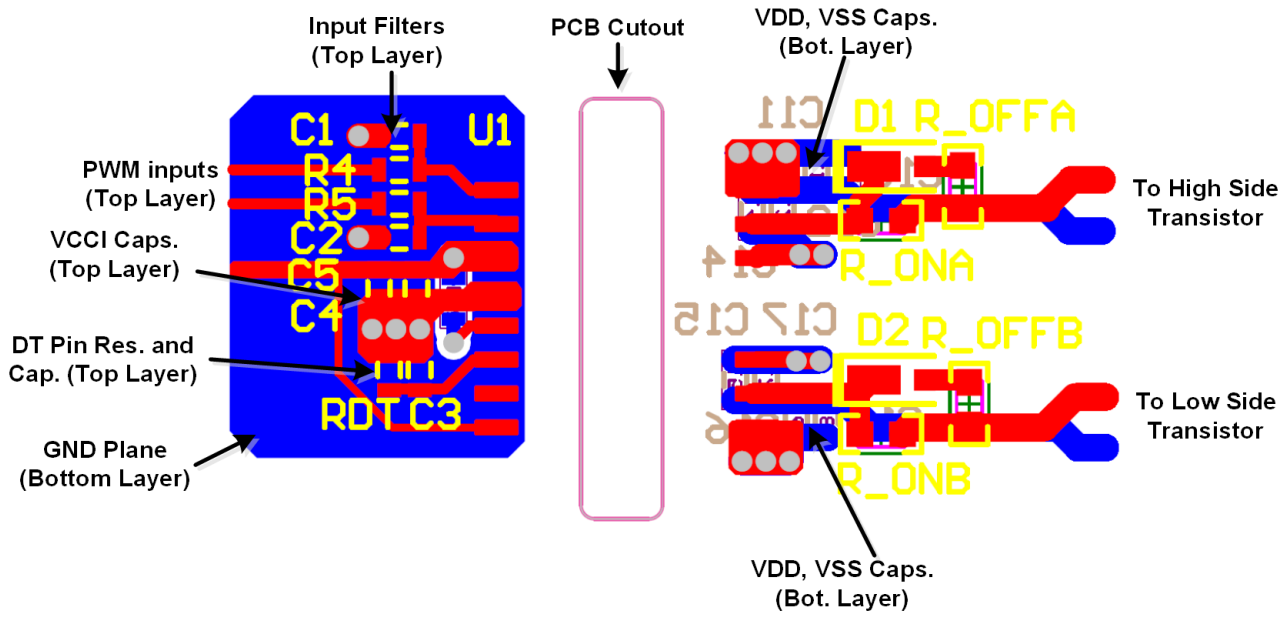



**Figure 9-1. Layout Example**

*Figure 9-2* and *Figure 9-3* shows top and bottom layer traces and copper.

**Note**

There are no PCB traces or copper between the primary and secondary side, which ensures isolation performance.

PCB traces between the high-side and low-side gate drivers in the output stage are increased to maximize the creepage distance for high-voltage operation, which will also minimize cross-talk between the switching node VSSA (SW), where high dv/dt may exist, and the low-side gate drive due to the parasitic capacitance coupling.

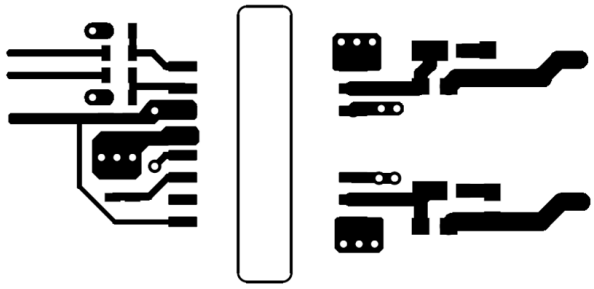


**Figure 9-2. Top Layer Traces and Copper**

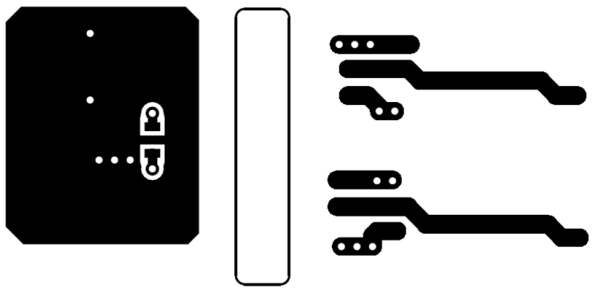


**Figure 9-3. Bottom Layer Traces and Copper**

*Figure 9-4* and *Figure 9-5* are 3D layout pictures with top view and bottom views.

**Note**

The location of the PCB cutout between the primary side and secondary sides, which ensures isolation performance.

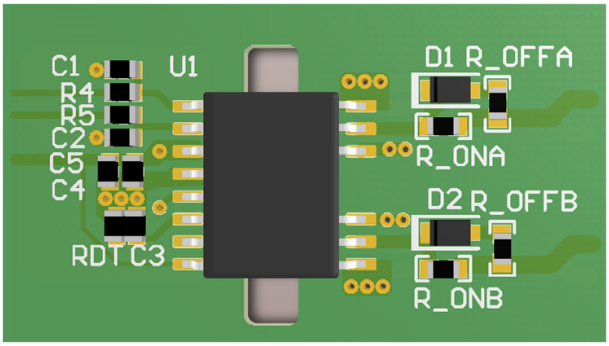



**Figure 9-4. 3-D PCB Top View**

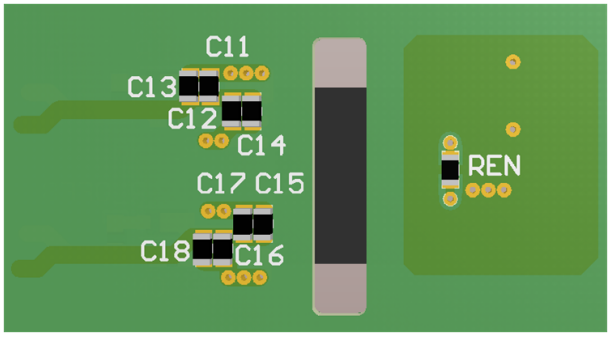



**Figure 9-5. 3-D PCB Bottom View**

# 10 Device and Documentation Support

## 10.1 Documentation Support

### 10.1.1 Related Documentation

For related documentation see the following:

- Isolation Glossary

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Community Resources

## 10.4 Trademarks

All trademarks are the property of their respective owners.

# Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC21530BQDWKQ1 | ACTIVE | SOIC | DWK | 14 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | U21530BQ | Samples |
| UCC21530BQDWKRQ1 | ACTIVE | SOIC | DWK | 14 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | U21530BQ | Samples |
| UCC21530QDWKQ1 | ACTIVE | SOIC | DWK | 14 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21530Q | Samples |
| UCC21530QDWKRQ1 | ACTIVE | SOIC | DWK | 14 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC21530Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF UCC21530-Q1 :**

- Catalog : UCC21530

NOTE: Qualified Version Definitions:

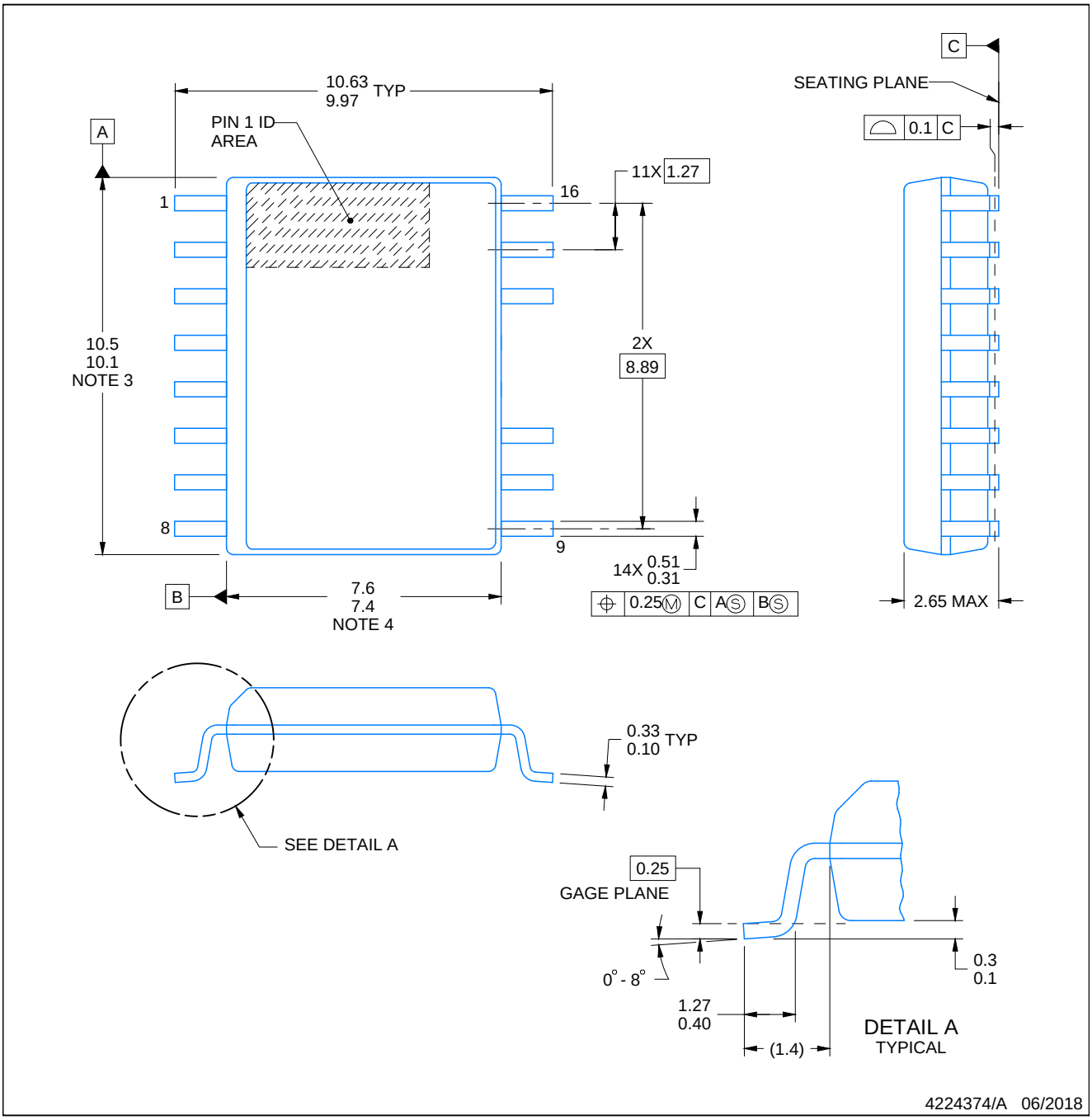
- Catalog - TI's standard catalog product

# PACKAGE OUTLINE

## DWK0014A

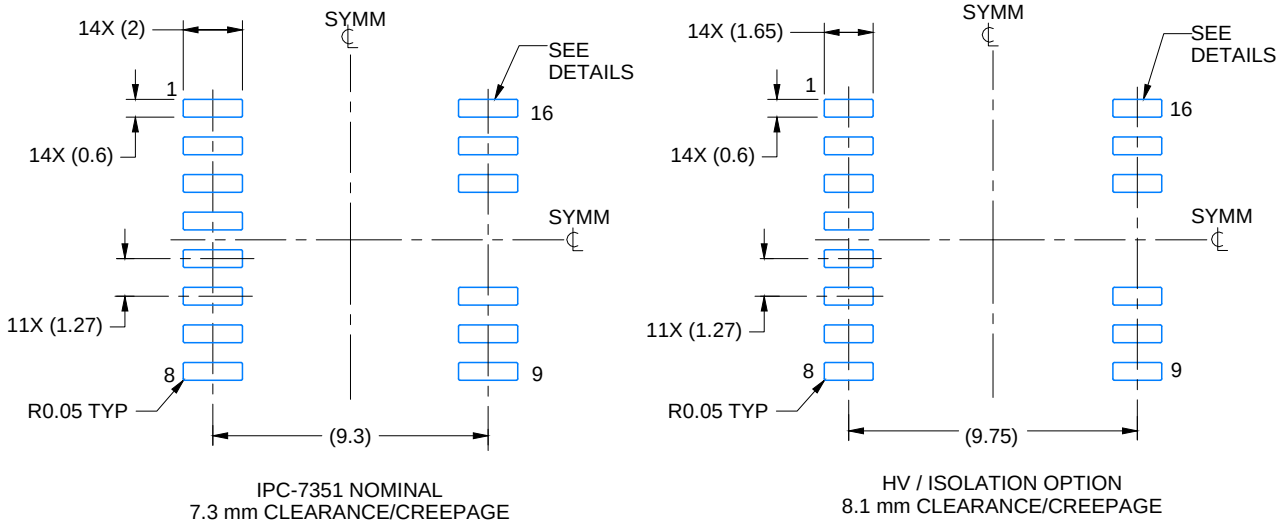
## SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

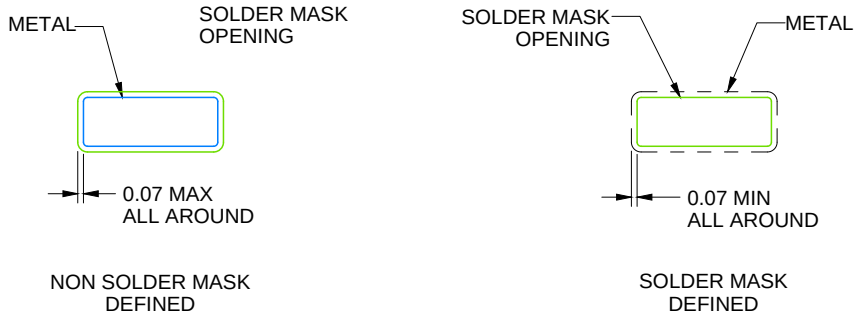



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:4X




SOLDER MASK DETAILS

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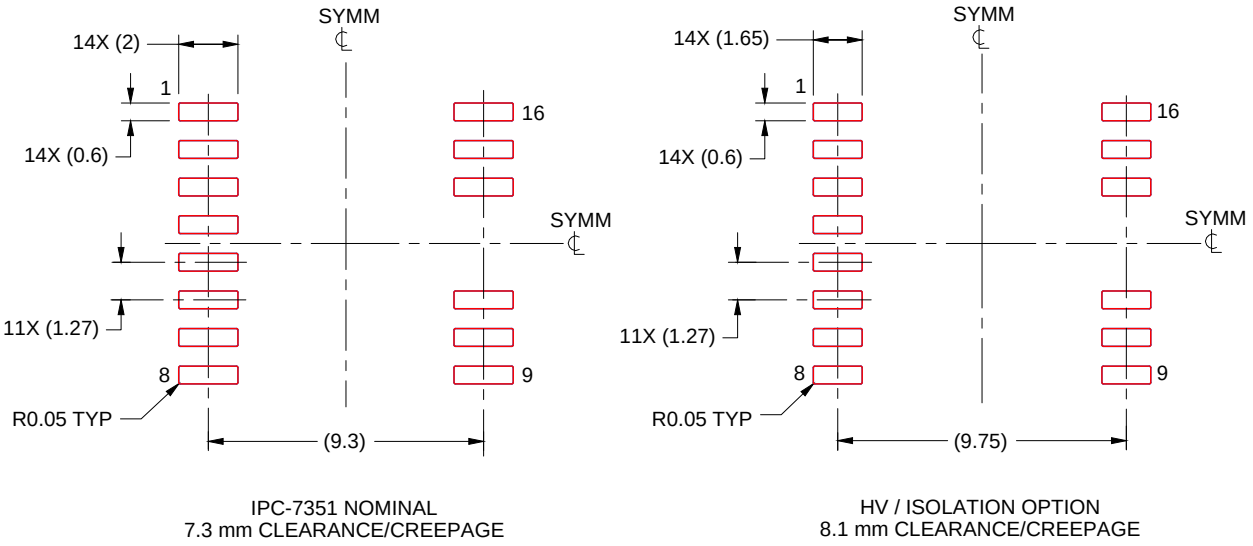
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224374/A 06/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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