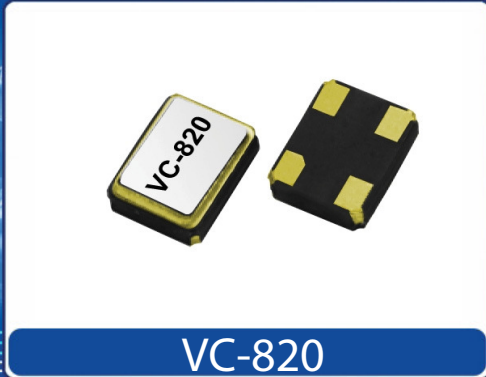



Helping Customers Innovate, Improve & Grow



## Description

Vectron's VC-820 Crystal Oscillator (XO) is a quartz stabilized square wave generator with a CMOS output. The VC-820 uses a fundamental or a 3rd overtone crystal, oscillating in a fundamental tone, resulting in very low jitter performance, and a monolithic IC which improves reliability and reduces cost.

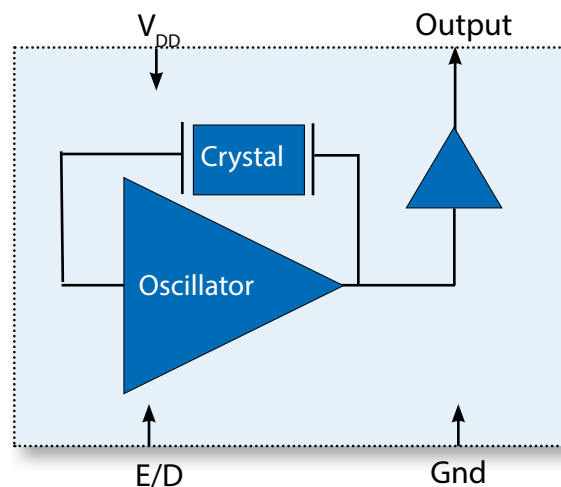
## Features

- CMOS output XO
- Output Frequencies from 625 kHz to 133.000 MHz
- 3.3 V, 2.5 V and 1.8 V Operation
- Low Jitter Performance
- Output Disable Feature
- Operating Temperature ranging from -55°C to 125°C
- Small Industry Standard Package, 3.2x2.5 mm
- Product is compliant to RoHS directive  and fully compatible with lead free assembly

## Applications

- SONET/SDH/DWDM
- Ethernet, GE, SynchE
- Storage Area Networking
- Fiber Channel
- Digital Video
- Broadband Access
- Base Stations, Picocells

## Block Diagram



# Specifications

**Table 1. Electrical Performance, 3.3V Option**

Parameter	Symbol	Min	Typical	Max	Units
<b>Supply Voltage</b>					
Voltage <sup>1</sup>	$V_{DD}$	3.15	3.3	3.45	V
Maximum Voltage		-0.5		5	V
Current <sup>2</sup> ≤20.000MHz 20.000 to 39.999MHz 40.000 to 49.999MHz 50.000 to 79.999MHz 80.000 to 99.999MHz 100.000 to 133.000MHz	$I_{DD}$			6 7 8 9 10 40	mA
Current, Output Disabled				5	uA
<b>Frequency</b>					
Nominal Frequency <sup>3</sup>	$f_N$	0.625		133.000	MHz
Stability <sup>4,8</sup> (Ordering Option)		±20, ±25, ±50, ±100			ppm
<b>Outputs</b>					
Output Logic Levels <sup>2</sup> , <40MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	0.9* $V_{DD}$  4 4		0.1* $V_{DD}$	V V mA mA
Output Logic Levels <sup>2</sup> , 40-99.99MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	$V_{DD}$ -0.4  4 4		0.4	V V mA mA
Output Logic Levels <sup>2</sup> , 100-133.000MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	2.3  8 8		0.4	V V mA mA
Load	$I_{OUT}$			15	pF
Output Rise /Fall Time <sup>2</sup>	$t_R/t_F$			4	ns
Duty Cycle <sup>2,5</sup>		45	50	55	%
Period Jitter <sup>6</sup> RMS Peak-Peak Random Jitter Deterministic Jitter	$\phi_J$		2.4 20.2 2.4 0		ps
RMS Jitter, 12k-20MHz, 125MHz	$\phi_J$		0.06	0.3	ps
<b>Enable/Disable</b>					
Output Enable/Disable <sup>7</sup> Output Enable Output Disable	$V_{IH}$ $V_{IL}$	0.7* $V_{DD}$		0.3* $V_{DD}$	V V
Disable time	$t_D$			150	ns
Start-Up Time	$t_{SU}$			5	ms
Operating Temp (Ordering Option)	$T_{OP}$	-10/70, -40/85, -40/105, -40/125, -55/105, -55/125			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.

2] Parameters are tested with the test circuit shown Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.

5] Duty Cycle is measured as On Time/Period, see Fig 2.

6] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.

7] The Output is Enabled if the Enable/Disable is left open.

8] Only ±50 and ±100ppm stability options are available for -40/105 °C, -40/125 °C, -55/105 °C and -55/125 °C temperature range.

# Specifications

**Table 2. Electrical Performance, 2.5V Option**

Parameter	Symbol	Min	Typical	Max	Units
<b>Supply Voltage</b>					
Voltage <sup>1</sup>	$V_{DD}$	2.375	2.5	2.625	V
Maximum Voltage		-0.5		5	V
Current <sup>2</sup> ≤20.000MHz 20.000 to 39.999MHz 40.000 to 79.999MHz 80.000 to 99.999MHz 100.000 to 125.000MHz	$I_{DD}$			4.5 5.5 7 7.5 30	mA
Current, Output Disabled				5	uA
<b>Frequency</b>					
Nominal Frequency <sup>3</sup>	$f_N$	0.625		125.000	MHz
Stability <sup>4,8</sup> (Ordering Option)		±20, ±25, ±50, ±100			ppm
<b>Outputs</b>					
Output Logic Levels <sup>2,3</sup> , <40MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	$0.9 \cdot V_{DD}$  4 4		$0.1 \cdot V_{DD}$	V V mA mA
Output Logic Levels <sup>2</sup> , 40-99.99MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	$V_{DD}-0.4$  4 4		0.4	V V mA mA
Output Logic Levels <sup>2</sup> , 100-125.000MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	1.65  8 8		0.4	V V mA mA
Load	$I_{OUT}$			15	pF
Output Rise /Fall Time <sup>2</sup>	$t_R/t_F$			4	ns
Duty Cycle <sup>2,5</sup>		45	50	55	%
Period Jitter <sup>6</sup> , 125.000MHz RMS Peak-Peak Random Jitter Deterministic Jitter	$\phi J$		2.4 20.2 2.4 0		ps
RMS Jitter, 12k-20MHz, 125.000MHz	$\phi J$		0.061	0.3	ps
<b>Enable/Disable</b>					
Output Enable/Disable <sup>7</sup> Output Enable Output Disable	$V_{IH}$ $V_{IL}$	$0.7 \cdot V_{DD}$		$0.3 \cdot V_{DD}$	V V
Disable time	$t_D$			150	ns
Start-Up Time	$t_{SU}$			5	ms
Operating Temp (Ordering Option)	$T_{OP}$	-10/70, -40/85, -40/105, -40/125, -55/105, -55/125			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.

2] Parameters are tested with the test circuit shown Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.

5] Duty Cycle is measured as On Time/Period, see Fig 2.

6] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.

7] The Output is Enabled if the Enable/Disable is left open.

8] Only ±50 and ±100ppm stability options are available for -40/105 °C, -40/125 °C, -55/105 °C and -55/125 °C temperature range.

**Table 3. Electrical Performance, 1.8V Option**

Parameter	Symbol	Min	Typical	Max	Units
<b>Supply</b>					
Voltage <sup>1</sup>	$V_{DD}$	1.71	1.8	1.89	V
Maximum Voltage		-0.5		3.6	V
Current <sup>2</sup> ≤40.000MHz 40.000 to 49.999MHz 50.000 to 79.999MHz 80.000 to 99.999MHz 100.0000 to 125.000MHz	$I_{DD}$			2.5 3.5 6.5 7 20	mA
Current, Output Disabled				10	uA
<b>Frequency</b>					
Nominal Frequency <sup>3</sup>	$f_N$	0.625		125.000	MHz
Stability <sup>4,8</sup> (Ordering Option)		±20, ±25, ±50, ±100			ppm
<b>Outputs</b>					
Output Logic Levels <sup>2,3</sup> , <40.000MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	0.9* $V_{DD}$  2.8 2.8		0.1* $V_{DD}$	V V mA mA
Output Logic Levels <sup>2,3</sup> , 40.00-125MHz Output Logic High Output Logic Low Output Logic High Drive Output Logic Low Drive	$V_{OH}$ $V_{OL}$ $I_{OH}$ $I_{OL}$	$V_{DD}$ -0.4  4 4		0.4	V V mA mA
Load	$I_{OUT}$			15	pF
Output Rise /Fall Time <sup>2</sup>	$t_R/t_F$			5	ns
Duty Cycle <sup>2,5</sup>		45	50	55	%
Period Jitter <sup>6</sup> RMS Peak-Peak Random Jitter Deterministic Jitter	$\phi J$		2.4 20.2 2.4 0		ps
RMS Jitter, 12kHz-20MHz, 62.500MHz	$\phi J$		0.4	0.9	ps
<b>Enable/Disable</b>					
Output Enable/Disable <sup>7</sup> Output Enable Output Disable	$V_{IH}$ $V_{IL}$	0.7* $V_{DD}$		0.3* $V_{DD}$	V V
Disable time	$t_D$			150	ns
Start-Up Time	$t_{SU}$			5	ms
Operating Temp (Ordering Option )	$T_{OP}$	-10/70, -40/85, -40/105, -40/125, -55/105, -55/125			°C

1] The power supply should have by-pass capacitors as close to the supply and to ground as possible, for example 0.1 and 0.01uF.

2] Parameters are tested with the test circuit shown Figure 1.

3] See Standard Frequencies and Ordering Information tables for more specific information.

4] Includes initial accuracy, operating temperature, supply voltage, shock and vibration (not under operation) and aging.

5] Duty Cycle is measured as On Time/Period, see Fig 2.

6] Broadband Period Jitter measured using Wavecrest SIA3300C, 90K samples.

7] The Output is Enabled if the Enable/Disable is left open.

8] Only ±50 and ±100ppm stability options are available for -40/105 °C, -40/125 °C, -55/105 °C and -55/125 °C temperature range.

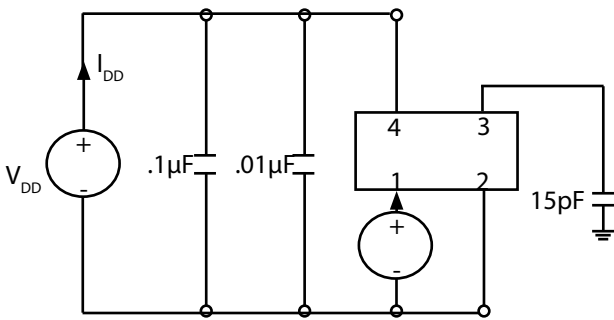


Fig 1: Test Circuit

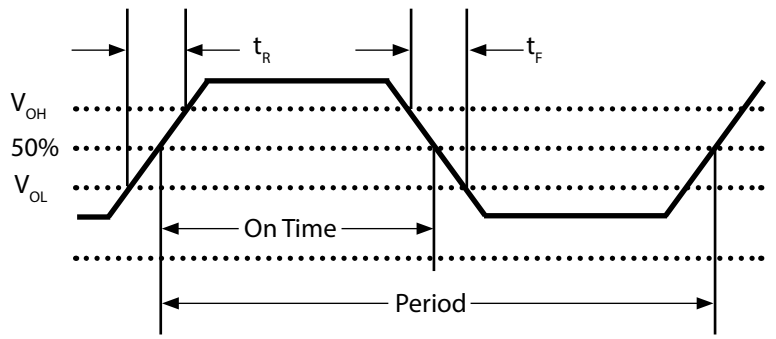
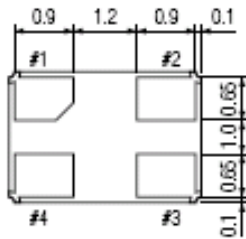
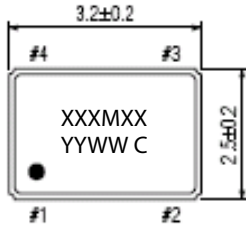


Fig 2: Waveform

## Outline Drawing & Pad Layout



Dimensions in mm

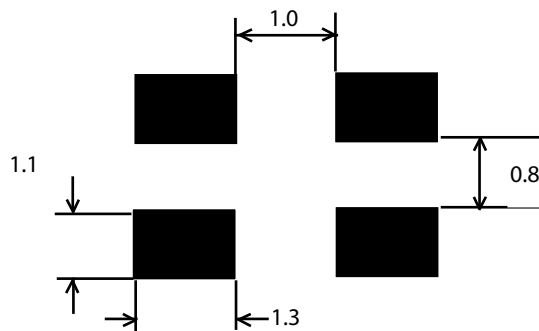


Table 4. Pin Out

Pin	Symbol	Function
1	E/D	Enable Disable
2	GND	Case and Electrical Ground
3	Output	Output
4	V <sub>DD</sub>	Power Supply Voltage

Table 5. Enable Disable Function

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

## Reliability

Vetron qualification will include aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-820 family is capable of meeting the following qualification tests:

Table 6. Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015
Moisture Sensitivity Level	MSL 1
Contact Pads	Gold (0.3µm min - 1.µm max) over Nickel
Weight	27 mg

Although ESD protection circuitry has been designed into the VC-820 proper precautions should be taken when handling and mounting. Vectron employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and design protection evaluation.

Table 7. ESD Ratings

Model	Minimum	Conditions
Human Body Model	1500V	MIL-STD-883, Method 3015
Charged Device Model	1000V	JESD22-C101

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this datasheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability. Permanent damage is also possible if E/D is applied before  $V_{DD}$ .

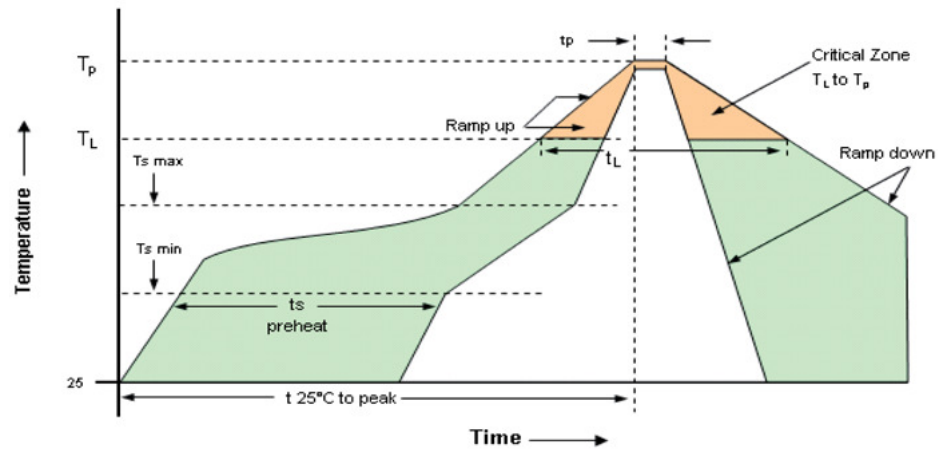
**Table 8. Absolute Maximum Ratings**

Parameter	Symbol	Ratings	Unit
Storage Temperature	$T_S$	-55 to 125	°C
Soldering Temp/Time	$T_{LS}$	260 / 30	°C / sec

## IR Reflow

Solderprofile:

The VC-820 is qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The VC-820 device is hermetically sealed so an aqueous wash is not an issue.



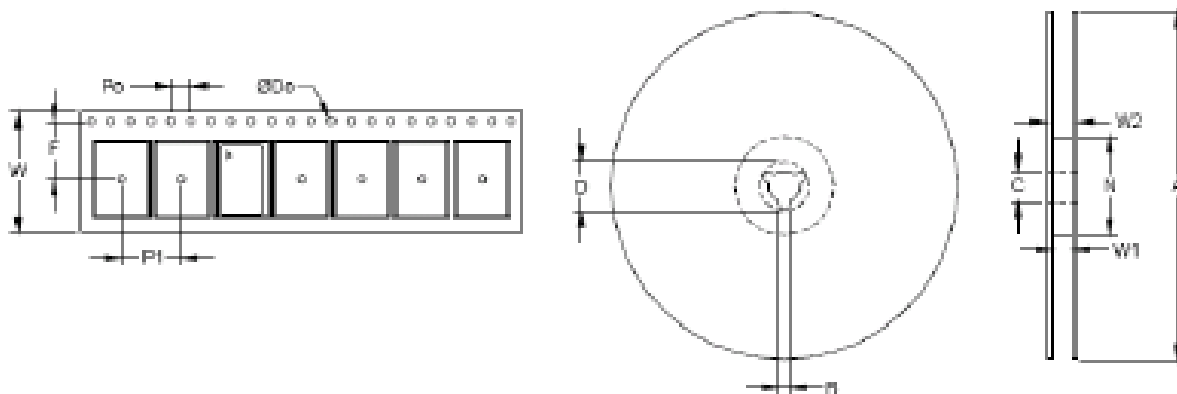
**Table 9. Reflow Profile**

Parameter	Symbol	Value
PreHeat Time $T_S$ -min $T_S$ -max	$t_S$	60 sec Min, 260 sec Max 150°C 200°C
Ramp Up	$R_{UP}$	3 °C/sec Max
Time Above 217 °C	$t_L$	60 sec Min, 150 sec Max
Time To Peak Temperature	$T_{AMB-P}$	480 sec Max
Time at 260 °C	$t_P$	30 sec Max
Ramp Down	$R_{DN}$	6 °C/sec Max

## Tape and Reel

**Table 10 . Tape and Reel Dimensions**

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VC-820	8	3.5	1.5	4	4	178	2	13	21	60	10	14	1000

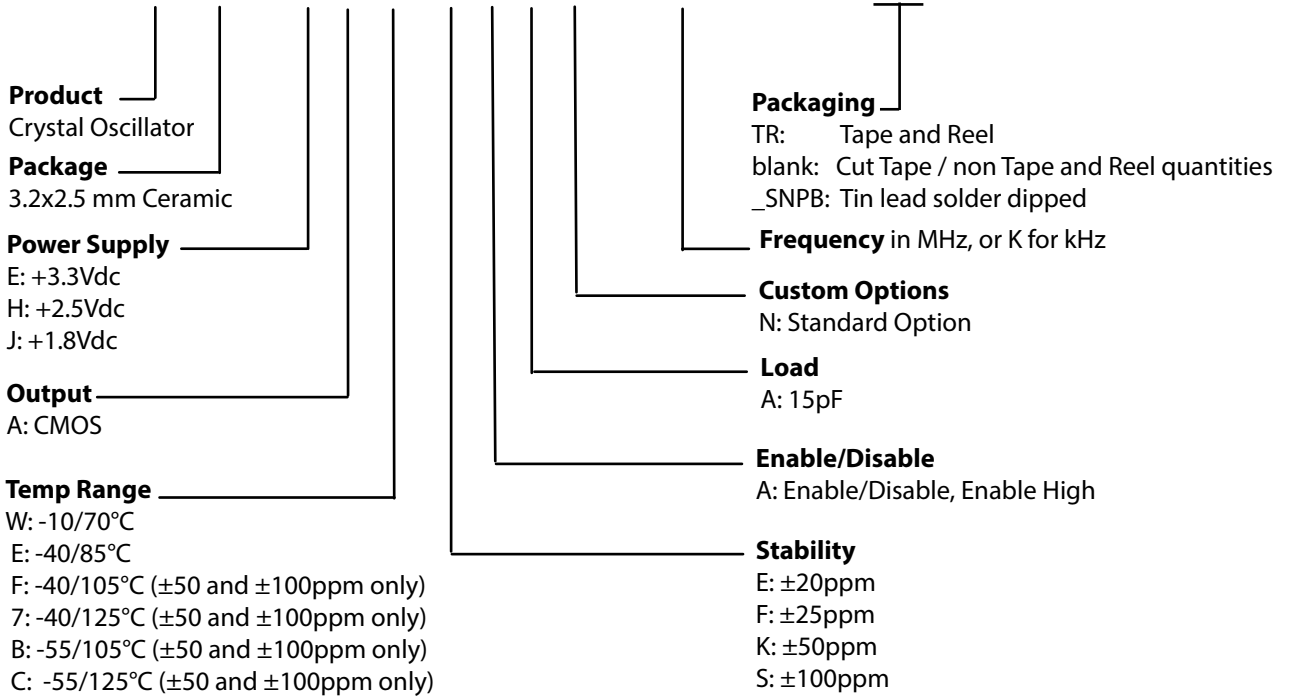


**Table 11. Standard Output Frequencies (MHz)**

0.032768	0.625000	2.000	4.000	8.000	10.000	10.700	14.31818	16.000
16.384	16.875	18.432	20.000	24.000	24.576	25.000	25.0125	26.000
27.000	28.63630	29.4912	30.000	31.250	31.700	32.000	33.000	33.333000
35.328	40.000	43.675771	48.000	50.000	62.500	64.000	66.666000	75.000
80.000	93.750	100.000	106.250	108.000	114.285	125.000		

## Ordering Information

### VC-820- E A W- K A A N- xxMxxxxxxxXX



*\*Note: not all combination of options are available. Other specifications may be available upon request. Please consult with factory.*

**Example:**

<b>VC-820-EAE-KAAN-25M000000TR</b>	<b>Tape and Reel</b>
<b>VC-820-EAE-KAAN-25M0000000</b>	<b>Cut Tape</b>
<b>VC-820-EAE-KAAN-25M0000000_SNPB</b>	<b>Tin lead solder dipped</b>

## Revision History

Revision Date	Approved	Description
January 20, 2015	VN	Included ordering options for -40/105°C, -40/125°C and -55/105°C Operating temperature ranges
August 10, 2018	FB	Update logo and contact information, added SNPB DIP ordering option
March 21, 2019	FB	Update logo and contact information, change to SNPB ordering option
April 30, 2020	FB	Add tape and reel ordering option, updates and corrections as needed

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