256-position I²C Compatible Digital Potentiometer (POT)

CAT5171

The CA5171 is a 256-position digital linear taper potentiometer ideally suited for replacing mechanical potentiometers and variable resistors.

The wiper settings are controlled through an I²C-compatible digital interface. Upon power-up, the wiper assumes a midscale position and may be repositioned anytime after the power is stable. The device can be programmed to reset the wiper position to midscale or to go to a shutdown state during operation. An address input pin, AD0, allows the connection of two devices onto the same I²C bus.

The CAT5171 operates from 2.7 V to 5.5 V, while consuming less than 2 μA. This low operating current, combined with a small package footprint, makes the CAT5171 ideal for battery-powered portable applications.

The CAT5171, designed as a pin for pin replacement for the AD5245, is offered in the 8-lead SOT23 package and operates over the −40°C to +85°C industrial temperature range.

Features

- 256-position
- End-to-End Resistance: 50 kΩ, 100 kΩ
- I²C Compatible Interface
- Power-on Preset to Midscale
- Single Supply 2.7 V to 5.5 V
- Low Temperature Coefficient 100 ppm/°C
- Low Power, I_{DD} 2 μA max
- Wide Operating Temperature −40°C to +85°C
- SOT−23 8-lead (2.9 mm x 3 mm) Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Potentiometer Replacement
- Transducer Adjustment of Pressure, Temperature, Position, Chemical, and Optical Sensors
- RF Amplifier Biasing
- Gain Control and Offset Adjustment

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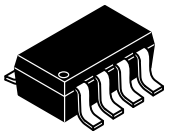
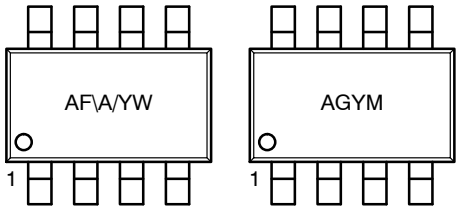


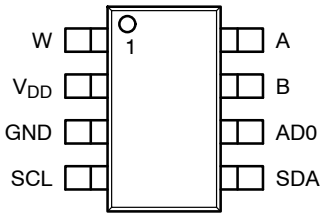
SOT23−8
TP, TB SUFFIX
CASE 527AK

MARKING DIAGRAM



AF = 50 kΩ
AG = 100 kΩ
\A/ = Assembly Location
YW = Production Year and Week
YM = Production Year (last digit) and Month (1 − 9, A, B, C)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

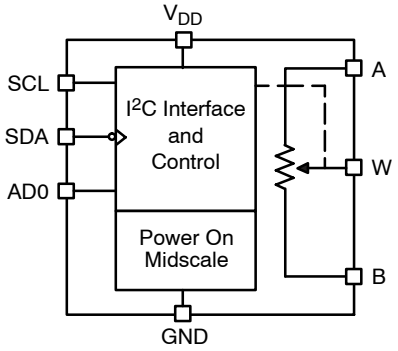


Figure 1. Functional Block Diagram

Table 1. ORDERING INFORMATION

Part Number	Resistance	Temperature Range	Package	Shipping†
CAT5171TBI−50GT3	50 kΩ	−40°C to 85°C	SOT−23−8 (Pb-Free)	3000/Tape & Reel
CAT5171TBI−00GT3	100 kΩ			3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	W	Resistor's Wiper Terminal
2	V_{DD}	Positive Power Supply
3	GND	Digital Ground
4	SCL	Serial Clock Input
5	SDA	Serial Data Input
6	AD0	I^2C Address bit 0 input
7	B	Bottom Terminal of resistive element
8	A	Top Terminal of resistive element

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 2)

Rating	Value	Unit
V_{DD} to GND	−0.3 to 6.5	V
V_A, V_B, V_W to GND	V_{DD}	
I_{MAX}	±20	mA
Digital Inputs and Output Voltage to GND	0 to 6.5	V
Operating Temperature Range	−40 to +85	°C
Maximum Junction Temperature (T_{JMAX})	150	°C
Storage Temperature	−65 to +150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

Table 4. ELECTRICAL CHARACTERISTICS: 50 kΩ and 100 kΩ Versions

V_{DD} = 2.7 V to 5.5 V; V_A = V_{DD}; V_B = 0 V; –40°C < T_A < +85°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ (Note 3)	Max	Unit
DC CHARACTERISTICS — RHEOSTAT MODE						
Resistor Differential Nonlinearity (Note 4)	R_{WB}, V_A = no connection	R–DNL	–1	±0.1	+1	LSB
Resistor Integral Nonlinearity (Note 4)	R_{WB}, V_A = no connection	R–INL	–2	±0.4	+2	LSB
Nominal Resistor Tolerance (Note 5)	T_A = 25°C	ΔR_{AB}	–20		+20	%
Resistance Temperature Coefficient	V_{AB} = V_{DD}, Wiper = no connection	$\Delta R_{AB}/\Delta T$		100		ppm/°C
Wiper Resistance	V_{DD} = 5 V, I_W = ±3 mA	R_W		50	120	Ω
	V_{DD} = 3 V, I_W = ±3 mA			100	250	
DC CHARACTERISTICS — POTENTIOMETER DIVIDER MODE						
Resolution		N			8	Bits
Differential Nonlinearity (Note 6)		DNL	–1	±0.1	+1	LSB
Integral Nonlinearity (Note 6)		INL	–1	±0.4	+1	LSB
Voltage Divider Temperature Coefficient	Code = 0x80	$\Delta V_W/\Delta T$		100		ppm/°C
Full-Scale Error	Code = 0xFF	V_{WFSE}	–3	–1	0	LSB
Zero-Scale Error	Code = 0x00	V_{WZSE}	0	1	3	LSB
RESISTOR TERMINALS						
Voltage Range (Note 7)		$V_{A,B,W}$	GND		V_{DD}	V
Capacitance (Note 8) A, B	f = 1 MHz, measured to GND, Code = 0 x 80	$C_{A,B}$		45		pF
Capacitance (Note 8) W	f = 1 MHz, measured to GND, Code = 0 x 80	C_W		60		pF
Common-Mode Leakage (Note 8)	V_A = V_B = V_{DD}/2	I_{CM}		1		nA
DIGITAL INPUTS						
Input Logic High	V_{DD} = 5 V	V_{IH}	0.7 x V_{DD}			V
Input Logic Low	V_{DD} = 5 V	V_{IL}			0.3V_{DD}	V
Input Logic High	V_{DD} = 3 V	V_{IH}	0.7 x V_{DD}			V
Input Logic Low	V_{DD} = 3 V	V_{IL}			0.3V_{DD}	V
Input Current	V_{IN} = 0 V or 5 V	I_{IL}			±1	μA
POWER SUPPLIES						
Power Supply Range		$V_{DD\ RANGE}$	2.7		5.5	V
Supply Current	V_{IH} = 5 V or V_{IL} = 0 V	I_{DD}		0.3	2	μA
Power Dissipation (Note 8)	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V	P_{DISS}			0.2	mW
Power Supply Sensitivity	ΔV_{DD} = +5 V ±10%, Code = Midscale	PSS			±0.05	%/%
DYNAMIC CHARACTERISTICS (Notes 8 and 10)						
Bandwidth –3 dB	R_{AB} = 50 kΩ / 100 kΩ, Code = 0x80	BW		100/40		kHz
Total Harmonic Distortion	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ	THD_W		0.05		%
V_W Settling Time (50 kΩ/100 kΩ)	V_A = 5 V, V_B = 0 V, ±1 LSB error band	t_S		2		μs

3. Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
4. Resistor position nonlinearity error R–INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R–DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
5. V_{AB} = V_{DD}, Wiper (V_W) = no connect.
6. INL and DNL are measured at VW with the digital potentiometer configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
7. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
8. Guaranteed by design and not subject to production test.
9. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
10. All dynamic characteristics use V_{DD} = 5 V.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. CAPACITANCE

T_A = 25°C, f = 1.0 MHz, V_{DD} = 5 V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 11)	Input/Output Capacitance (SDA, SCL)	$V_{I/O}$ = 0V	8	pF

Table 6. POWER UP TIMING (Notes 11 and 12)

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

11. This parameter is tested initially and after a design or process change that affects the parameter.
12. t_{PUR} and t_{PUW} are delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 7. DIGITAL POTENTIOMETER TIMING

Symbol	Parameter	Min	Max	Units
t_{WRPO}	Wiper Response Time After Power Supply Stable		50	μs
t_{WR}	Wiper Response Time: SCL falling edge after last bit of wiper position data byte to wiper change		20	μs

Table 8. A.C. CHARACTERISTICS

V_{DD} = +2.7 V to +5.5 V, −40°C to +85°C unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency			400	kHz
t_{HIGH}	Clock High Period	600			ns
t_{LOW}	Clock Low Period	1300			ns
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	600			ns
$t_{HD:STA}$	Start Condition Hold Time	600			ns
$t_{SU:DAT}$	Data in Setup Time	100			ns
$t_{HD:DAT}$	Data in Hold Time	0			ns
$t_{SU:STO}$	Stop Condition Setup Time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1300			ns
t_R	SDA and SCL Rise Time			300	ns
t_F	SDA and SCL Fall Time			300	ns
t_{DH}	Data Out Hold Time		100		ns
T_I	Noise Suppression Time Constant at SCL, SDA Inputs			50	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out			1	μs

TYPICAL CHARACTERISTICS

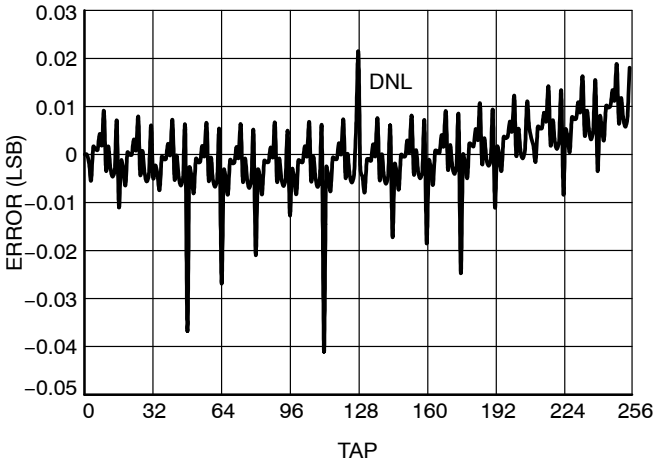


Figure 2. Differential Non−Linearity, V_{DD} = 5.6 V

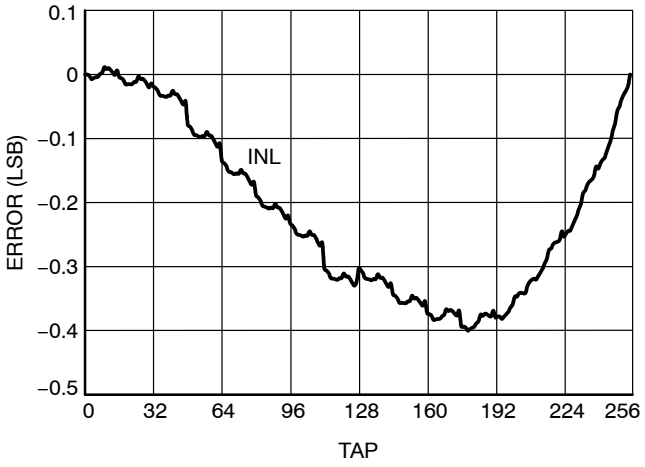


Figure 3. Integral Non−Linearity, V_{DD} = 5.6 V

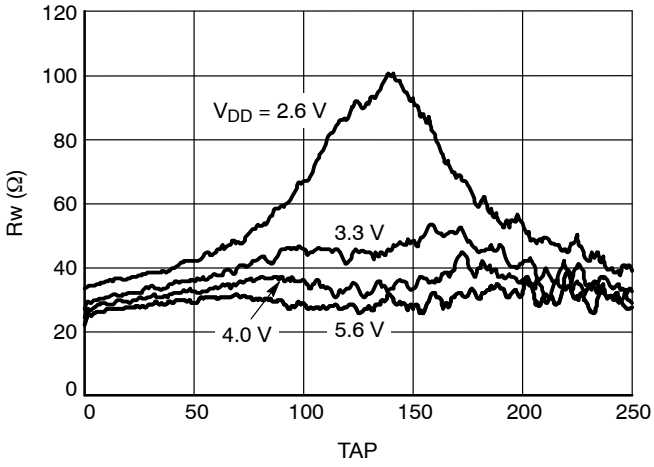


Figure 4. Wiper Resistance at Room Temperature

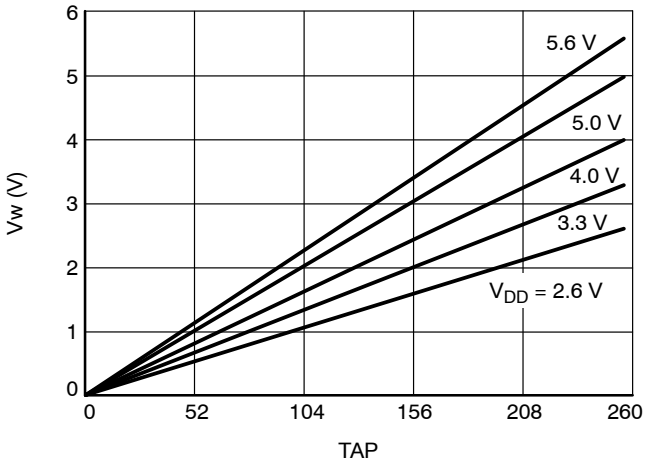


Figure 5. Wiper Voltage

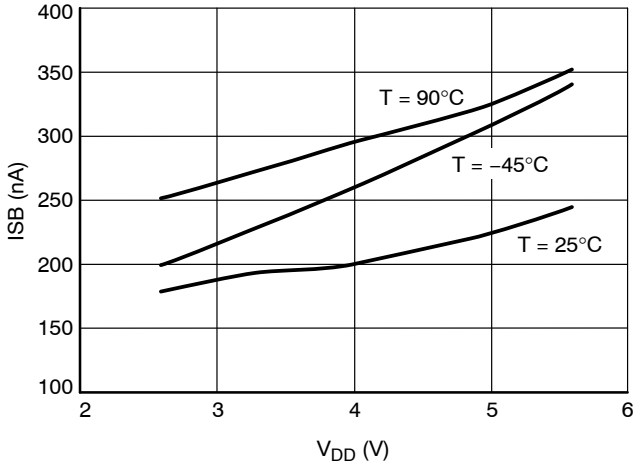


Figure 6. Standby Current

TYPICAL CHARACTERISTICS

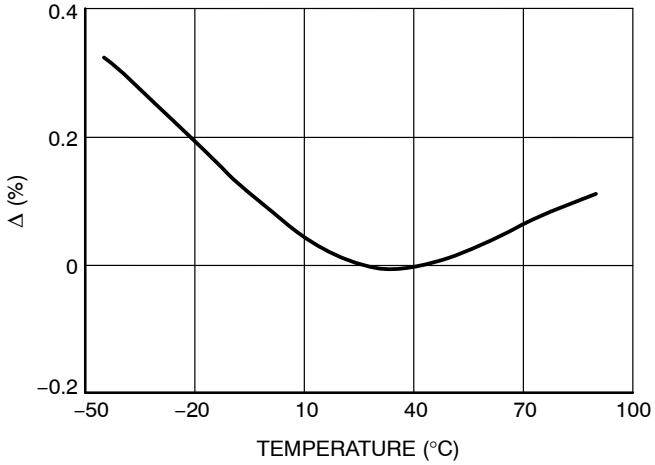


Figure 7. Change in End−to−End Resistance

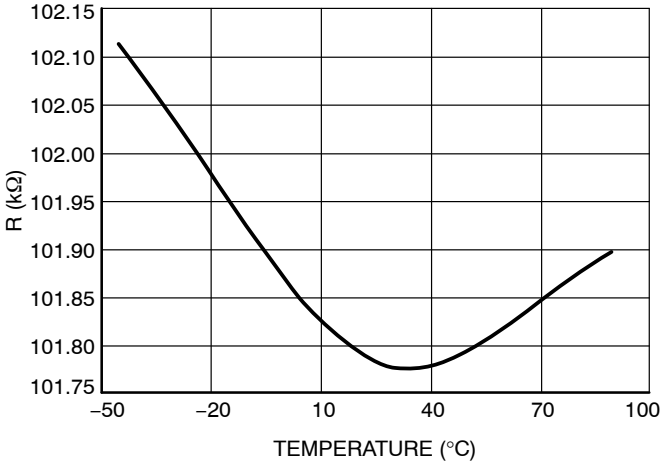


Figure 8. End−to−End Resistance vs. Temperature

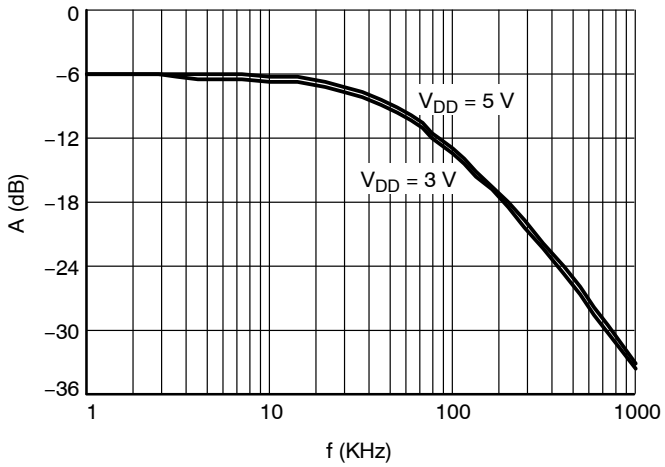


Figure 9. Gain vs. Bandwidth (Tap 0x80)

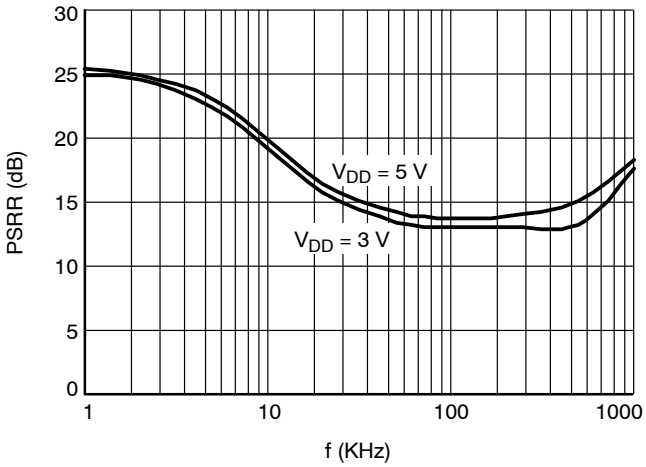


Figure 10. PSRR

BASIC OPERATION

The CAT5171 is a 256-position digitally controlled potentiometer. When power is first applied, the wiper assumes a mid-scale position. Once the power supply is stable, the wiper may be repositioned via the I^2C compatible interface.

PROGRAMMING: VARIABLE RESISTOR

Rheostat Mode

The resistance between terminals A and B, R_{AB}, has a nominal value of 50 kΩ or 100 kΩ and has 256 contact points accessed by the wiper terminal, plus the B terminal contact. Data in the 8-bit Wiper register is decoded to select one of these 256 possible settings.

The wiper's first connection is at the B terminal, corresponding to control position 0x00. Ideally this would present a 0 Ω between the Wiper and B, but just as with a mechanical rheostat there is a small amount of contact resistance to be considered, there is a wiper resistance comprised of the R_{ON} of the FET switch connecting the wiper output with its respective contact point. In CAT5171 this 'contact' resistance is typically 50 Ω. Thus a connection setting of 0x00 yields a minimum resistance of 50 Ω between terminals W and B.

For a 100 kΩ device, the second connection, or the first tap point, corresponds to 441 Ω ($R_{WB} = R_{AB}/256 + R_W$ = 390.6 + 50 Ω) for data 0x01. The third connection is the next tap point, is 831 Ω (2 x 390.6 + 50 Ω) for data 0x02, and so on. Figure 11 shows a simplified equivalent circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

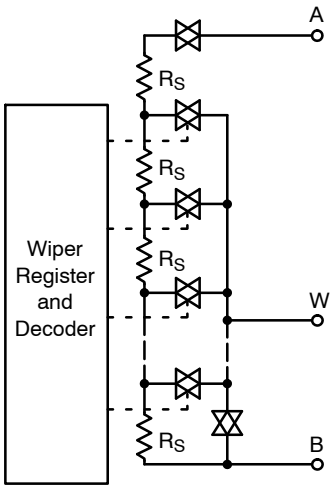


Figure 11. CAT5171 Equivalent Digital POT Circuit

The equation for determining the digitally programmed output resistance between W and B is

$$R_{WB} = \frac{D}{256} R_{AB} + R_W \qquad \text{(eq. 1)}$$

where D is the decimal equivalent of the binary code loaded in the 8-bit Wiper register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 100 kΩ and the A terminal is open circuited, the following output resistance R_{WB} will be set for the indicated Wiper register codes:

Table 9. CODES AND CORRESPONDING R_{WB} RESISTANCE FOR R_{AB} = 100 kΩ, V_{DD} = 5 V

D (Dec.)	R_{WB} (Ω)	Output State
255	99,659	Full Scale (R_{AB} – 1 LSB + R_W)
128	50,050	Midscale
1	441	1 LSB
0	50	Zero Scale (Wiper Contact Resistance)

Be aware that in the zero-scale position, the wiper resistance of 50 Ω is still present. Current flow between W and B in this condition should be limited to a maximum pulsed current of no more than 20 mA. Failure to heed this restriction can cause degradation or possible destruction of the internal switch contact.

Similar to the mechanical potentiometer, the resistance of the digital POT between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} R_{AB} + R_W \qquad \text{(eq. 2)}$$

For R_{AB} = 100 kΩ and the B terminal open circuited, the following output resistance R_{WA} will be set for the indicated Wiper register codes.

Table 10. CODES AND CORRESPONDING R_{WA} RESISTANCE FOR R_{AB} = 100 kΩ, V_{DD} = 5 V

D (Dec.)	R_{WA} (Ω)	Output State
255	441	Full Scale
128	50,050	Midscale
1	99,659	1 LSB
0	100,050	Zero Scale

Typical device to device resistance matching is lot dependent and may vary by up to ±20%.

ESD Protection

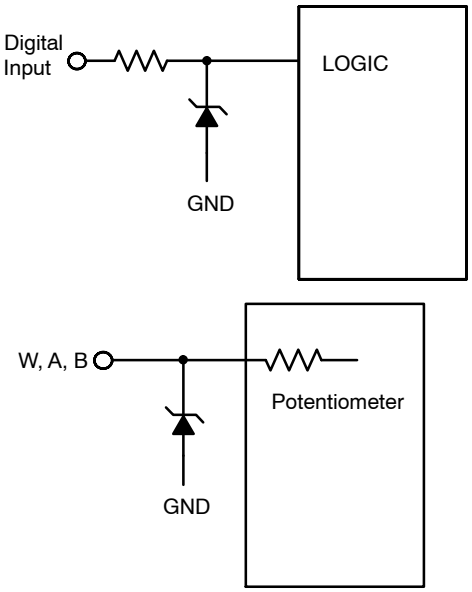


Figure 12. ESD Protection Networks

Terminal Voltage Operating Range

The CAT5171 V_{DD} and GND power supply define the limits for proper 3-terminal digital potentiometer operation. Signals or potentials applied to terminals A, B or the wiper must remain inside the span of V_{DD} and GND. Signals which attempt to go outside these boundaries will be clamped by the internal forward biased diodes.

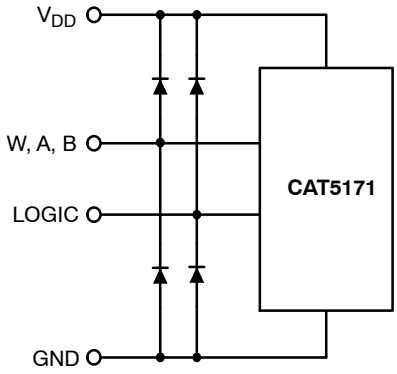


Figure 13.

Power-up Sequence

Because ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 12), it is recommended that V_{DD}/GND be powered before applying any voltage to terminals A, B, and W. The ideal power−up sequence is: GND, V_{DD}, digital inputs, and then $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

Power Supply Bypassing

Good design practice employs compact, minimum lead length layout design. Leads should be as direct as possible. It is also recommended to bypass the power supplies with quality low ESR Ceramic chip capacitors of 0.01 μF to 0.1 μF. Low ESR 1 μF to 10 μF tantalum or electrolytic capacitors can also be applied at the supplies to suppress transient disturbances and low frequency ripple. As a further precaution digital ground should be joined remotely to the analog ground at one point to minimize the ground bounce.

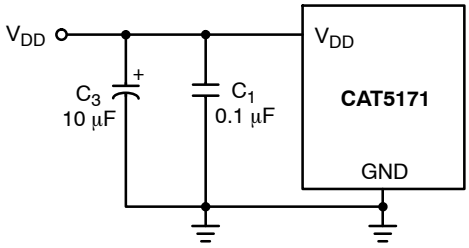


Figure 14. Power Supply Bypassing

I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5171 will be considered a slave device in all applications.

START Condition

The START condition precedes all commands to the device, and is defined as a high to low transition of SDA when SCL is high. The CAT5171 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A low to high transition of SDA when SCL is high determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The six most significant bits of the 8-bit slave address are fixed as 010110 for the CAT5171. The next bit (AD0) is the device least significant address bit and defines which device the Master is accessing. Up to two devices may be individually addressed by the system. Typically, +5 V (V_{DD}) or ground is hard-wired to the AD0 pin to establish the device's address.

After the Master sends a START condition and the slave address byte, the CAT5171 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT5171 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT5171 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5171 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Write Operation

In the Write mode, the Master device sends the START condition and the slave address information to the Slave device. After the Slave generates an acknowledge, the Master sends the instruction byte. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the wiper register. The CAT5171 acknowledges once more and the Master generates the STOP condition.

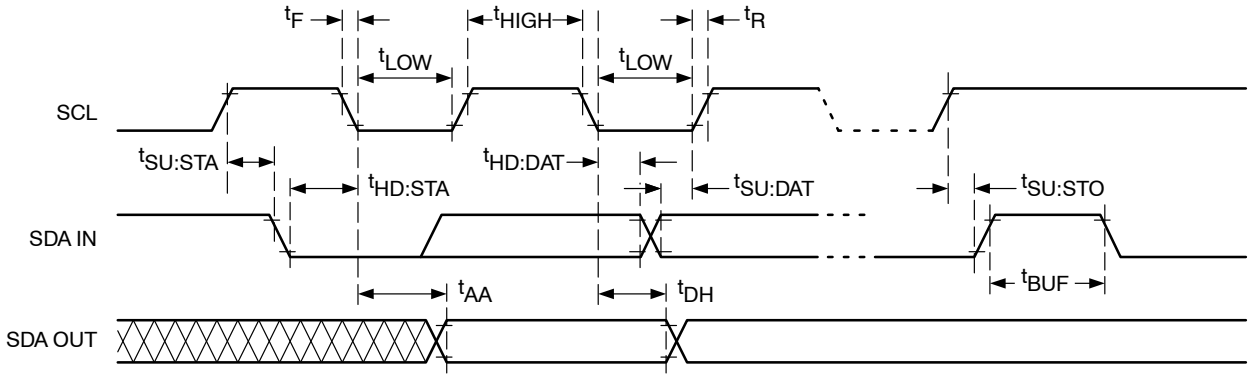


Figure 15. Bus Timing Diagram

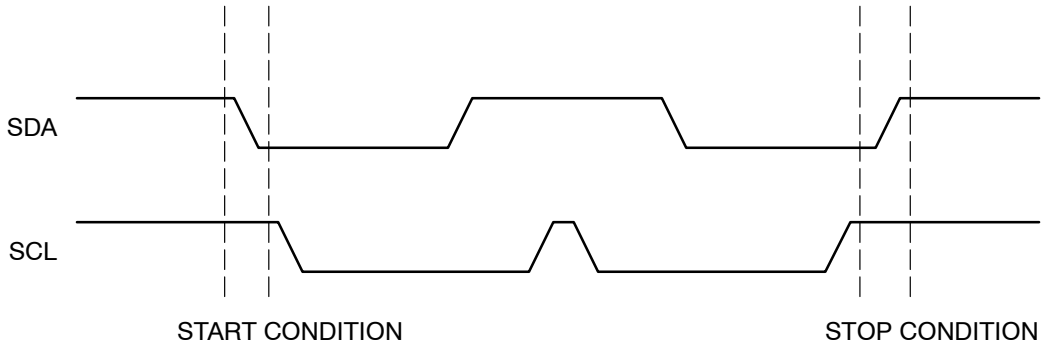


Figure 16. Start/Stop Condition

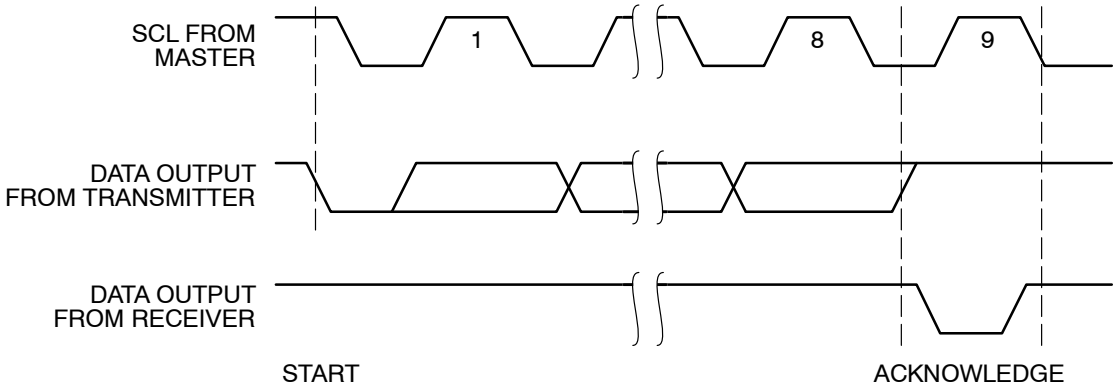


Figure 17. Acknowledge Condition

INSTRUCTION AND REGISTER DESCRIPTION

Slave Address Byte

The first byte sent to the CAT5171 from the master/processor is called the Slave Address Byte. The most significant six bits of the slave address are a device type identifier. For the CAT5171, these bits are fixed at 010110.

The next bit, AD0, is the first bit of the internal slave address and must match the physical device address which is defined by the state of the AD0 input pin for the CAT5171 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The AD0 input can be actively driven by CMOS input signals or tied to the supply voltage or ground.

The next bit, R/$\overline{W}$, indicates whether this command corresponds to a Write or Read instruction. To write into the Wiper control register, R/$\overline{W}$ bit is set to a logic low; while a read from the wiper register is done with the bit high.

Wiper Control

The CAT5171 contains one 8-bit Wiper Control Register (WCR). The Wiper Control Register output is decoded to select one of 256 switches along its resistor array. The contents of the WCR may be written by the host via Write instruction.

The Wiper Control Register is a volatile register that loses its contents when the CAT5171 is powered-down. Upon power-up, the wiper is set to midscale and may be repositioned anytime after the power has become stable.

Instructions

Write and Read instructions are respectively three and two bytes in length. The basic sequence of the two instructions is illustrated in Table 11 and 12.

In write mode, the second byte is the instruction byte. The first bit (MSB) of the instruction byte is a don't care. The second MSB, RS, is the midscale reset. A logic high on this bit moves the wiper to the center tap. The third MSB, SD, is a shutdown bit. A logic high causes an open circuit at terminal A, and short the wiper terminal W to terminal B. The "shutdown" operation does not change the contents of the wiper register. When the shutdown bit, SD, goes back to a logic low, the previous wiper position is restored. Also during shutdown, new settings can be programmed. As soon as the device is returned from shutdown, the wiper position is set according to the wiper register value.

Two CAT5171 on a Single Bus

When needed, it is possible to connect two CAT5171 potentiometers on the same I^2C bus and be able to address each one independently. Each device can be set to a unique address by using the AD0 input pin. One device AD0 pin is connected to ground, and the other device AD0 pin is tied to the supply voltage.

Table 11. Write

S	0	1	0	1	1	0	AD0	$\overline{W}$	A	X	RS	SD	X	X	X	X	X	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Instruction Byte									Data Byte									

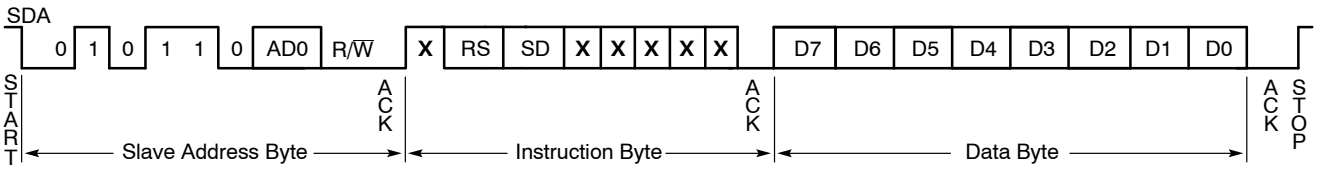
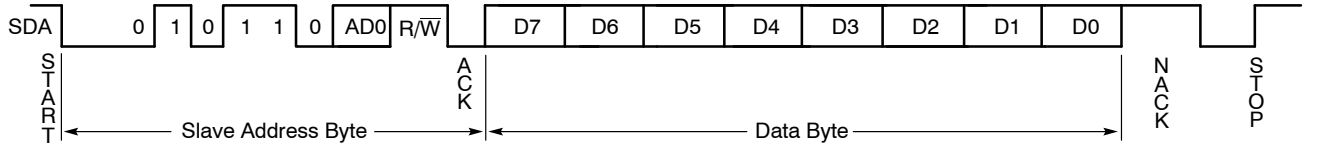


Table 12. READ

S	0	1	0	1	1	0	AD0	R	A	D7	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									



Legend

S = Start
P = Stop
A = Acknowledge
AD0 = Address bit 0, needed when using two potentiometers on the same I^2C bus.
D = Data bit
R = Read (bit is 1 for Read instruction)
$\overline{W}$ = Write (bit is 0 for Write instruction)
RS = When the bit is 1, the wiper position is moved to mid-scale 0x80
SD = Shut Down:
0: normal operation
1: wiper is parked at B terminal and terminal A is open circuit.
X = Don't Care

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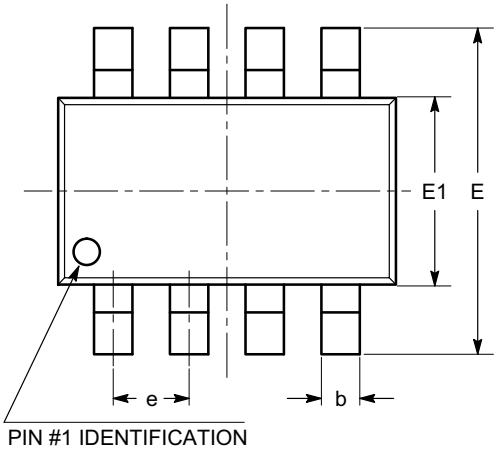
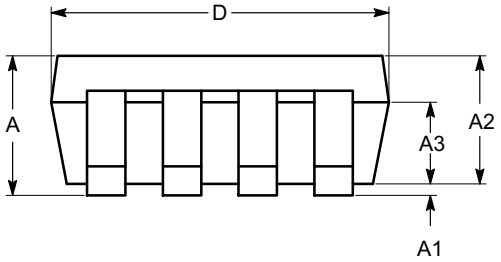
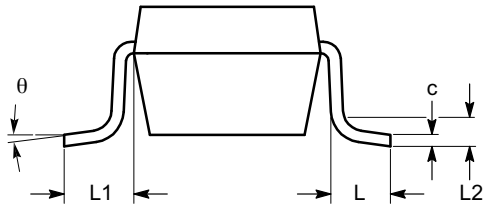


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.10	1.30
A3	0.60		0.80
b	0.28		0.38
c	0.08		0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.65 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

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