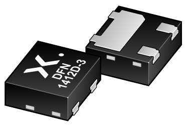


PDTC143/114/124/144EQC series

50 V, 100 mA NPN resistor-equipped transistors

Rev. 1 — 1 October 2021

Product data sheet

1. General description

100 mA NPN Resistor-Equipped Transistor (RET) family in an ultra small DFN1412D-3 (SOT8009) leadless Surface-Mounted Device (SMD) plastic package with side-wettable flanks.

Table 1. Product overview

Type number	R1	R2	Package		PNP complement:
	kΩ	kΩ	Nexperia	JEDEC	
PDTC143EQC	4.7	4.7	SOT8009	MO-340CA	PDTA143EQC
PDTC114EQC	10	10			PDTA114EQC
PDTC124EQC	22	22			PDTA124EQC
PDTC144EQC	47	47			PDTA144EQC

2. Features and benefits

- 100 mA output current capability
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- Suitable for Automatic Optical Inspection (AOI) of solder joint

3. Applications

- Digital applications
- Cost saving alternative for BC847 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

Table 2. Quick reference data

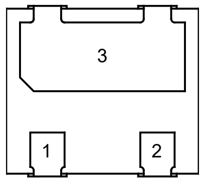
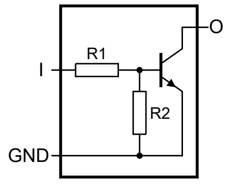
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA

nexperia

5. Pinning information

Table 3. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 Transparent top view	
2	GND	GND (emitter)		
3	O	output (collector)		

6. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTC143EQC	DFN1412D-3	plastic leadless ultra small outline package with side-wettable flanks (SWF); 3 terminals; 0.8 mm pitch; body: 1.4 x 1.2 x 0.48 mm	SOT8009
PDTC114EQC			
PDTC124EQC			
PDTC144EQC			

7. Marking

Table 5. Marking

Type number	Marking code
PDTC143EQC	8N
PDTC114EQC	8J
PDTC124EQC	8M
PDTC144EQC	8R

8. Limiting values

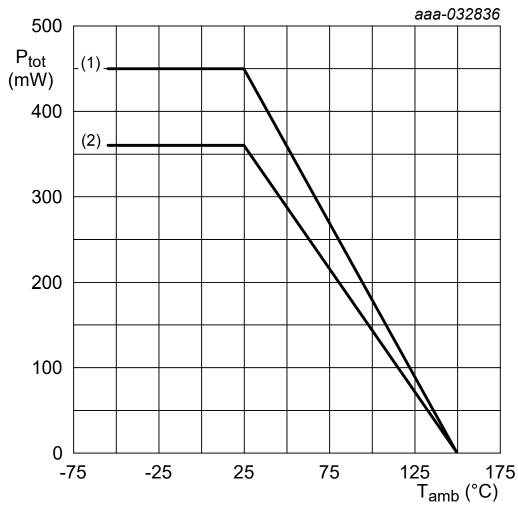
Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage					
	PDTC143EQC			-10	+30	V
	PDTC114EQC			-10	+40	V
	PDTC124EQC			-10	+40	V
	PDTC144EQC			-10	+40	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	T_{amb} ≤ 25 °C	[1]	-	360	mW
			[2]	-	450	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided; 35 µm copper; tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB; single-sided; 70 µm copper; tin-plated and standard footprint.



(1) FR4 PCB; single-sided; 70 µm copper; standard footprint
(2) FR4 PCB; single-sided; 35 µm copper; standard footprint

Fig. 1. Power derating curves

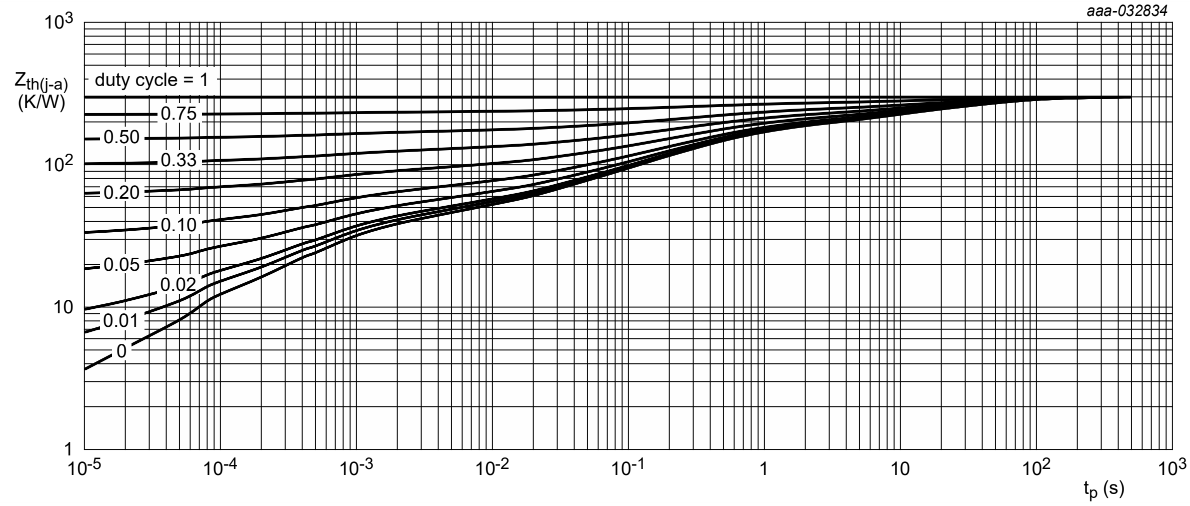
9. Thermal characteristics

Table 7. Thermal characteristics

T_{amb} = 25 °C unless otherwise specified.

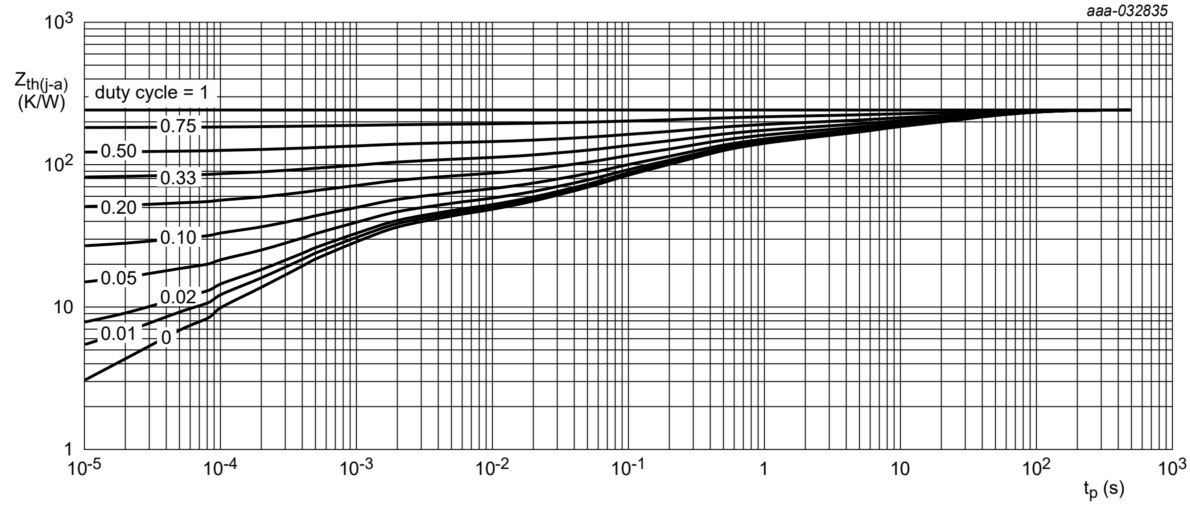
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	348	K/W
			[2]	-	-	278	K/W

[1] Device mounted on an FR4 PCB; single-sided; 35 µm copper; tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB; single-sided; 70 µm copper; tin-plated and standard footprint.



FR4 PCB; single-sided; 35 µm copper; tin-plated and standard footprint.

Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB; single-sided; 70 µm copper; tin-plated and standard footprint.

Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

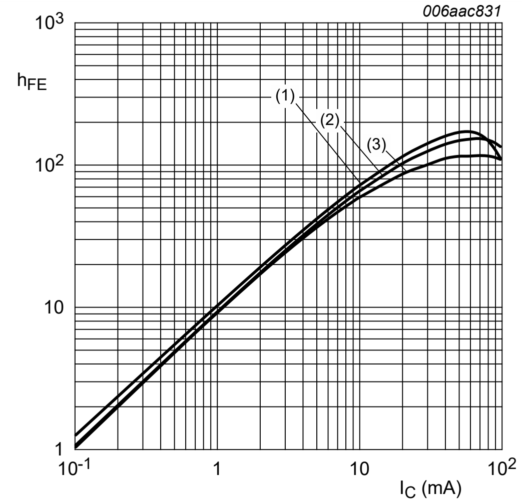
10. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

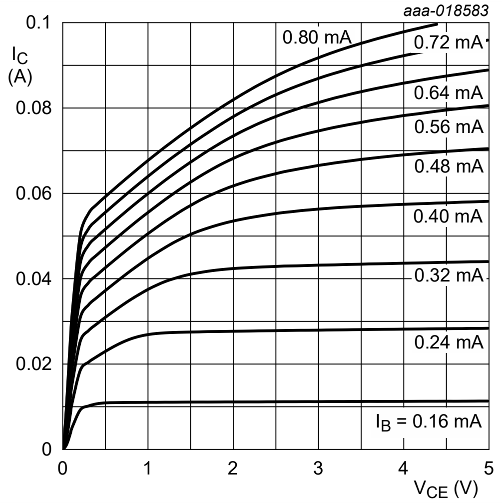
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A		50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A		-	-	100	nA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	5	µA
I_{EBO}	emitter-base cut-off current						
	PDTC143EQC	V_{EB} = 5 V; I_C = 0 A		-	-	900	µA
	PDTC114EQC			-	-	400	µA
	PDTC124EQC			-	-	180	µA
	PDTC144EQC					90	µA
h_{FE}	DC current gain						
	PDTC143EQC	V_{CE} = 5 V; I_C = 10 mA		30	-	-	
	PDTC114EQC	V_{CE} = 5 V; I_C = 5 mA		30	-	-	
	PDTC124EQC			60	-	-	
	PDTC144EQC			80	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA		-	-	100	mV
$V_{I(off)}$	off-state input voltage						
	PDTC143EQC	V_{CE} = 5 V ; I_C = 100 µA		-	1.1	0.5	V
	PDTC114EQC			-	1.1	0.8	V
	PDTC124EQC			-	1.1	0.8	V
	PDTC144EQC			-	1.2	0.8	V
$V_{I(on)}$	on-state input voltage						
	PDTC143EQC	V_{CE} = 0.3 V ; I_C = 20 mA		2.5	1.9	-	V
	PDTC114EQC	V_{CE} = 0.3 V ; I_C = 10 mA		2.5	1.8	-	V
	PDTC124EQC	V_{CE} = 0.3 V ; I_C = 5 mA		2.5	1.7	-	V
	PDTC144EQC	V_{CE} = 0.3 V ; I_C = 2 mA		3.0	1.6	-	V
R1	bias resistor 1 (input)						
	PDTC143EQC		[1]	3.3	4.7	6.1	kΩ
	PDTC114EQC			7	10	13	kΩ
	PDTC124EQC			15.4	22	28.6	kΩ
	PDTC144EQC			33	47	61	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz	[2]	-	230	-	MHz
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz		-	-	2.5	pF

[1] See "Section 11: Test information" for resistor calculation and test conditions
[2] Characteristics of built-in transistor



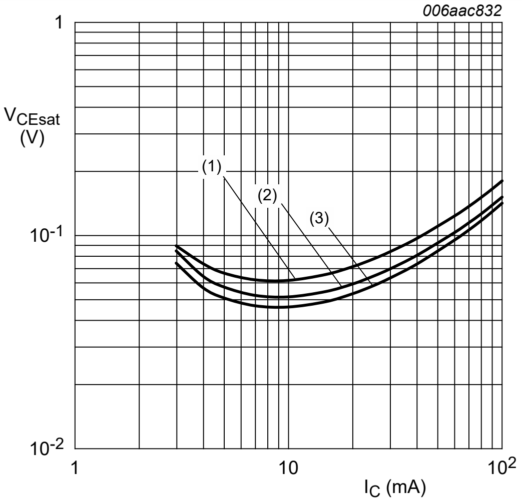
V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 4. PDTC143EQC: DC current gain as a function of collector current; typical values



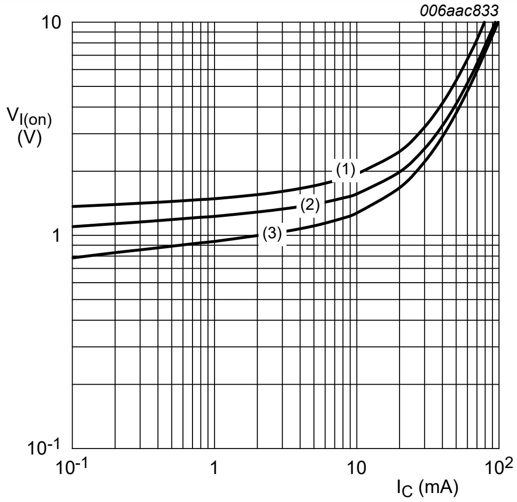
T_{amb} = 25 °C

Fig. 5. PDTC143EQC: Collector current as a function of collector-emitter voltage; typical values



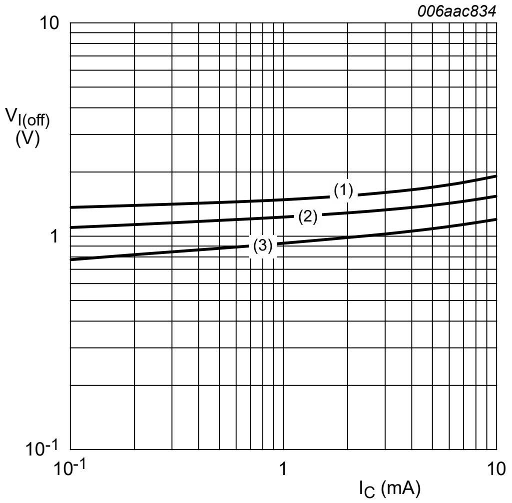
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 6. PDTC143EQC: Collector-emitter saturation voltage as a function of collector current; typical values



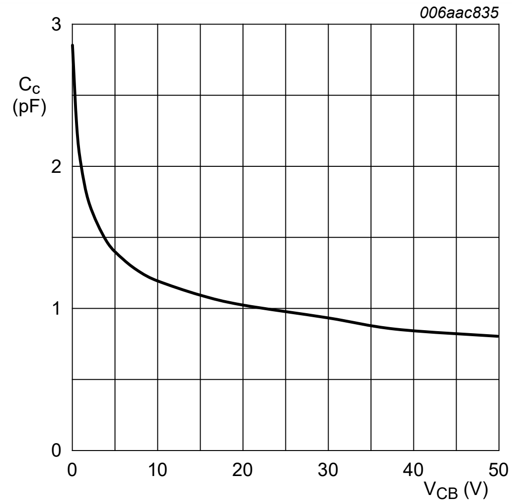
V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 7. PDTC143EQC: On-state input voltage as a function of collector current; typical values



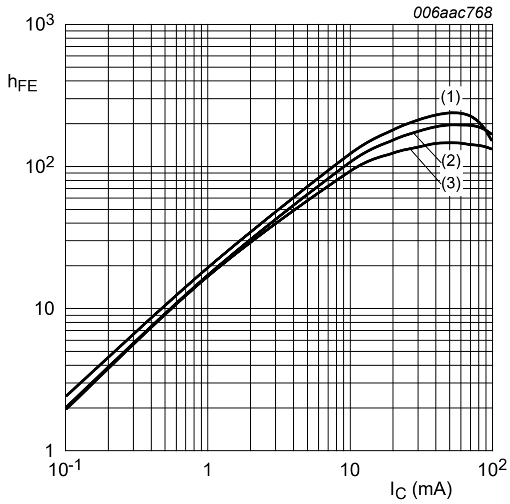
V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 8. PDTC143EQC: Off-state input voltage as a function of collector current; typical values



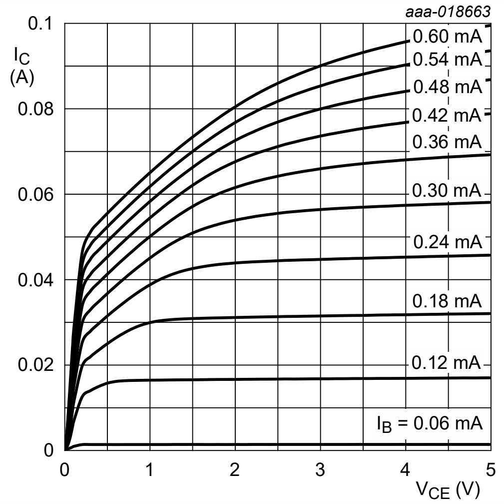
f = 1 MHz
T_{amb} = 25 °C

Fig. 9. PDTC143EQC: Collector capacitance as a function of collector-base voltage; typical values



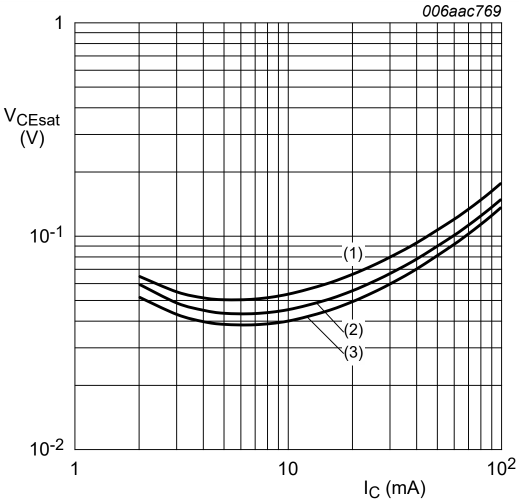
V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 10. PDTC114EQC: DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

Fig. 11. PDTC114EQC: Collector current as a function of collector-emitter voltage; typical values



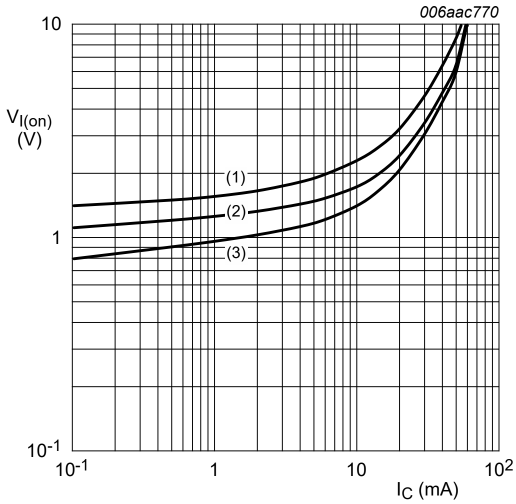
$I_C/I_B = 20$

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = -40 °C

Fig. 12. PDTC114EQC: Collector-emitter saturation voltage as a function of collector current; typical values



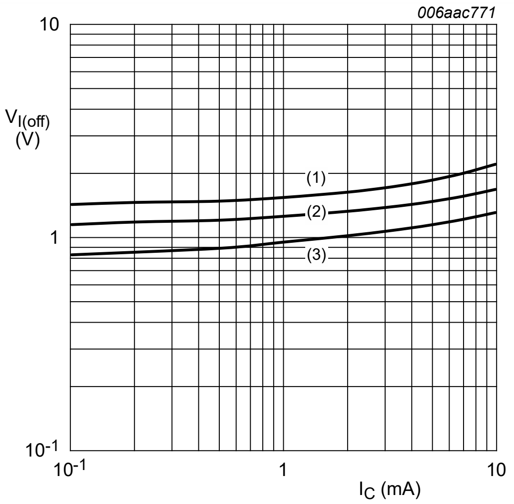
V_{CE} = 0.3 V

(1) T_{amb} = -40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig. 13. PDTC114EQC: On-state input voltage as a function of collector current; typical values



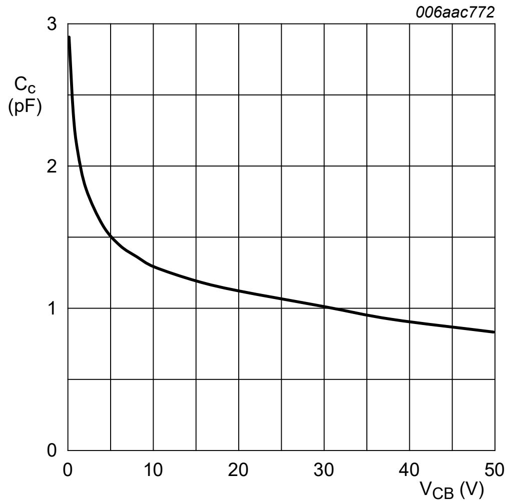
V_{CE} = 5 V

(1) T_{amb} = -40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

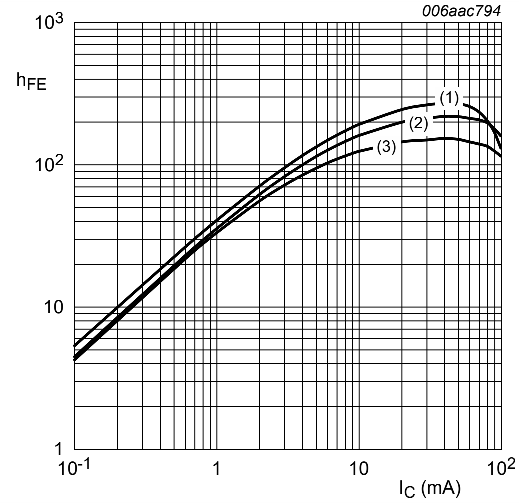
Fig. 14. PDTC114EQC: Off-state input voltage as a function of collector current; typical values



f = 1 MHz

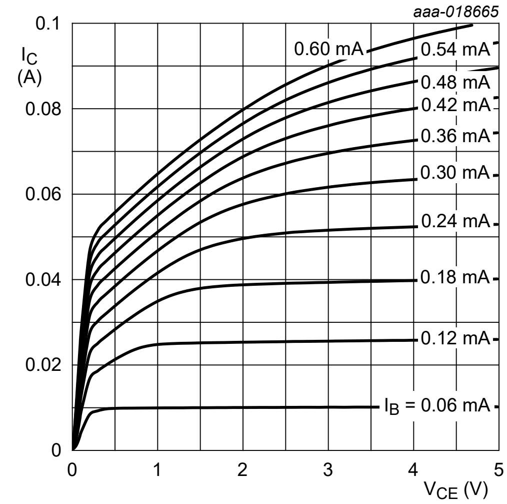
T_{amb} = 25 °C

Fig. 15. PDTC114EQC: Collector capacitance as a function of collector-base voltage; typical values



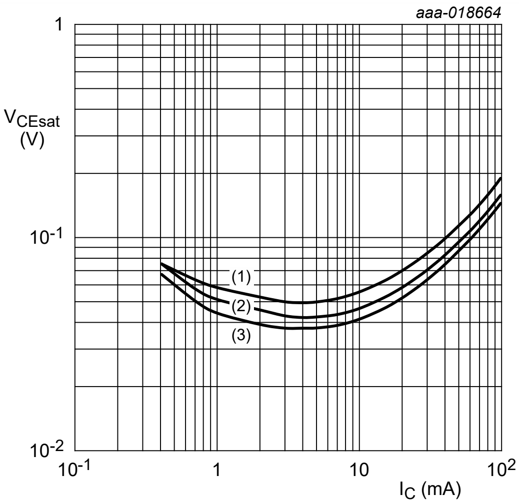
V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 16. PDTC124EQC: DC current gain as a function of collector current; typical values



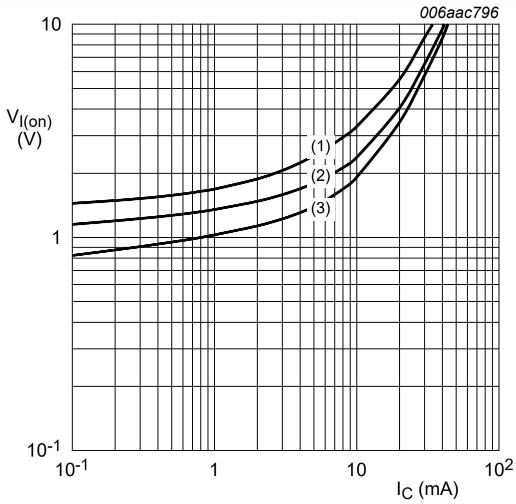
T_{amb} = 25 °C

Fig. 17. PDTC124EQC: Collector current as a function of collector-emitter voltage; typical values



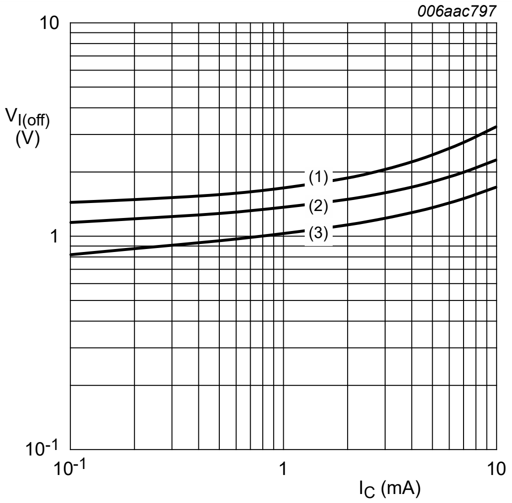
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 18. PDTC124EQC: Collector-emitter saturation voltage as a function of collector current; typical values



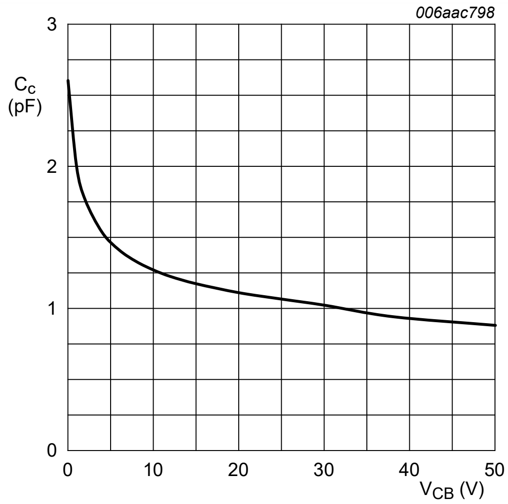
V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 19. PDTC124EQC: On-state input voltage as a function of collector current; typical values



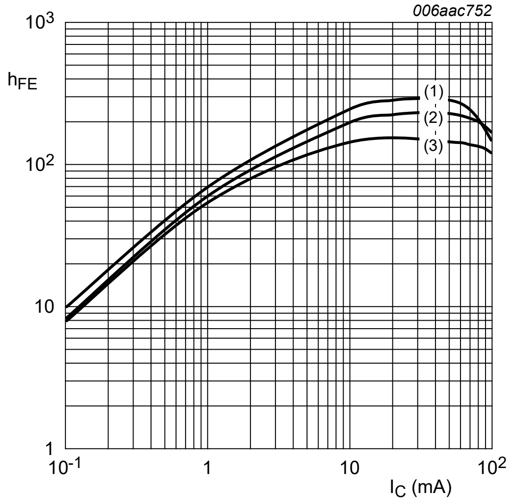
V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 20. PDTC124EQC: Off-state input voltage as a function of collector current; typical values



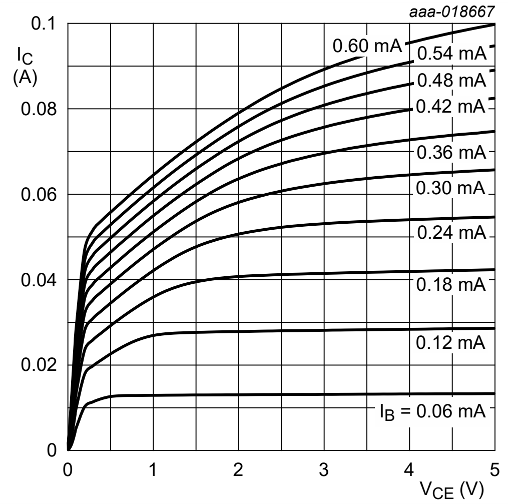
f = 1 MHz
T_{amb} = 25 °C

Fig. 21. PDTC124EQC: Collector capacitance as a function of collector-base voltage; typical values



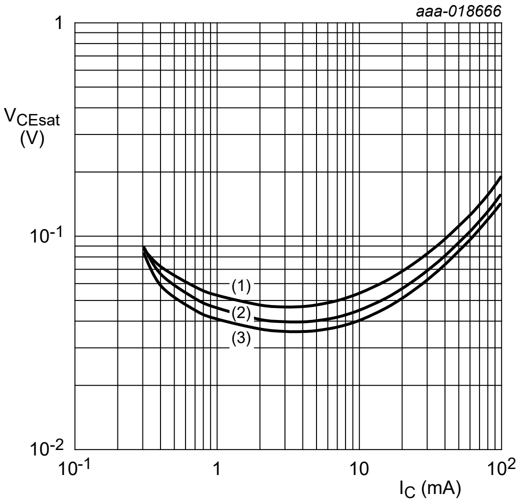
V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 22. PDTC144EQC: DC current gain as a function of collector current; typical values



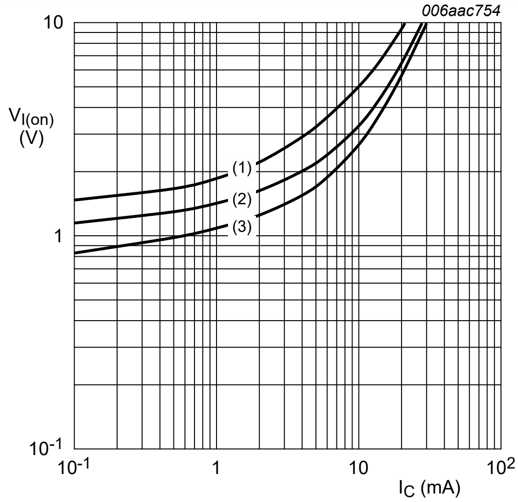
T_{amb} = 25 °C

Fig. 23. PDTC144EQC: Collector current as a function of collector-emitter voltage; typical values



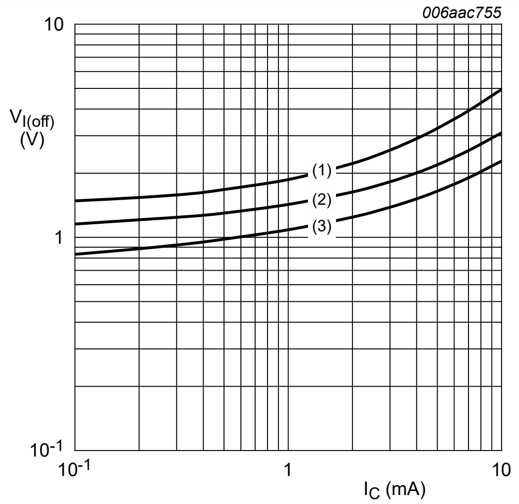
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 24. PDTC144EQC: Collector-emitter saturation voltage as a function of collector current; typical values



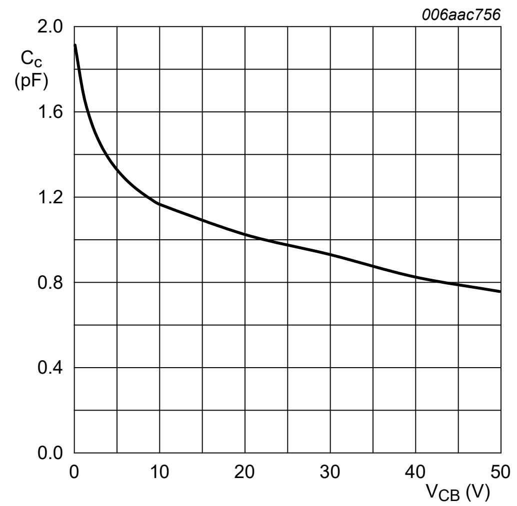
V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 25. PDTC144EQC: On-state input voltage as a function of collector current; typical values



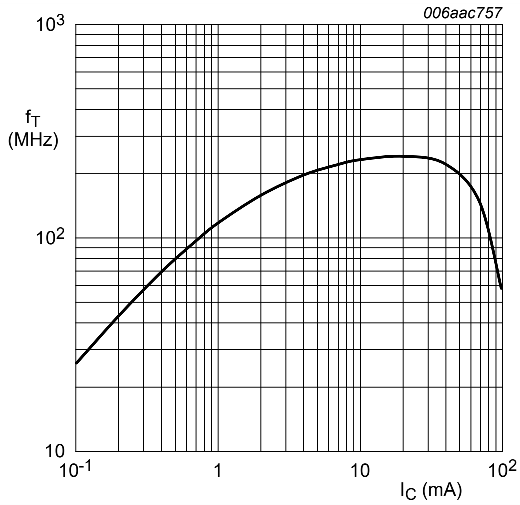
V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 26. PDTC144EQC: Off-state input voltage as a function of collector current; typical values



f = 1 MHz
T_{amb} = 25 °C

Fig. 27. PDTC144EQC: Collector capacitance as a function of collector-base voltage; typical values



f = 100 MHz

T_{amb} = 25 °C

V_{CE} = 5 V

Fig. 28. Transition frequency as a function of collector current; typical values

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

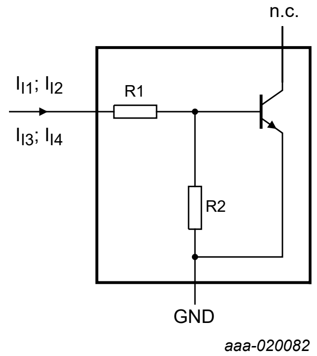


Fig. 29. Resistor test circuit

Resistor test conditions

Table 9. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_{I1}	I_{I2}	I_{I3}	I_{I4}
PDTC143EQC	4.7	4.7	600 µA	700 µA	-600 µA	-700 µA
PDTC114EQC	10	10	350 µA	450 µA	-350 µA	-450 µA
PDTC124EQC	22	22	150 µA	230 µA	-150 µA	-230 µA
PDTC144EQC	47	47	55 µA	105 µA	-55 µA	-105 µA

12. Package outline

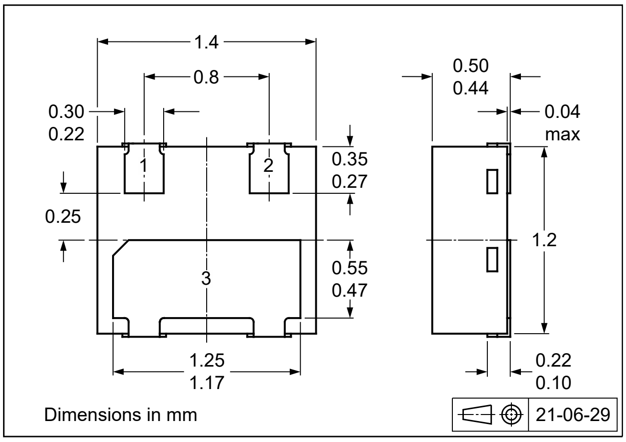


Fig. 30. Package outline DFN1412D-3 (SOT8009)

13. Soldering

Footprint information for reflow soldering of DFN1412D-3 package **SOT8009**

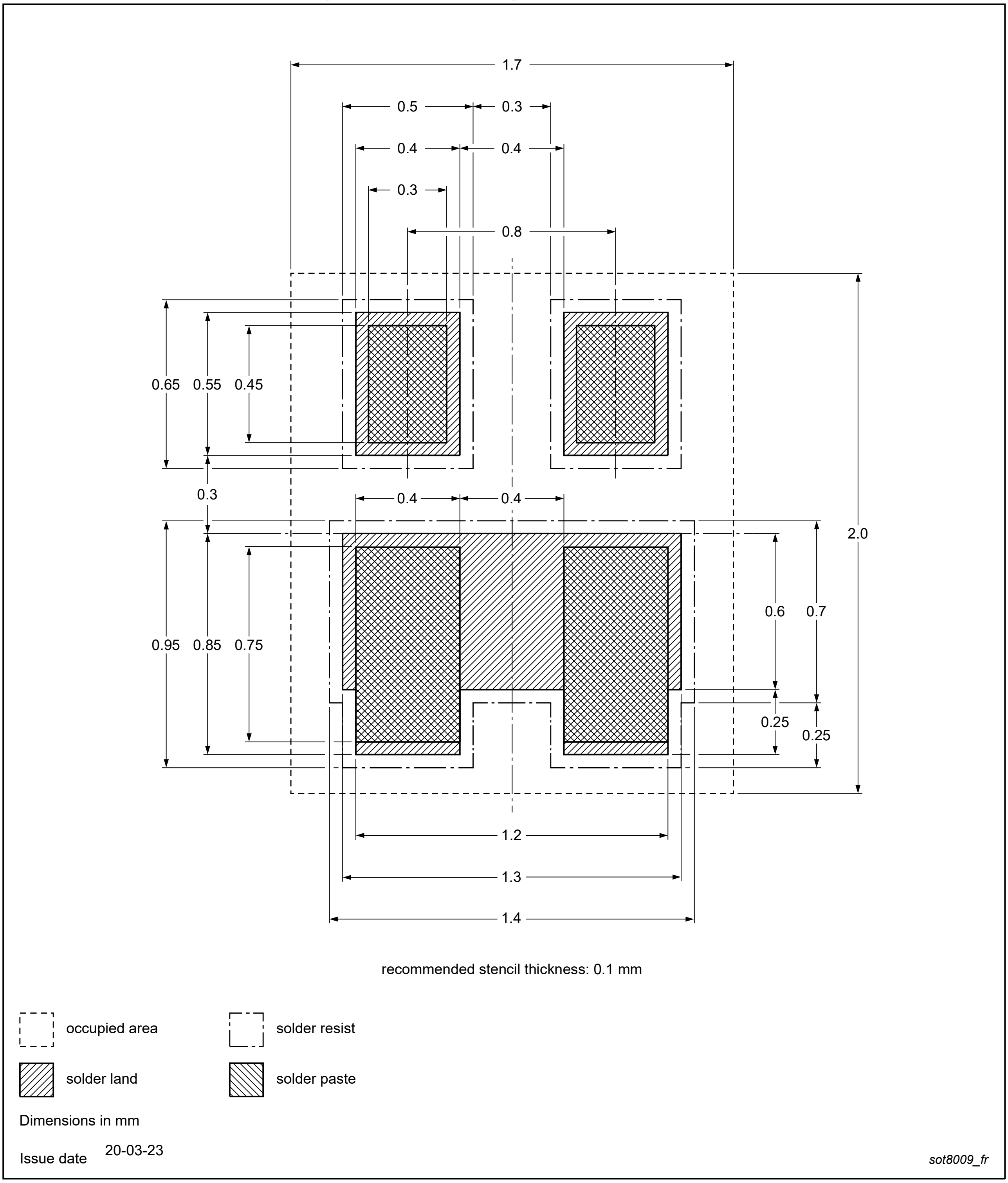


Fig. 31. Reflow soldering footprint DFN1412D-3 (SOT8009)

14. Revision history

Table 10. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTC143_114_124_144EQC_SER v.1	20211001	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

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Contents

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