B10G3741N55D

LDMOS 3-stage integrated Doherty MMIC

AMPLEON

Rev. 2 — 16 April 2021 Product data sheet

1. Product profile

1.1 General description

The B10G3741N55D is a 3-stage fully integrated asymmetrical Doherty MMIC solution using Ampleon's state of the art GEN10 LDMOS technology. The carrier and peaking device, input splitter, output combiner and pre-match are integrated in a single package. This multiband device is perfectly suited as a final stage for small cells and massive MIMO applications in the frequency range from 3700 MHz to 4100 MHz. Available in PQFN outline.

Table 1. Application performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 73 mA (carrier and peaking); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.4$ V. Test signal: 1-carrier LTE 20 MHz; PAR = 7.6 dB at 0.01 % probability CCDF; measured in an Ampleon f = 3700 MHz to 4100 MHz integrated Doherty application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
1-carrier LTE 20 MHz (3900 MHz) PAR = 7.6 dB	3900	28	7.94	34.8	37

1.2 Features and benefits

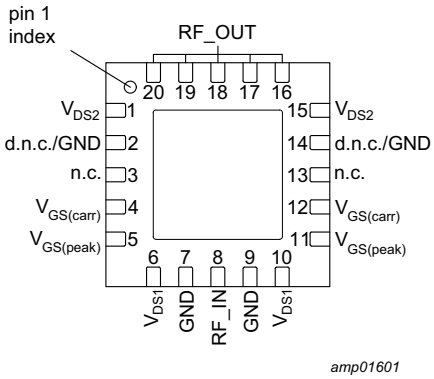
- Integrated input splitter
- Integrated output combiner
- 30 Ω output impedance thanks to integrated pre-match
- Very high efficiency thanks to asymmetry
- Designed for wideband operation (frequency 3700 MHz to 4100 MHz)
- Independent control of carrier and peaking bias
- Integrated ESD protection
- Source impedance 50 Ω; high power gain
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power MMIC for multi-carrier and multi-standard 5G, W-CDMA and LTE base stations in the 3700 MHz to 4100 MHz frequency range

2. Pinning information

2.1 Pinning



Transparent top view.

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{DS2}	1	drain-source voltage of final stages
d.n.c./GND	2	do not connect or GND
n.c.	3	not connected
$V_{GS(carr)}$	4	gate-source voltage of carrier
$V_{GS(peak)}$	5	gate-source voltage of peaking
V_{DS1}	6	drain-source voltage of driver stages
GND	7	RF ground
RF_IN	8	RF input
GND	9	RF ground
V_{DS1}	10	drain-source voltage of driver stages
$V_{GS(peak)}$	11	gate-source voltage of peaking
$V_{GS(carr)}$	12	gate-source voltage of carrier
n.c.	13	not connected
d.n.c./GND	14	do not connect or GND
V_{DS2}	15	drain-source voltage of final stages
RF_OUT	16	RF output
RF_OUT	17	RF output
RF_OUT	18	RF output
RF_OUT	19	RF output
RF_OUT	20	RF output

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Table 2. Pin description *…continued*

Symbol	Pin	Description
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1462-1	B10G3741N55DZ	9349 604 16515	TR13; 500-fold; 16 mm; dry pack	500

4. Block diagram

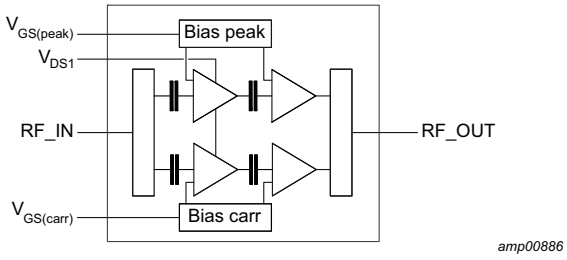

Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	200	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; P_L = 8 W [1]	2.75	K/W
		T_{case} = 90 °C; P_L = 10 W [1]	2.45	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 9.9 dB at 3800 MHz.

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7. Characteristics

Table 6. DC characteristics

T_{case} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 70 mA	1.8	2.1	2.55	V
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	140	nA
Peaking						
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA

Table 7. RF Characteristics

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 70 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.5$ V; P_L = 39 dBm. Test signal: pulsed CW [1]; f = 3900 MHz measured in an Ampleon production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain		32.7	34.7	36.7	dB
η_D	drain efficiency	P_L = 7.94 W (39 dBm)	35	41	-	%
		$P_L = P_{L(3dB)}$	38	42	-	%
RL_{in}	input return loss		-	-	−10	dB
$P_{L(M)}$	peak output power		46.8	47.6	-	dBm

[1] Pulsed CW power sweeps measurement (δ = 10 %; t_p = 100 µs).

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8. Application information

Table 8. Typical performance

T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 73 mA (driver and final stages); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.4$ V. Test signal: 1-carrier LTE 20 MHz; PAR = 7.6 dB at 0.01 % probability CCDF; measured in an Ampleon f = 3700 MHz to 4100 MHz frequency band symmetrical integrated Doherty application circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 3900 MHz [1]	-	47	-	dBm
$\varphi_{s21}/\varphi_{s21(norm)}$	normalized phase response	at 3 dB compression point; f = 3900 MHz [2]	-	−63	-	°
η_D	drain efficiency	8 dB OBO ($P_{L(AV)}$ = 39 dBm); f = 3900 MHz	-	36.6	-	%
G_p	power gain	$P_{L(AV)}$ = 39 dBm; f = 3900 MHz	-	34.8	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 37 dBm; 2-tone CW; f = 3900 MHz	-	400	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 39 dBm; f = 3900 MHz to 4100 MHz	-	2.9	-	dB
$\Delta G/\Delta T$	gain variation with temperature	f = 3900 MHz [3]	-	0.056	-	dB/°C
$ACPR_{20M}$	adjacent channel power ratio (20 MHz)	$P_{L(AV)}$ = 39 dBm; f = 3900 MHz	-	−25.3	-	dBc
K	Rollett stability factor	T_{case} = −40 °C to 125 °C; f = 0.5 GHz to 6.1 GHz [3]	-	>1.5	-	

[1] Pulsed CW power sweeps measurement (δ = 10 %; t_p = 100 µs).

[2] 25 ms CW power sweep measurement.

[3] For both sections (S-parameters measured with broadband demo board).

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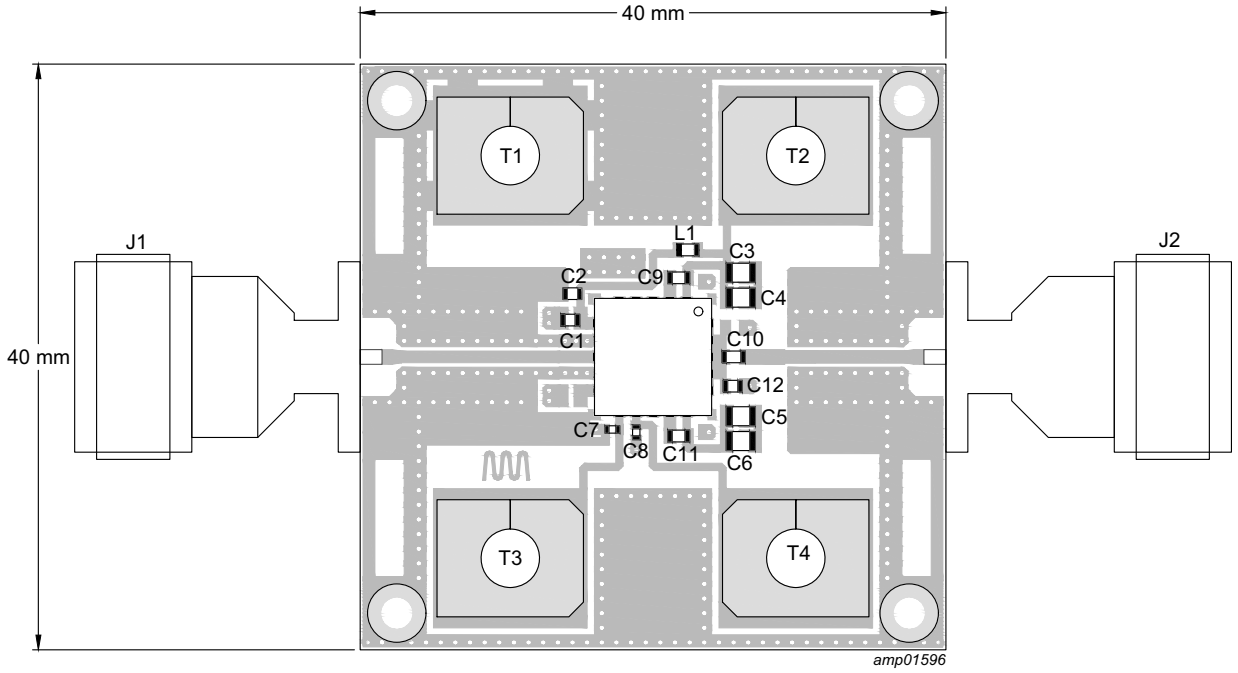

Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm.

Fig 3. Component layout

Table 9. Demo test circuit list of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	15 nF, 50 V	Murata: 06035C153KAZ2A
C2	multilayer ceramic chip capacitor	100 nF, 50 V	Murata: 06035C104KAT2A
C3, C4, C5, C6	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: GRM21BR6YA106KE43
C7, C8	multilayer ceramic chip capacitor	4.7 μF, 6.3 V	Murata: GRM155R60J475ME47D
C9	multilayer ceramic chip capacitor	3 pF ± 0.1 %	Murata: GQM1875C2E3R0BB12
C10	multilayer ceramic chip capacitor	1.6 pF ± 0.1 %	Murata: GQM1875C2E1R6BB12
C11	SMA Coaxial panel connector male	3 pF	Murata: GQM1875C2E3R0BB12
C12	SMA Coaxial panel connector female	0.1 pF	Murata: GQM1875CER10BB12
L1	ferrite bead	420 Ω at 700 MHz [1]	Murata: BLF03JD421GZE
J1	SMA Coaxial panel connector male		Huber & Suhner: 13_SMA-50-0-2/111_N
J2	SMA Coaxial panel connector female		Huber & Suhner: 23_SMA-50-0-2/111_N
T1, T2, T3, T4	PCB Terminal	6.35 mm × 0.81 mm, 4.1 mm	TE connectivity

[1] It is strongly recommended to use L1.

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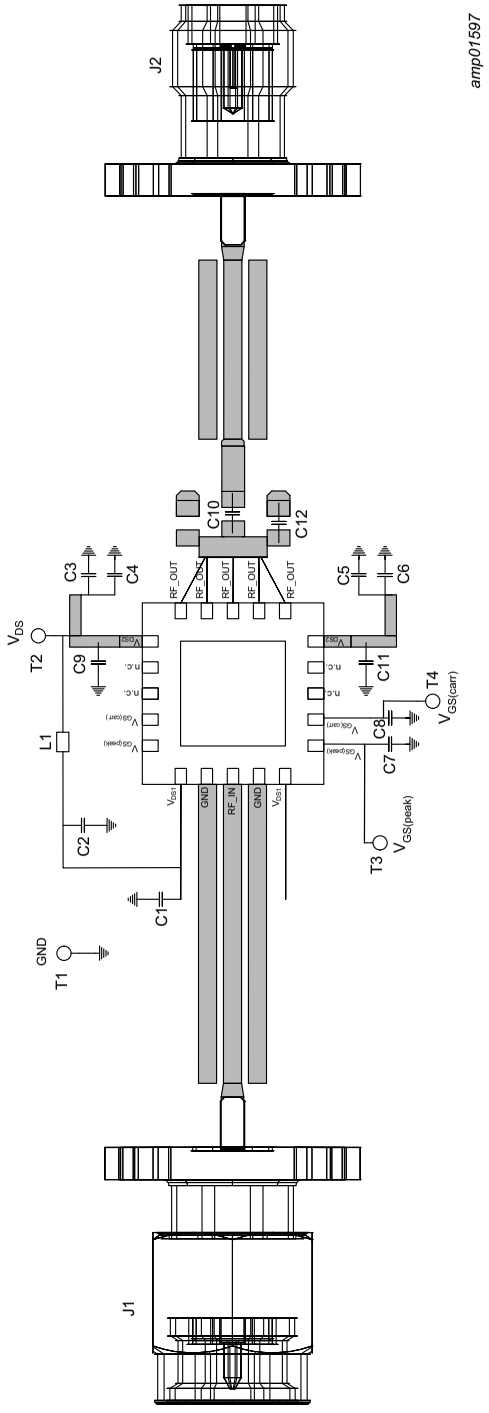

Fig 4. Electrical schematic

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8.1 Ruggedness in a Doherty operation

The B10G3741N55D is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 70 mA (carrier); P_i corresponding to $P_{L(3dB)}$ − 5 dB under Z_S = 50 Ω load; f = 4100 MHz (1-carrier W-CDMA PAR 9.9 signal is used during the stress); T_{case} = 25 °C.

8.2 Impedance information

Table 10. Typical impedance for optimum Doherty operation

Measured load-pull data; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 70 mA (carrier); $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.5 V; t_p = 100 µs; δ = 10 %.

f	tuned for optimum Doherty operation				
	Z_L [1]	$P_{L(3dB)}$	$G_{p(max)}$	η_{add} [2]	η_{add} [3]
(MHz)	(Ω)	(dBm)	(dB)	(%)	(%)
3600	24.78 – j16.91	47.69	34.77	39.50	41.24
3700	23.44 – j16.21	47.70	35.54	40.41	40.60
3800	24.52 – j17.91	47.65	35.85	40.48	40.48
3900	27.03 – j18.57	47.68	36.35	41.97	39.82
4000	28.32 – j17.21	47.67	36.43	43.98	38.49
4100	28.40 – j14.33	47.62	36.13	44.58	37.19
4200	25.82 – j11.16	47.40	36.06	45.92	35.70

[1] Reference package plane.

[2] At $P_{L(3dB)}$.

[3] At 39 dBm.

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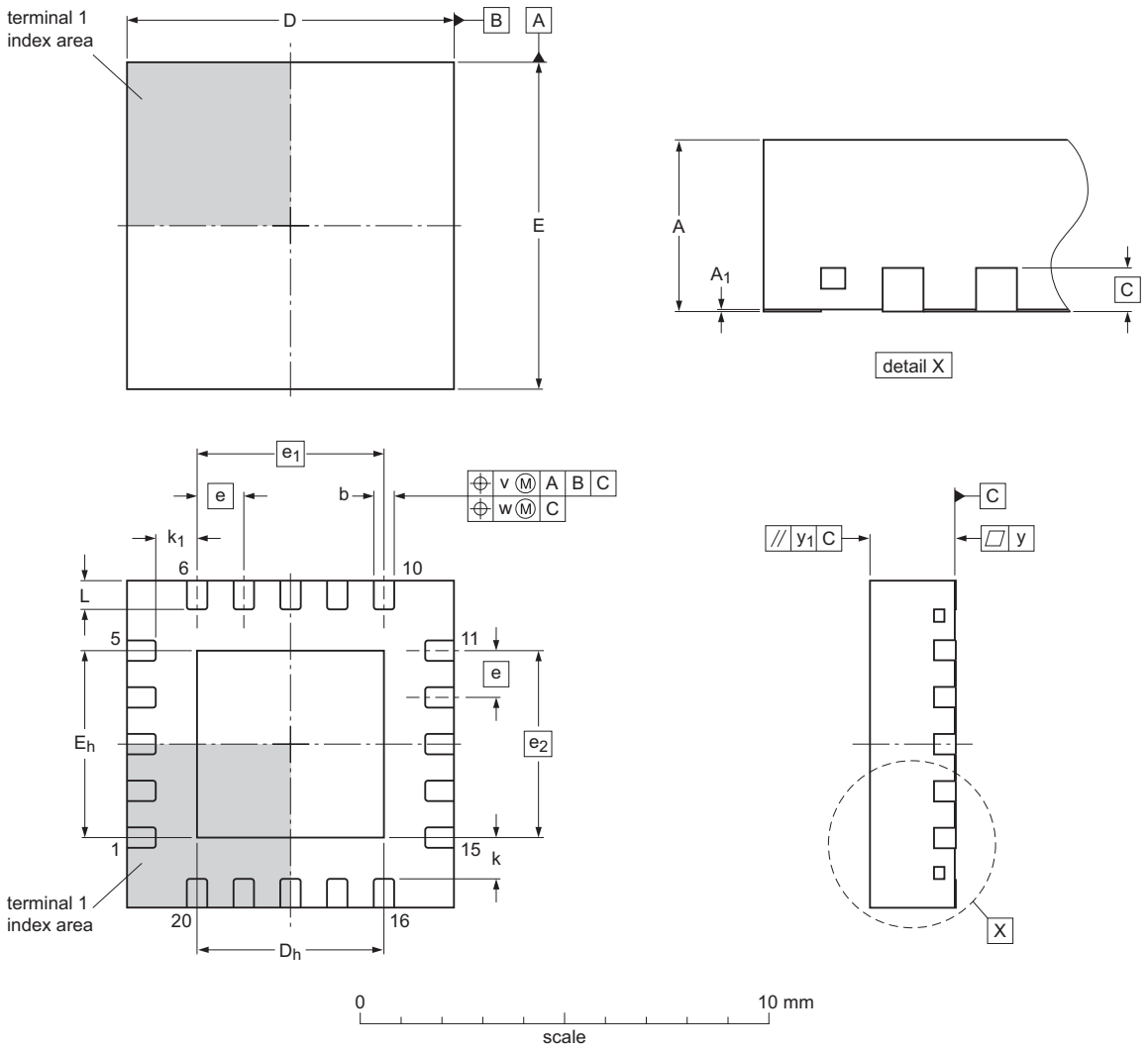
9. Package outline

PQFN20: plastic thermal enhanced quad flat package; no leads; 20 terminals; body 8.0 x 8.0 x 2.1 mm **SOT1462-1**



Dimensions

Unit		A(1)	A1	b	C	D(1)	Dh	E(1)	Eh	e	e1	e2	k	k1	L	v	w	y	y1
	max	2.20	0.05	0.60		8.1	4.72	8.1	4.72						0.8				
mm	nom	2.10		0.50	0.508	8.0	4.62	8.0	4.62	1.15	4.6	4.6			0.7	0.1	0.05	0.1	0.1
	min	2.00	0.00	0.40		7.9	4.52	7.9	4.52				0.99	0.99	0.6				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1462-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1462-1						~~15-10-12~~ 17-06-23

Fig 5. Package outline SOT1462-1 (PQFN20)

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10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

11. Abbreviations

Table 12. Abbreviations

Acronym	Description
5G	Fifth Generation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
ESD	ElectroStatic Discharge
GEN10	Tenth Generation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MIMO	Multiple Input Multiple Output
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

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12. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
B10G3741N55D v.2	20210416	Product data sheet	-	B10G3741N55D v.1
Modifications:	• Figure 3 on page 6: figure updated • Table 9 on page 6: table updated • Figure 4 on page 7: figure updated			
B10G3741N55D v.1	20210330	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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