STNRG012

Datasheet

Digital combo multi-mode PFC and time-shift LLC resonant controller for AC and DC input line

S020

Features

- Digital combo multi-mode PFC + time-shift LLC resonant half-bridge controller
- Management of both AC and DC input
- Input voltage range up to 305 VAC
- On-board 800 V start-up circuit, line sense
- Enhanced fixed-on-time multi-mode TM PFC controller with input voltage feed-forward, new thd optimizer and frequency limitation
- Complete set of PFC protections
- Time-shift control of resonant half-bridge
- Brownout protection
- Complete set of half-bridge protections
- S020 package

Application

- Street lighting
- Home lighting
- Industrial

Description

The STNRG012 embodies a multi-mode (Transition-Mode and DCM) PFC controller, a high-voltage double-ended controller for LLC resonant half-bridge, an 800 V-rated start-up generator and a sophisticated digital engine that manage optimal operation of three blocks.

The STNRG012 manages both input line AC or DC.

The device comes in a 20-pin SO package and offers an advanced solution for power-factor-corrected high-efficiency converters supposed to comply with the most stringent energy saving regulations.

The power system and the control algorithms are managed by an 8 bit core with dedicated fast peripherals (SMED). Optimized digital algorithms together with HW analog IPs are implemented to guarantee very high performance, BOM optimization and robustness.

The digital algorithms are stored in an internal ROM memory and all key application parameters can be stored into a device's NVM memory during production phase, allowing wide configurability and calibration.

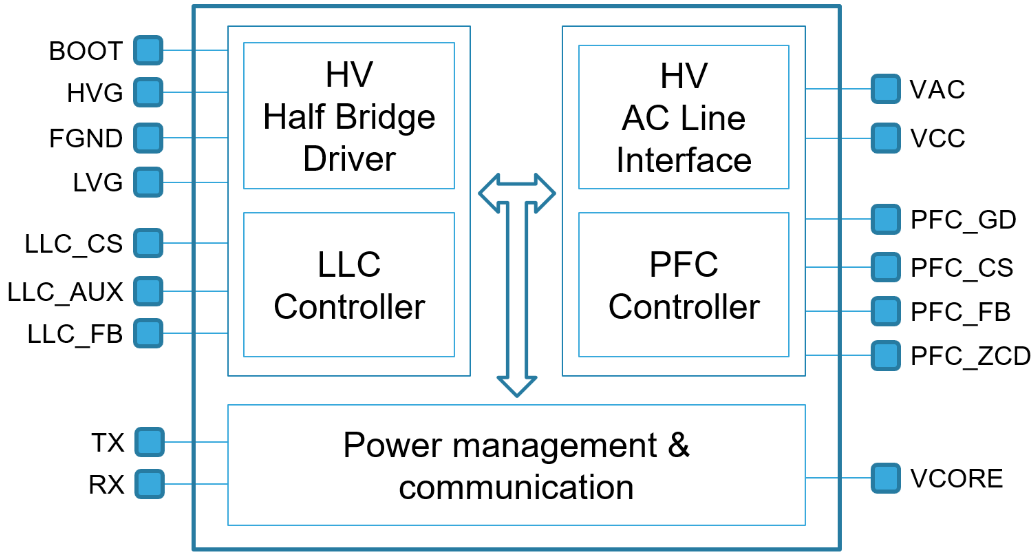
The device can also externally communicate through a 2-pin UART, allowing monitor function, black box storing into an external flash and software patch upload from the external flash.

Product status link
STNRG012

Product label
SUSTAINABLE TECHNOLOGY

1 Block diagram

Figure 1. Block Diagram



2 Pin connection

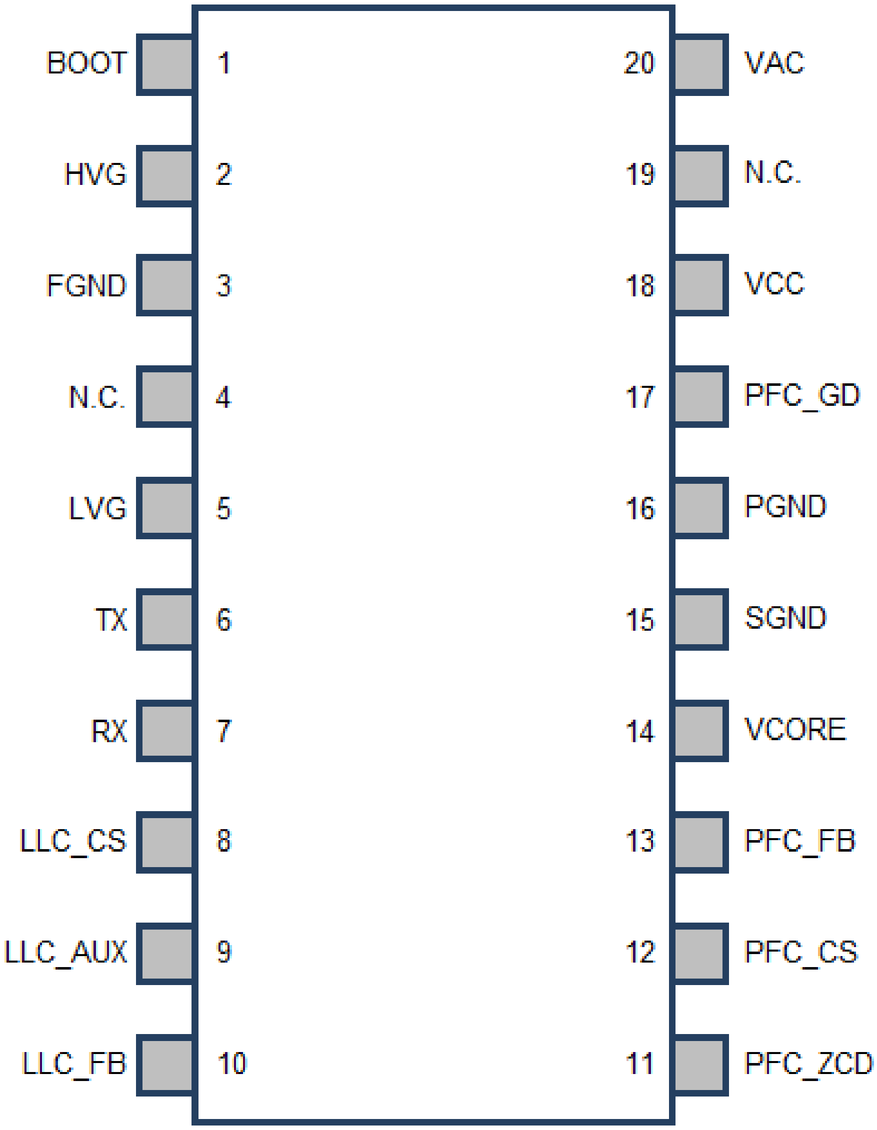


Figure 2. Pin connection (top view)

3 Absolute maximum ratings and thermal data

Table 1. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{AC}	VAC	Voltage range	-1 to 800	V
V_{BOOT}	BOOT	Floating supply voltage, referred to GND	-0.3 to 600 + VCC	V
V_{FGND}	FGND	Half-bridge node voltage	-3 up to a value included in the range BOOT - VCC and BOOT +0.3	V
$d_{VFGND /dt}$	FGND	Floating ground max. slew rate	50	V/ns
V_{HVG}	HVG	HVG voltage	FGND -0.3 to BOOT +0.3	V
V_{VCC}	VCC	IC supply voltage	-0.3 to 19	V
V_{LVG}	LVG, PFC_GD	Voltage range	-0.3 to VCC	V
V_{VCORE}	VCORE	Voltage range	-0.3 to 5.5	V
I_{PFC_CS}, I_{LLC_CS}, I_{PFC_ZCD},	PFC_CS, LLC_CS, PFC_ZCD	Clamped source current (pin voltage: < 0V, self-limited)	2	mA
V_{PFC_CS}, V_{LLC_CS}, V_{PFC_ZCD}	PFC_CS, LLC_CS, PFC_ZCD	Positive voltage range	VCORE+0.3	V
V_{PFC_FB}, V_{LLC_FB}	PFC_FB. LLC_FB	Voltage range	-0.3 to VCORE+0.3	V
V_{RX}	RX	Voltage range	-0.3 to VCORE+0.3	V
V_{TX}	TX	Voltage range	-0.3Vto VCORE+0.3	V

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rth j-amb Jedec 1s0p	Max. thermal resistance, junction-to-ambient, Jedec 1s0p	120	°C/W
Rth j-amb Jedec 2s2p	Max. thermal resistance, junction-to-ambient, Jedec 2s2p	65	°C/W
Tj	Junction temperature operating range	-40 to 150	°C
Tstg	Storage temperature	-55 to 150	°C

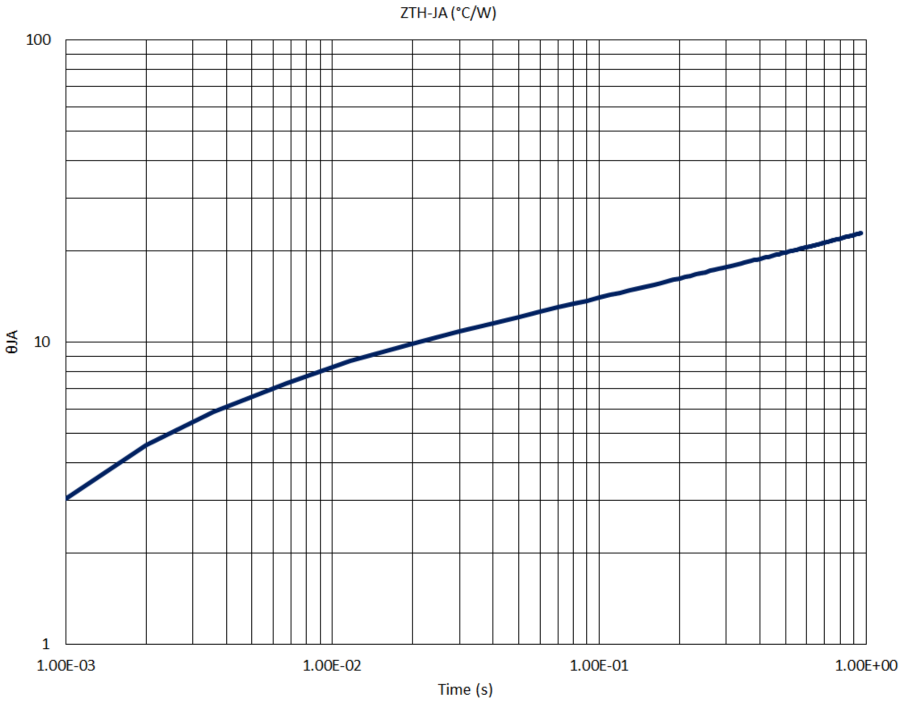
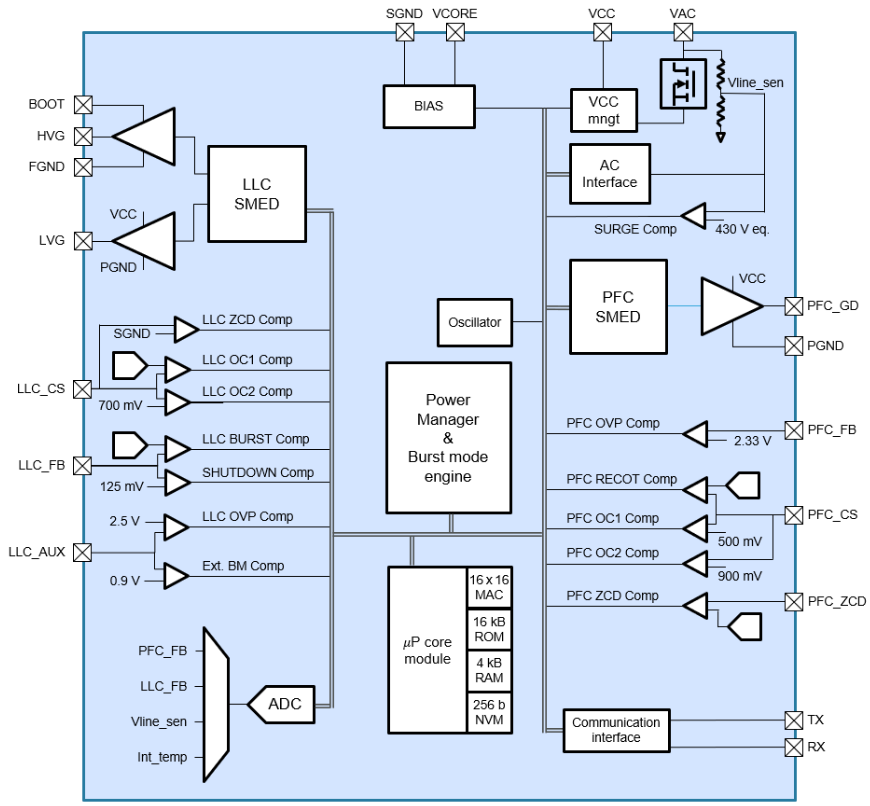


Figure 3. **Dynamic thermal resistance, junction-to-ambient**

4 Detailed block diagram

Figure 4. **Detailed block diagram**



5 Pin function

Table 3. **Pin function detailed description**

N.	Name	Function
1	BOOT	High-side gate-drive floating supply voltage. The bootstrap capacitor is connected between this pin and FGND. A fast diode has to be connected from this pin and VCC to guarantee recharge of the bootstrap capacitor.
2	HVG	High-side gate-drive output. The driver is capable of 0.5 A source and 0.75 A sink peak current (minimum values) to drive the upper MOSFET of the half-bridge leg. A resistor internally connected to FGND ensures that the pin is never floating.
3	FGND	High-side gate-drive floating ground. It is the return path for the high-side gate-drive current. Lay out carefully the connection of this pin to avoid too large spikes below ground.
4	N.C.	High-voltage spacer. The pin is not internally connected to isolate the high-voltage section and ease compliance with safety regulations (creepage distance) on the PCB.
5	LVG	Low-side gate-drive output. The driver is capable of 0.5 A source and 0.75 A sink peak current (minimum values) to drive the lower MOSFET of the half-bridge leg. The pin is actively pulled to GND during UVLO.
6	TX	TX pin for UART/I2C interface
7	RX	RX pin for UART/I2C interface
8	LLC_CS	LLC tank current sensing input. A voltage proportional to the tank current (usually obtained with a capacitive divider) has to be applied to this pin. The information is used for zero-crossing detection (required by time-shift algorithm), the first and second level OCP.
9	LLC_AUX	LLC_AUX is connected to a divider sensing the auxiliary voltage from the LLC transformer. The LLC OVP detection is active on this pin.
10	LLC_FB	The voltage from this pin is used as the LLC feedback voltage. It has to be connected to the feedback phototransistor collector and a pull-up resistor to VCORE.
11	PFC_ZCD	PFC ZCD input, connected to the PFC AUX winding through a resistor divider detecting the PFC inductor demagnetization.
12	PFC_CS	Current sense input for PFC. The current flowing in the MOSFET is sensed through a resistor, and the resulting voltage is applied to this pin. After GD turns on, a first voltage threshold cross allows enhanced COT control implementation. A second level can be detected for overcurrent protection.
13	PFC_FB	Input for PFC output voltage. It is used for closing the PFC loop and OVP protection. It has to be connected with a voltage divider to the bulk capacitor.
14	VCORE	Internal VCORE bypass capacitor connection.
15	SGND	Signal ground. Reference ground for analog signals.
16	PGND	Power ground. Current return for the PFC gate-driver and the low-side gate-driver of the half-bridge. Keep the PCB trace that goes from this pin to the sources of the PFC and the low-side MOSFETs separate from the trace that collects the grounding of the bias components.
17	PFC_GD	PFC gate-driver output.

N.	Name	Function
		The output stage is able to drive power MOSFETs, it is capable of 0.7 A source current and 0.8 A sink current (minimum values).
18	VCC	Supply voltage of both the signal part of the IC and the gate-drivers. A bypass capacitor to GND is necessary to sustain the IC during startup and low power modes. The voltage on the pin is internally clamped to protect the internal circuits from temporary excessive supply voltages.
19	N.C.	The pin is not internally connected to isolate the high-voltage section and ease compliance with safety regulations (creepage distance) on the PCB.
20	VAC	High-voltage startup generator input. The pin has to be connected directly to the mains voltage through two dedicated diodes. If the voltage on the pin is higher than 40 V, an internal current source charges the capacitor connected between the pin VCC and GND until the voltage on the VCC pin reaches the startup threshold. Normally, the generator is re-enabled when the voltage on the VCC pin falls below the UVLO threshold. The pin is also used as the line voltage sensing input. This pin is internally connected to a 20 MΩ resistor divider. It is used for all line sense related functions: the brownout, input voltage feed-forward, line synchronization.

6 Electrical characteristics

(T_j = -40°C to +125°C,Vcc = V_{BOOT} = 15 V,C_{HVG} = C_{LVG} = C_{GD_PFC} = 1 nF; unless otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE						
Vccz	$V_{cc\ clamp}$		19	-	-	
Vcc	Operating range	After turn-on	9.5	-	19	V
Vcc_{On}	Processing turn-on threshold	Voltage rising(1)	16	17	18	V
V_{ccOff}	Processing turn-off threshold	Voltage falling(1)	7.9	8.7	9.4	V
H_{ys}	Hysteresis		-	8.3	-	V
Vcc_{CoreOn}	VCC threshold for VCore turn-on	Voltage rising(1)	-	8	-	V
$Vcc_{CoreOff}$	VCC threshold for VCore turn-off	Voltage falling(1)	-	7	-	V
VCore	Operating range	I_{source} 0 to 1 mA	4.75	-	5.25	V
SUPPLY CURRENT						
I_{VCCS}	Quiescent current during sleep (BM)	T 25°C	-	0.5	-	mA
I_{VCCQ}	Operating supply current @ f_{sw} = 50 kHz, C = 1 nF, VCC = 12 V	PFC and LLC off	-	18	-	mA
		PFC driver only (during pfc ss)	-	20	-	
		All drivers	-	22	-	
HIGH-VOLTAGE START-UP GENERATOR						
V_{AC_BR}	Breakdown voltage	I_{HV} < 50 µA VCC > VCC_{On}	800	-	-	V
I_{VAC_on}	ON-state input current	V_{VAC} > 40 V Vcc < 0.8 V	-	1	-	mA
		V_{VAC} > 40 V 0.8 V < Vcc < Vcc_{CoreOn}	-	6	-	
		V_{VAC} > 100 V Vcc_{CoreOn} < Vcc < 14 V	-	6	-	
		V_{VAC} > 100 V 14 V < Vcc < $Vcc_{\_on}$	-	4	-	
		40 V < V_{VAC} < 100 V Vcc_{CoreOn} < Vcc < 14 V	-	20	-	
		40 V < V_{VAC} < 100 V 14 V < Vcc < Vcc_{on}	-	10	-	
I_{vcc_charge}	ON-state VCC charge current	V_{VAC} > 40 V Vcc < 0.8 V	-0.5	-0.75	-1.3	mA
		V_{VAC} > 40 V 0.8 V < Vcc < Vcc_{CoreOn}	-3.5	-5	-8	

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{vcc_charge}	ON-state VCC charge current	V_{VAC} > 100 V Vcc_{CoreOn} < Vcc < 14 V	-	-5	-	mA
		V_{VAC} > 100 V 14 V < Vcc < Vcc_{on}	-	-3.5	-	
		40 V < V_{VAC} < 100 V Vcc_{CoreOn} < Vcc < 14 V	-	-18	-	
		40 V < V_{VAC} < 100 V 14 V < Vcc < Vcc_{on}	-	-8	-	
I_{VAC_off}	OFF-state VAC input current	V_{VAC} = 400 V, Vcc > Vcc_{on}	-	20	40	µA
$I_{VAC\_HV\_SINK}$	VAC reading improvement current	V_{VAC} = 100 V	-	100	-	µA
PFC - GATE DRIVER						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	-	0.7	V
V_{OH}	Output high voltage	I_{source} = -10 mA VCC = 10 V, VCC = 18 V	9.85 17.9	9.95 17.95	- -	V
I_{srcpk}	Peak source current	Cgate = 4.7 nF(2)	-0.7	-1.1	-	A
I_{snkpk}	Peak sink current	Cgate = 4.7 nF(2)	0.8	1.3	-	A
t_f	Voltage fall time		-	25	-	ns
t_r	Voltage rise time		-	30	-	ns
$PFC_{\_uvlo}$	UVLO saturation	Vcc = 0 to Vcc_{on}, I_{sink} = 1 mA	-	0.9	1.15	V
LOW-SIDE GATE DRIVER (voltages referred to GND)						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	-	0.7	V
V_{OH}	Output high voltage	I_{source} = 10 mA Vcc = 10 V Vcc = 18 V	9.85 17.85	9.9 17.9	- -	V
I_{srcpk}	Peak source current	Cgate = 4.7 nF(2)	-0.5	-0.8	-	A
I_{snkpk}	Peak sink current	Cgate = 4.7nF(2)	0.75	1.2	-	A
t_f	Voltage fall time		-	25	-	ns
t_r	Voltage rise time		-	40	-	ns
$LVG_{\_uvlo}$	UVLO saturation	Vcc = 0 to Vcc_{on}, I_{sink} = 1 mA	-	0.9	1.15	V
HIGH-SIDE GATE DRIVER (voltages referred to FGND)						
V_{OL}	Output low voltage	I_{sink} = 100 mA	-	-	0.7	V
V_{OH}	Output high voltage	I_{source} = 10 mA VBOOT = 10 V, VBOOT = 18 V	9.85 17.85	9.9 17.9	- -	V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{srcpk}	Peak source current	Cgate = 4.7nF(2)	-0.5	-0.8	-	A
I_{snkpk}	Peak sink current	Cgate = 4.7nF(2)	0.75	1.2	-	A
t_f	Voltage fall time		-	25	-	ns
t_r	Voltage rise time		-	40	-	ns
HSGD$_{_pdw}$	HSGD-COMM pull-down		-	25	-	kΩ
I_{FGND}	Current from VBOOT to FGND	V_{boot}= 200 V	-	1.5	-	µA
BROWN IN/OUT						
BI(3)	TH	Vline rising	112	114	116	V
BO(3)		Vline falling		108		V
BIBO_H(3)	H_{yst}		5.25	6	6.75	V
BO$_{_mask}$	Brownout time			77		ms
Overtemperature (by design)						
OTP_TH	TH	T rising	130	140	150	C
OTP_H	H_{yst}	T rising		-30		C
CK						
F_{ck}	Ck run mode		57	60	63.7	MHz
ADC						
ADC$_{_res}$	Resolution	V_{in} ADC > 50 mv	-	10	-	bit
FSR	Conversion range		0	-	2.5	V
DNL	Differential non linearity	V_{in} ADC > 50 mv	-	±1.5	-	lsb
F_{ck_adc}	Clock frequency	V_{in} ADC > 50 mv	-	15	-	MHz
T_s	Sampling time	V_{in} ADC > 50 mv	-	7	-	Adc Ck cycles
T_c	Total conversion time (sampling included)	V_{in} ADC > 50 mv	-	18	-	Adc Ck cycles
COMPARATORS						
PFC_CS RECOT(4)	TH RISE (DAC 6bit)	Input pin PFC_CS		FSR = 125 STEP = 1.95		mV
	HYST			5		
PFC_CS OC1	TH RISE	Input pin PFC_CS		500		mV
	TH FALL			450		
PFC_CS OC2	TH RISE	Input pin PFC_CS		900		mV
	TH FALL			850		
PFCZCD ZCD(4)	TH FALLING (TH_F)	Input pin PFC_ZCD		0/50/100/200		mV
	HYST (TH_R)			210/110(5)/310/ TH_F +10		
PFC_FB OVP	TH RISING	Input pin PFC_FB		2.33		V
	HSYR			75		mV
LLC_FB(4)	TH RISING	Input pin LLC_FB		0.75/1/1.25		V
BURST	HYST			5/10		mV

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
LLC_FB SHUTDOWN	TH RISING	Input pin LLC_FB		145		mV
	TH FALLING			125		
LLC_AUX OVP	TH RISE	Input pin LLC_AUX		2.5		V
	TH FALL			2.4		
LLC_AUX Ext BM.	TH RISING	Input pin LLC_AUX		0.9		V
	TH FALLING			0.8		
LINE SURGE	TH RISING	Input pin VAC		430		V
	TH FALLING			410		
LLC_OC1(4)	TH RISING (DAC 5bit)	Input pin LLC_CS		FSR = 500 STEP = 15.6		mV
	HYST			20		mV
LLC_OCP2	TH RISING	Input pin LLC_CS		700		
	TH FALLING			650		

1. *Parameters tracking each other.*
2. *Guaranteed by design, not production tested.*
3. *Thresholds referred only to AC input line.*
4. *Thresholds and hysteresis are programmed by the software in use.*
5. *The selection for TH_R = 110 mV is not allowed if TH_F = 200 mV.*

7 Typical application schematic

Figure 5. Typical application schematic (part 1)

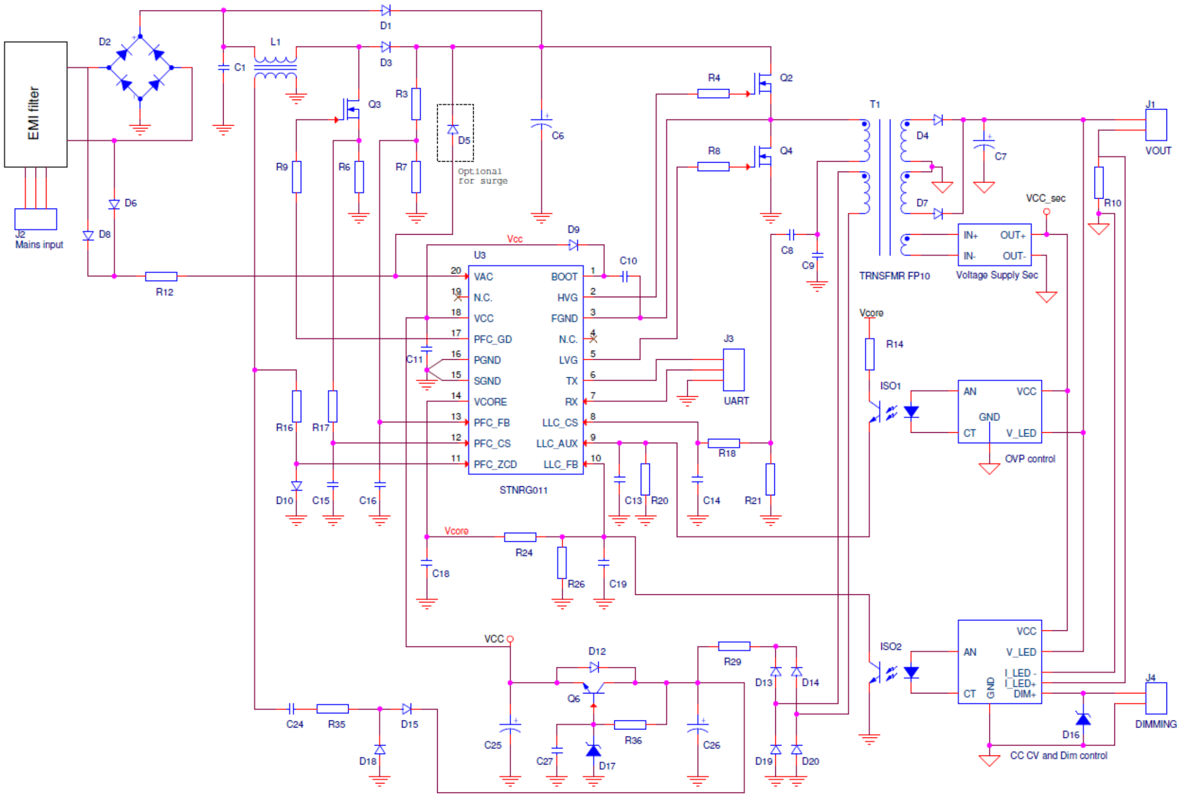
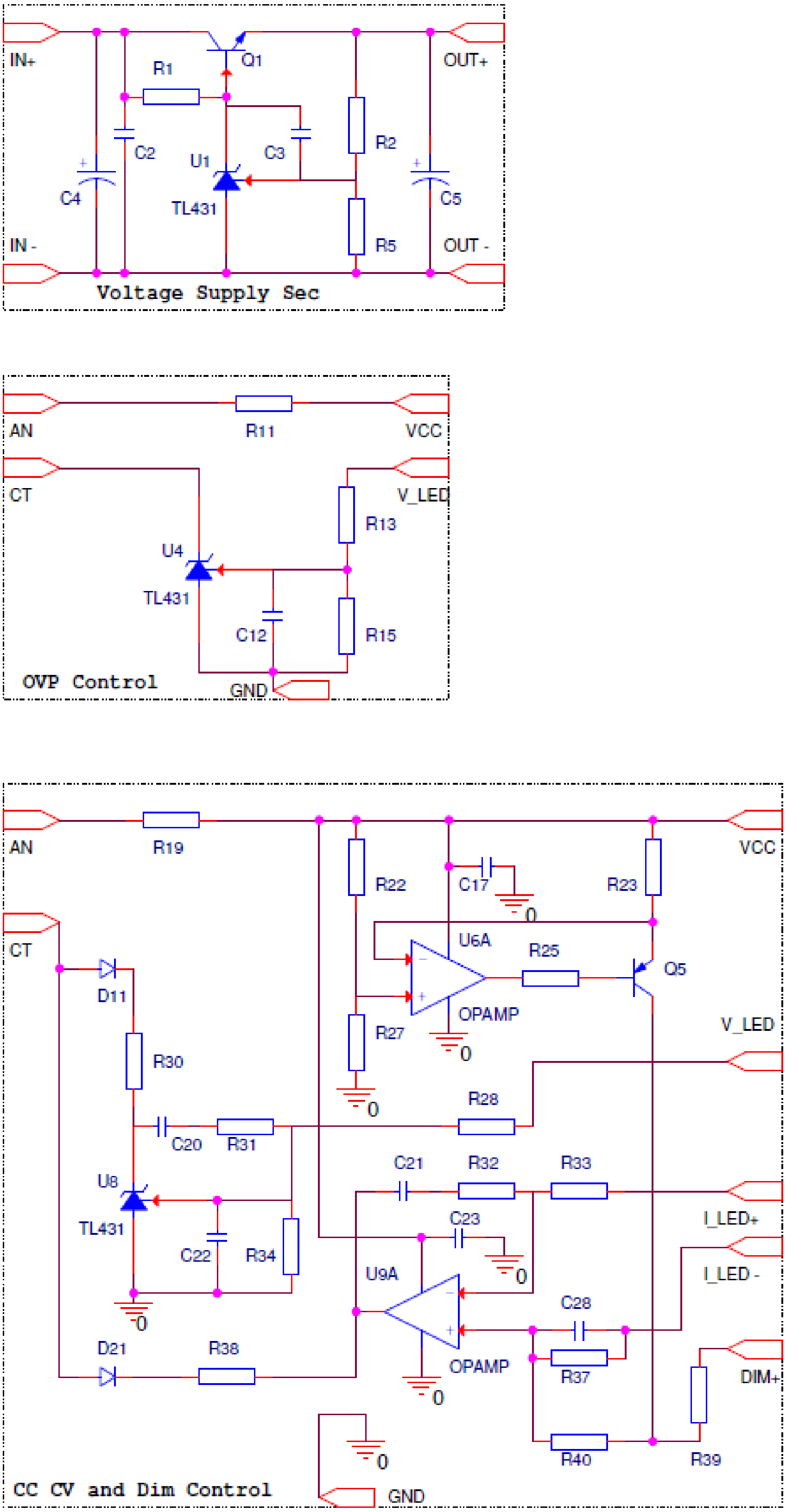


Figure 6. **Typical application schematic (part 2)**



8 Architecture

The PFC and LLC external MOSFETs gates are managed by the “State Machine Event Driven” (SMEDs): 2 for PFC (PFC SMEDs) and 2 for LLC (LLC SMEDs).

The SMEDs are programmable state machine driven by events:

1. External events
2. Analog comparators outputs
3. Power manager generated events (protections)
4. Internal events
5. Timers events

PFC SMEDs

- Inputs events: PFC RECOT, PFC OC1, PFC ZCD
- Outputs: PFC_GD

LLC SMEDs

- Inputs events: LLC ZCD
- Outputs: LVG, HVG

The **μP subsystem** manages dynamically the control loop.

- Analog comparators thresholds setting
- SMED configuration
- SMED timers
- ADC scheduler
- Interrupt management

The multichannel **ADC** is controlled by a programmable event driven scheduler: sampling sequence can be configured and every sample can be triggered by a specific SMED state occurrence and an internal timer value. Different priorities can be programmed to allow fast sampling for real time control and slow sampling for state control.

The scheduler can be programmed to generate interrupts after completion of selectable conversions.

A dedicated **AC line monitor** easily follows the AC line providing system triggers.

The uP reads data from the ADC and performs the loop calculation with the support of a dedicated 16-b x 16-b multiplier and a 32-b accumulator unit.

A **Power management and burst-mode machine** manages the system power state in order to have very low idle consumption and fast activity restart during the burst-mode operation.

Hard protections are managed with a very low propagation delay; the protection enable and the latched/not latched response are programmable. If not specified, the duration of autorestart timer for not latched response is configurable by one NVM parameter.

The power manager controls also the brown-in/out, VCC charge/discharge and AC monitor.

A **Watchdog** resets the system in case of missed μP signal for a long time.

A **communication peripheral** allows serial communication at startup and during the normal operation for:

- External memory communication for
  - Black box external recording
  - Patch SW upload
- Monitoring
- Internal memory R/W and NVM management
- Test mode

9 Functional description

The main functions are:
- HV startup and VCC management
- Line monitor and protection
- Drivers
- PFC control and fault management
- Resonant HB control and fault management
- Power management
- Communication and configuration

9.1 HV startup and VCC management

The VAC pin voltage can be both:
- a rectified sine wave at 100 Hz/120 Hz
- a DC voltage

The VAC pin is the device supply at the startup.

At the VAC pin a HV DMOS is internally connected to charge the capacitor connected to the VCC pin.

From the VCC pin an internal LDO provides the 5 V VCore for analog and digital circuitry; the digital section is supplied by the internal LDO from the VCORE pin.

At startup, from the HV DMOS the capacitor connected to the VCC pin is charged to provide the power supply to the whole device; then the HV DMOS is turned off.

The VCC pin starts sourcing current to the connected capacitor after about 15 V VAC pin voltage.

The VCC capacitor charge current is limited to 0.75 mA (typ.) during the first charge phase to limit the temperature increase in case the VCC pin is short-circuited at startup. After the VCC pin voltage is above 0.8 V, the charging current rises to 5 mA (typ.).

VCORE pin voltage rises when the VCC pin crosses 8 V (Vcc_{CoreOn}). There is a VCORE overload protection that limits the VCC charging current below 1.3 mA in case the VCORE pin is short-circuited at startup. Then the VCC capacitor charge continues with an average current higher than 6 mA: the current is increased during the time the VAC pin voltage is below 100 V (see Electrical characteristics table, parameter I_{vcc_charge}).

Once the VCC pin crosses the 17 V, Vcc_{On} rising threshold the HV DMOS turns off and the whole device starts working: the uP boots.

If the VCC pin goes below the 8.7 V, Vcc_{Off} falling threshold (UVLO threshold) the uP stops working and the HV DMOS turns on again.

If the VCC pin falls below 7 V ($Vcc_{CoreOff}$) the device stops working and the capacitor connected to the VCORE pin discharges. The VCC pin can rise again only after the voltage on the VCORE pin falls below 1 V.

The worst case average charging current from the 0.8 V to the Vcc_{on} threshold is estimated in 4.6 mA (in case the mains voltage is 115 Vac - 60 Hz) and 4.1 mA (in case the mains voltage is 230 Vac - 50 Hz).

9.2 AC line monitor and protection

A HV voltage divider is internally connected to the VAC pin to generate Vline_sense for the input line monitoring and protection:
- Brown-in/out
- Line synchronization
- Line monitor for PFC control

9.2.1 Brown in/out

Brown-in and brownout functions are implemented based on the Vline_sense information.

The peak, in case of VAC voltage, or its value, in case of VDC voltage, is monitored to enable and disable the PFC. The PFC is enabled when the input pin voltage crosses the brown-in threshold. The PFC is disabled after 77 ms (typ.) the VAC pin has gone below the brownout threshold.

Please consider that the brownout threshold and hysteresis values are guaranteed for AC input only.

In order to improve AC line reading and avoid false brown-in, the HV DMOS is turned on sinking IXCD current for 3 ms in case of brownout. In case the device turns off for brownout, only after 100 ms are the turning-on conditions checked again.

This function can be enabled / disabled through the dedicated NVM bit.

9.2.2 Line synchronization

A dedicated digital peripheral manages the PFC synchronization with the AC line sine wave.

In order to improve AC line reading and synchronization, the HV DMOS is turned on sinking IVAC_HV_SINK current at startup. This function can be enabled / disabled through the dedicated NVM bit.

In case the input line switches from AC to DC the device simulates the line synchronization maintaining the AC input line frequency.

In case the input line is DC voltage at the startup, the device emulates the line synchronization as 60 Hz input line (i.e. half period of about 8.3 ms).

9.2.3 Line monitor for PFC control

A 20 MΩ voltage divider for the AC line monitor is internally connected from the VAC pin to GND.

9.2.4 Vline surge stop

A surge can be detected on the VAC pin (430 V).

During the surge the PFC activity is stopped for one half-cycle.

If a line surge is detected during the PFC soft-start, the system shuts down with a not latched fault.

The surge protection can be enabled / disabled through the dedicated NVM bit.

9.3 Gate drivers

The HVG and LVG are matched drivers. Deadtimes are programmable by the user.

During the burst-mode sleep phase, the HS BOOT capacitor discharges. The burst packets always start with an LVG pulse to recharge the bootstrap capacitor. A fast external bootstrap diode is necessary.

9.4 PFC control and fault management

9.4.1 PFC resources

Table 5. PFC related pins

Pin name	Description	Level	Function
PFC_CS	PFC MOSFET current sense	0-125 mV	6-bit ramp enhanced COT feature
		500 mV	OCP1
		900 mV	OCP2 Fault
PFC_ZCD	PFC auxiliary connection for ZCD detection		
PFC_FB	Reading for PFC Vout estimation	ADC, 10 bit	
VAC	Mains line voltage reading	ADC, 10 bit	
PFC_GD	PFC MOSFET gate driver		

9.4.2 Vin reading

Input line voltage peak (Vin) reading on the VAC pin by the ADC at the AC line peak.

In case a DC is applied, the Vin is read each 8.3 ms if the device starts with a DC input. Otherwise, the sampling period depends on the last AC applied before switching to DC.

9.4.3 PFC output voltage feedback reading

PFC output voltage reading on the PFC_FB pin by the ADC.

9.4.4 PFC OVP comparator

The PFC OVP comparator sets the limit for the PFC output voltage.

It monitors the PFC_FB pin with respect to a fixed 2.33 V threshold.

9.4.5 PFC RECOT comparator

The PFC RECOT comparator implements the TON adjustment for the ramp enhanced constant on-time (RECOT) control.

It monitors the PFC_CS pin with respect to a programmable threshold. Its output communicates to the PFC SMED.

The new THD optimizer is based on this comparator.

9.4.6 PFC OC1 comparator

The PFC OC1 comparator sets the limit for the operational maximum allowed peak current into the PFC MOSFET. If the OC1 threshold is hit the PFC_GD is turned off. This protection works cycle by cycle. It monitors the PFC_CS pin with respect to a fixed 500 mV threshold. Its output communicates to the PFC SMED.

9.4.7 PFC OC2 comparator

The PFC OC2 comparator sets a HW limit for the current flowing into the PFC MOSFET: it triggers the OCP fault.

It monitors the PFC_CS pin with respect to a fixed 900 mV threshold.

9.4.8 PFC ZCD

The PFC ZCD comparator performs the zero cross detection to implement the soft switching of the PFC MOSFET.

It monitors the PFC_ZCD pin with respect to two programmable rising and falling thresholds.

Its output communicates to the PFC SMED.

Please consider that the PFC ZCD feedback disconnection is not implemented.

9.4.9 PFC state machine event driven (SMED)

The PFC high frequency operations are managed by a programmable 8-state ”State Machine Event Driven” (2 coupled 4-state SMEDs).

The SMED controls the PFC MOSFET based on the PFC comparators output and internally controlled counters.

It generates also the comparators' enable signals. It works at 60 MHz.

9.5 PFC algorithm

The PFC operates based on a multi-mode scheme.

A constant on-time (COT) control is implemented; TON is calculated from the PFC feedback and the measured Vin (the peak in case of a VAC, its value in case of a VDC).

T_{ON} is calculated and updated at the line cycle valley in case of VAC input, otherwise the system executes the TON calculation each 8.3 ms (in case the device starts with DC input).

Based on the working PFC's operating state variables, the working mode is changed to optimize the overall efficiency.

The device includes an automatic bulk voltage drop management: during running operation, in case the PFC_FB pin is below 31 LSB with respect to the target, the device boosts the PFC output changing automatically the control loop parameters (only during the management of the drop).

9.5.1 Ramp enhanced COT improved (patented)

The PFC control is based on the constant on-time scheme, with a proprietary improved algorithm: the calculated TON is applied only after the PFC RECOT comparator is triggered to balance the recovery diode energy and the EMI capacitor current.

The PFC RECOT comparator threshold is adjusted by the core with a 6-bit DAC and allows to apply the programmed base and ramp (defined by user into NVM).

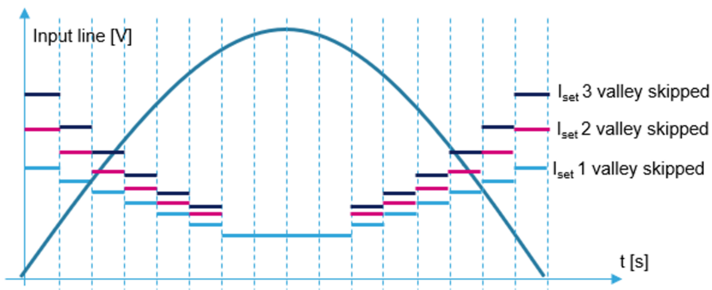
This feature allows improving the total harmonic distortion (THD) and the power factor (PF) of the application.

9.5.2 New THD optimizer (patented)

The device implements the new THD optimizer algorithm that can be enabled/disabled by the NVM. This new (patented) algorithm is based on the enhanced COT:

The PFC RECOT comparator threshold is adjusted by the core with a 6-bit DAC but, instead of constant threshold, the DAC value depends on both the phase of the AC input line and on the mode of the PFC.

Figure 7. New THD optimizer algorithm example



The user can fine tune the algorithms by the related NVM parameters.

9.5.3 Operating modes

The PFC manager changes the operating modes by dynamically reconfiguring the SMEDs, obtaining optimal performances in terms of both efficiency and THD/PF.

- Transition mode (TM mode)
- Valley skipping
- Discontinuous mode (DCM)

9.6 PFC protections

9.6.1 PFC OVP

The device includes two different PFC OVP protections: hardware (based on PFC_OVP comparator) and software (based on ADC PFC_FB sampling). In both cases, if the PFC OVP protection is triggered during the running state of the PFC, the device turns off the PFC until the next line valley. The HW OVP threshold is fixed, the SW OVP threshold is an NVM parameter.

Please see the PFC_CS disconnection paragraph for information about PFC_OVP and PFC_CS disconnection.

The device shuts down for PFC_OVP only if all the following three conditions are triggered:

- the PFC_OVP HW comparator is triggered during the PFC startup
- the feedback disconnection faults are enabled
- PFC_CS comparator is not triggered during PFC start-up phase

Please consider that in all other cases the device does not enter fault state so the half-bridge input voltage could be higher than the PFC_OVP HW threshold with the output still in regulation.

9.6.2 PFC OCP2

If the PFC OC2 comparator is triggered, the PFC gate is truncated and remains off until the beginning of a new line half cycle. In case the PFC OC2 comparator is triggered for more than a programmable number of consecutive half line cycles, the device enters the OCP2 fault and it is turned off.

The OCP2 fault can be programmed as latched or not latched.

9.6.3 PFC soft-start timeout

If the PFC soft-start is not finished after 1 s the system enters the PFC soft-start timeout fault state and it is turned off. The fault is not latched.

9.6.4 PFC UVP

If the PFC_FB pin is below a programmable threshold for more than about 600 us, the device enters the PFC UVP fault and it shuts down. The PFC UVP fault is a not latched fault.

In case the LLC is in running state and the PFC UVP is triggered, the not latched timer depends on the related NVM parameter and could be set to either:

- 100 ms

or

- Programmable autorestart timer for not latched fault

In case the PFC UVP is triggered and the LLC is not in running state (i.e. soft-start or ACP management state), the duration of not latched timer is set to the programmable autorestart timer for not latched fault.

9.6.5 PFC_FB disconnection

It could be enabled/disabled by NVM parameter.

If the PFC_FB is stuck low the system enters the PFC_FB disconnection fault state (latched) and it is turned off.

9.6.6 PFC_CS disconnection

It could be enabled/disabled by NVM parameter. If enabled, the PFC_CS disconnection fault protection is latched.

In case the PFC_CS is stuck high during the operative mode, the device enters the PFC_CS disconnection protection and it is turned off.

In case the PFC_CS pin is stuck low (or high) during the PFC start-up phase, the device enters the PFC_CS disconnection protection and it is turned off.

In particular, during the start-up phase if the disconnection faults detection is enabled and the PFC_OVP is triggered, the device behavior depends on the following cases:

- If the voltage of PFC_FB pin is between PFC_FB target and HW PFC_OVP threshold:
  - AC CASE: as long as the PFC_CS is not triggered, after the 45° input line phase, the system turns on the PFC gate for a few pulses about every 0.6 ms.
  - DC CASE: if the PFC_CS is not triggered the system turns on the PFC gate for a few pulses before entering the soft-start phase.

in both cases, if the PFC_CS comparator is not triggered during the start-up phase and the feedback disconnections are enabled, the device turns off entering PFC_CS disconnection fault protection.

- If the voltage of PFC_FB pin is above the HW PFC_OVP threshold:
  - in case the PFC_CS is not triggered the device turns off entering PFC_OVP fault protection (not latched).

9.7 LLC control and protection

9.7.1 LLC related resources

Table 6. LLC related pins

Pin name	Description	Level	Function
LLC_CS	Low-side current sense	0-500 mV	5 bit OLP
		700 mV	OCP2 fault
LLC_AUX	LLC auxiliary winding voltage sense	0.9 V	External burst mode
		2.5 V	LLC output OVP
LLC_FB	LLC OPTO feedback sense, burst comparator and SHUTDOWN comparator	ADC, 10 bit	Feedback sense
		Programmable	Burst comparator
		125 mV	Shutdown comparator
HVG	High-side gate driving		
LVG	Low-side gate driving		

9.7.2 LLC OC1 comparator

The LLC OC1 comparator implements the overload protection (OLP). It monitors the LLC_CS pin with respect to a programmable threshold. If the LLC_CS pin goes every cycle over the OC1 threshold for a programmable time, the IC shuts down and enters the OLP fault.

Both threshold and duration are programmable trough NVM parameters.

9.7.3 LLC OC2 comparator

The LLC OC2 comparator sets a HW limit for the current flowing into the LLC resonant tank: it triggers the OCP2 fault.

It monitors the LLC_CS pin with respect to a fixed 700 mV threshold. If this threshold is triggered for a programmable consecutive number of cycles, the OCP2 fault is triggered and the system shuts down.

9.7.4 LLC ZCD comparator

The LLC ZCD comparator detects the LLC current zero-crossing during the normal operation to implement the time-shift control and the anti-capacitive protection.

Its output communicates to the LLC SMED.

The comparator’s hysteresis is programmable by NVM choosing between the available values 5 mV or 10 mV. It is recommended to use the 10 mV hysteresis.

9.7.5 LLC_FB voltage reading: OPTO feedback loop error

The LLC_FB pin is connected to the optocoupler and its voltage is the error signal of the LLC loop.

The LLC_FB voltage is sampled by the ADC to calculate the time-shift.

9.7.6 Shutdown feature

If the LLC_FB pin is forced below 125 mV, the device shuts down. If the voltage returns over such threshold the system restarts performing the soft-start.

This feature can be enabled / disabled using an NVM bit.

9.7.7 SMEDs

HVG and LVG are driven by an event driven 60 MHz state machine (2 coupled 4-state SMEDs).

Driving events are the ZCD event and the elapsing of the programmable time which sets the high-side and low-side time-shift values and drivers deadtime.

9.7.8 Algorithm

The LLC operation is based on “Symmetric Time-Shift Control” (STSC), an improved version of time-shift control that guarantees 50% of the HB duty cycle. The time-shift value is calculated from the LLC_FB pin.

9.7.9 Time-shift (patented)

The TSC methodology consists in controlling the amount of time elapsing from a zero crossing of the tank current to the switch-off of the MOSFET currently on.

Conceptually, with TSC an inner loop is closed and the outer loop that regulates the output voltage provides the reference for the inner loop. This inner loop is completely managed by SMEDs using the zero current detection information.

9.8 LLC protections

9.8.1 Anti-capacitive protection

Anti-capacitive control is applied at the SMEDs level using ZCD time events.

The IC monitors the phase relationship between the LLC tank current sensed on the LLC_CS pin and the voltage at the HVG and LVG, checking the time between the gate rising edge and the tank current zero cross detection.

If this time is below a programmable threshold, which is indicative of impending capacitive-mode operation, the monitoring circuit activates the “Soft” ACP procedure: the time-shift is reduced (and therefore the switching frequency is increased) in order to keep the converter away from that dangerous condition.

If the time reaches “zero” the device is stopped immediately. This is called “Hard” ACP.

Both hard and soft ACP can be enabled and disabled through NVM.

9.8.2 LLC OLP

If the LLC OC1 comparator is triggered the system could enter the overload protection (OLP). During this phase the system regulates the output and checks for a programmable time if the OCP1 event is still present, in this case the device is shut down entering the OLP fault state that can be programmed as latched or not latched.

9.8.3 LLC OCP2

If the LLC OC2 comparator is triggered for a number of times greater than a threshold set by the user, the device sets the OCP2 fault and it is shut down. The OCP2 fault can be programmed as latched or not latched.

9.8.4 LLC soft-start timeout

If the LLC output voltage cannot reach the regulation value within 100 ms, the device enters the LLC soft-start timeout fault and it is shut down. The fault can be programmed as latched or not latched.

9.8.5 LLC OVP

If the LLC_AUX pin voltage is higher than the LLC OVP comparator threshold (2.5 V) the system enters the LLC OVP fault state and it is turned off. The fault can be programmed as latched or not latched and can be disabled.

The autorestart timer is set to about 34 ms in case not latched chosen.

9.8.6 LLC_CS disconnection

If the LLC_CS pin is stuck at 0 V or 5 V during the soft-start the system enters the LLC_CS disconnection fault (not latched) and it is shut down if the disconnection faults detection is enabled in NVM.

9.8.7 LLC_AUX disconnection

If the pure external burst-mode is enabled and the LLC_AUX pin is stuck at 0 V during the burst and the LLC_FB pin is higher than the burst comparator threshold, after 32 burst packets the system enters LLC_AUX disconnection protection (latched) and it is shut down if the disconnection faults detection is enabled in NVM.

9.9 ADC

The system ADC is an 8-channel 15-MHz SAR 10-bit A/D converter.

It needs 7 cycles (470 ns) for sampling and 11 cycles (740 ns) to convert the data.

It is controlled by an SW programmable scheduler allowing flexible system signals reading:

- Fixed time sequence conversion
- Event driven sequence conversion

Table 7. **ADC input signals**

Signal	Pin	Internal voltage divider	FST
Input line voltage	VAC	Internal voltage divider	484.5 V
PFC feedback voltage	PFC_FB	Direct reading	2.5 V
LLC feedback voltage	LLC_FB	Direct reading	2.5 V

9.10 Burst-mode

9.10.1 Specific resources

Burst comparator on LLC_FB pin

The LLC BURST comparator at the LLC_FB pin is used to wake up the system, in order to perform a burst sequence.

The comparator is alive also during sleep and the wake-up threshold is programmable (0.75 V, 1 V, 1.25 V).

External burst-mode comparator on LLC_AUX pin

The external burst-mode comparator with the 0.9 V threshold on the LLC_AUX pin is used to enter / exit the burst-mode using an external digital signal. The external burst-mode operation can be enabled / disabled using a NVM bit.

30-kHz system oscillator

A 30-kHz oscillator (always on) keeps the system alive.

9.10.2 Algorithm

The system can manage the deep sleep state with very low VCC current consumption (500 μA).

The system in deep sleep

- Monitors the AC line for brownout condition
- Monitors the burst comparator to detect wake condition
- Monitors the VCC for data integrity
- Maintains all RAM data

The device implements two different burst-mode algorithms: the LLC_FB burst or external burst. The first one is based on just the LLC_FB pin voltage, the second one is based on the external BM comparator on the LLC_AUX pin that can be driven sensing the output current.

The burst-mode can be programmed to depend either on the LLC_FB pin only, or LLC_AUX pin only, or both. This third possibility is called hybrid external burst.

In case of the LLC_FB burst-mode, the device enters sleep mode if the LLC_FB pin voltage goes below a programmable threshold. The burst switching activity is enabled after the burst comparator is triggered.

The normal switching activity is restored if the time between two bursts is lower than a programmable threshold. This time defines a precise power level at which the controller exits the burst-mode. In order to have a faster response to the big load transient the system exits burst-mode also if the LLC_FB pin voltage is still above the burst comparator threshold after one burst packet.

In case of the LLC_AUX pin driven burst-mode, two types of external burst mode could be

defined:

- Pure external burst-mode: only the external BM comparator manages the burst-mode entering / exiting;

- Hybrid external burst-mode: if the external BM comparator is high, the system stays out of burst-mode while if the external BM comparator is low, burst-mode entering / exiting is managed by the LLC_FB pin settings.

In both external burst-mode cases, the burst switching activity is anyway managed by the LLC_FB pin and the burst comparator.

The PFC and LLC switching activities during the burst-mode are synchronized.

The LLC can perform a burst without the PFC, depending on the system conditions.

9.11 Communication and configuration

The device communicates with an external digital device through a serial interface.

The serial interface uses two dedicated pins with a standard UART protocol. It implements also an I^2C protocol for external E^2PROM writing and reading.

The serial interface allows the user

- To write the NVM to configure the device in a specific application: 24 bytes are available
- To write into the RAM for test and SW patch purposes
- To read the NVM content
- To read the RAM content
- To read registers content
- To configure the device for specific tests

Based on a specific code into the NVM the serial interface functionality can be reduced for security reasons.

9.11.1 Monitor

Some internal data can be provided to an external digital device through the UART interface for monitoring purposes.

9.11.2 Black box

Black box data are written into the external E^2PROM (if present) during the normal operation.

9.11.3 Patches

SW patches (if necessary) are uploaded by the device from the external E^2PROM at the startup. It can be enabled/disabled using a NVM bit for security reasons.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO20 package information

Figure 8. SO20 package outline

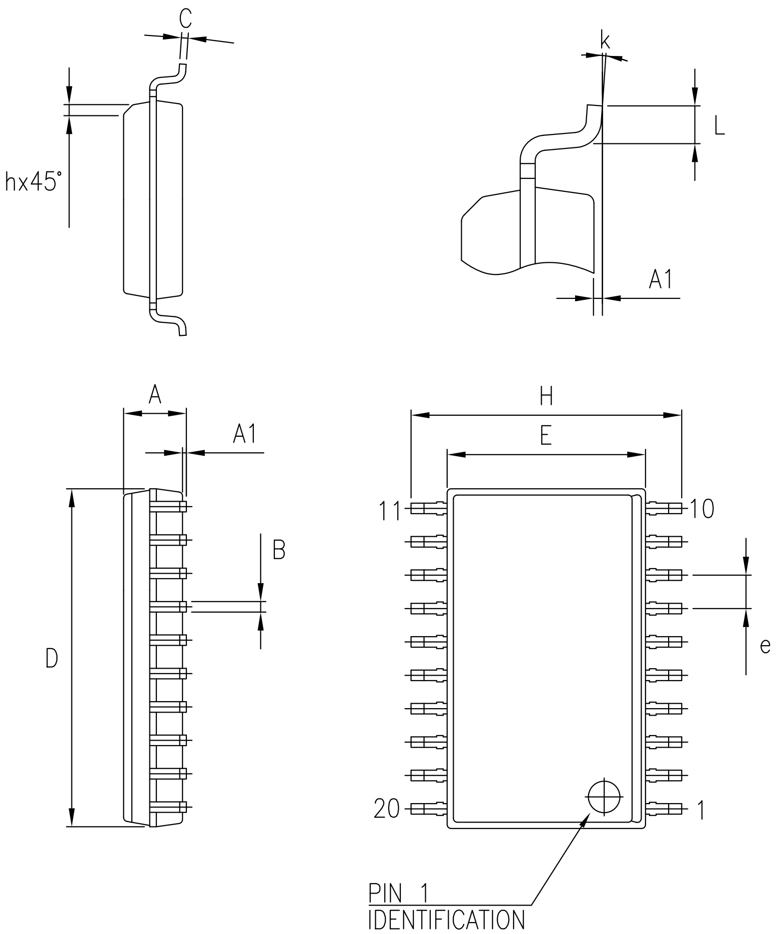


Table 8. SO20 package mechanical data

Symbol	Dimension					
	mm			Inch		
	Min.	Typ.	Max	Min.	Typ.	Max.
A	2.35	-	2.65	0.093	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
B	0.33	-	0.51	0.013	-	0.020
C	0.23	-	0.32	0.090	-	0.013

Symbol	Dimension					
	mm			Inch		
	Min.	Typ.	Max	Min.	Typ.	Max.
D	12.60	-	13.00	0.496	-	0.512
E	7.40	-	7.60	0.291	-	0.299
e	-	1.27	-	-	0.050	-
H	10.00	-	10.65	0.394	-	0.419
h	0.25	-	0.75	0.010	-	0.030
L	0.40	-	1.27	0.016	-	0.050
K	0° (min.), 8° (max.)					

11 Ordering information

Table 9. Order codes

Part number	Package	Packing
STNRG012	SO20	Tube
STNRG012TR	SO20	Tape and reel

Revision history

Table 10. Document revision history

Date	Version	Changes
23-Feb-2021	1	Initial release.

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