Reference Design:

HFRD-29.12

Rev 1; 12/09

REFERENCE DESIGN

Dual-Rate (1.25Gbps/10.3125Gbps) VCSEL SFP+ Transceiver with DS1874 Controller

maxim integrated™

Dual-Rate (1.25Gbps/10.3125Gbps) VCSEL SFP+ Transceiver

Table of Contents

1 Overview

High-Frequency Reference Design (HFRD-29.12) is a complete optical transceiver targeted for the small form-factor pluggable (SFP+) Multisource Agreement (MSA) market and other high-speed optical-transceiver applications.

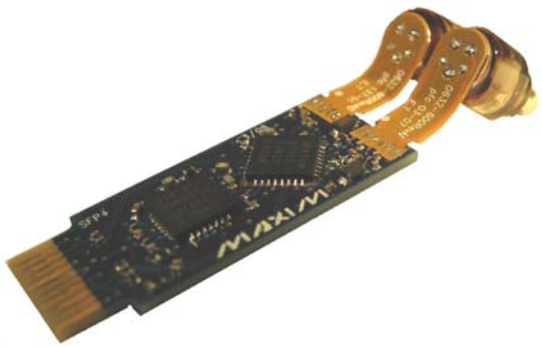
This design showcases the MAX3799 combination differential VCSEL driver and limiting amplifier. The MAX3799 limiting amplifier is optimized to provide standards-compliant sensitivity at data rates of either 1.25Gbps or 10.3125Gbps. The reference design is available with a variety of VCSEL (TOSAs) and receivers (ROSAs). Control of the MAX3799 is provided by the DS1874 SFP+ controller. The DS1874 interfaces to the MAX3799 with a 3-wire digital interface, and is used to regulate optical power, monitor functions, and control other MAX3799 settings. Communication with the SFP+ module is accomplished through the standard MSA I^2C interface.

The MAX3799 is a cost-effective solution for an SFP+ dual-rate transceiver. Combining the VCSEL driver and limiting amplifier into a single, 5mm x 5mm package reduces cost without compromising performance. Mask margins in excess of 40% at 10.3125Gbps are achievable.

The HFRD-29.12 transceiver reduces design time for SFP+ and other optical transmitters by providing the schematics, PC-board layout, Gerber files, and bill of materials. The module is provided with some basic firmware and a graphical user interface (GUI) to demonstrate the operation of the MAX3799. Test data and typical performance from an assembled board also aid in evaluating this reference design.

1.1 Features

- Schematics and Bill of Materials provided
- Gerber plot files available
- Dual-rate compliant (1.25Gbps or 10.3125Gbps)
- Single +3.3V power supply
- SFP+ multisource footprint
- Digital diagnostic monitors
- 850nm wavelength LC VCSEL (TOSA) and receiver (ROSA) provided
- DS1874 eliminates need for firmware
- Basic GUI provided with sample



2 Obtaining Additional Information

Limited quantities of the HFRD-29.12 SFP+ transmitter board and HFRD-30.1 SFP host board (see section 6.4) are available. For more information about this reference design or to obtain an SFP+ transmitter or host board, please access our customer support at: https://support.maxim-ic.com.

3 Reference-Design Details

3.1 Components

3.1.1 MAX3799 Laser Driver/Limiting Amp

The MAX3799 is a combination VCSEL driver and limiting amplifier with a 3-wire digital-control interface.

The laser driver portion has many registers and features, including:

1. Waveform peaking
2. Pulse-width fine adjustment
3. Control of bias and modulation
4. Soft and hard limits on bias and modulation
5. Driver back termination
6. Full differential drive
7. Up to 12mA modulation
8. Fault detection capability

The limiting amplifier features:

1. Adjustable-output CML level
2. Adjustable-output slew rate
3. Input-bandwidth select feature
4. Output pre-emphasis enable
5. 5mV input sensitivity
6. LOS polarity/squelch
7. Programmable LOS level

For additional information, see the MAX3799 data sheet, available on the Internet at: www.maxim-ic.com/MAX3799.

3.1.2 DS1874 SFP+ Controller

The DS1874 contains all of the features and input/output connections to control and monitor the MAX3799 functions.

The DS1874 performs the following tasks:

1. I^2C interface to host board
2. 3-wire digital interface to the MAX3799
3. Monitor and control of VCSEL power
4. Diagnostic monitoring
5. Control of all MAX3799 registers
6. Fault monitoring

The DS1874 controls and monitors all functions for the SFP+ module including all SFF-8472 functionality. The combination of the DS1874 with MAX3799 provides APC loop, modulation current control, and eye-safety functionality. Six ADC channels monitor VCC, temperature, and four external monitor inputs (MON1-MON4) that can be used to meet all monitoring requirements.

The DS1874 eliminates the need to design and write additional firmware that would be required in a microprocessor-based design. The DS1874 includes all of the necessary registers, diagnostic monitoring, and functions to provide SFP compliance.

3.1.3 VCSEL (TOSA)

HFRD-29.12 is available with one of three VCSEL brands:

JDSU™ PL-FLD-00-S40-C5 www.jdsu.com

EMCORE®:8585-3760 www.emcore.com

Finisar®: HFE6192-261 www.finisar.com

All VCSELs are provided with flex circuit interconnect and packaged in LC headers.

3.1.4 Receive Optical Subassemblies (ROSA)

HFRD-29.12 can be provided to the customer with either of these ROSA brands:

Finisar: HFD 6180-418 or 6180-419

JDSU: PL-FLR-00-S43-C6

3.2 Functional Block Diagram

The functional block diagram is shown in Figure 1. The 20-pin SFP+ electrical interface is shown on the left portion of the diagram. The TOSA and ROSA are located to the right of the MAX3799. A simple, but effective, RC equalizer is included on the Tx data input lines to help compensate for the jitter added by the edge connector. The TX_DISABLE function is controlled through the DS1874.

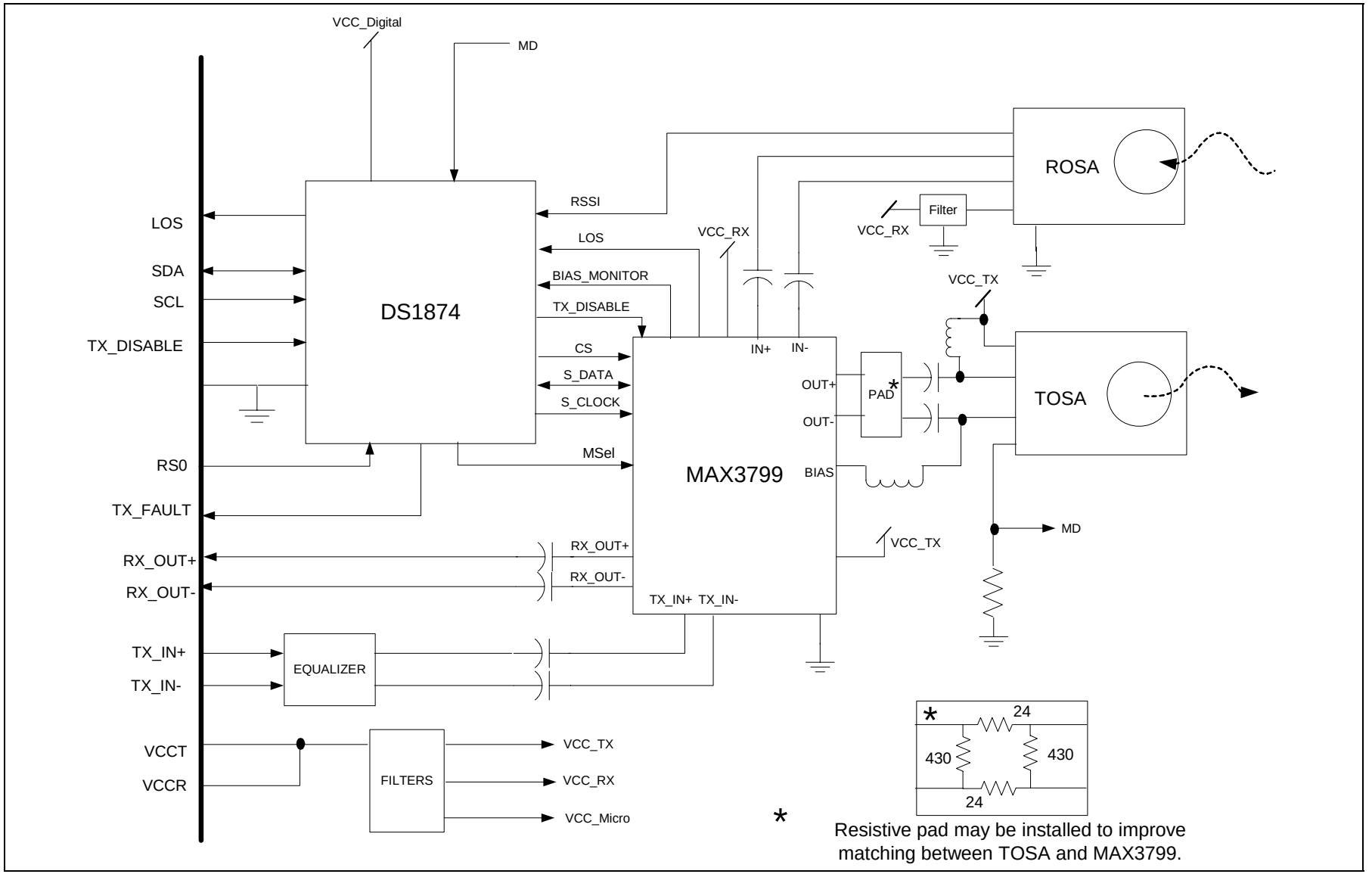
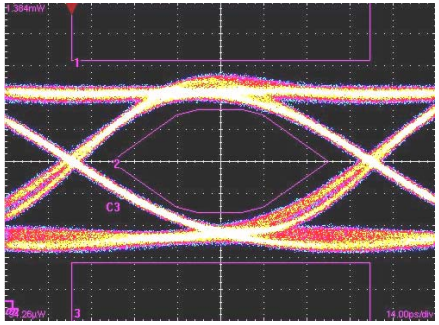
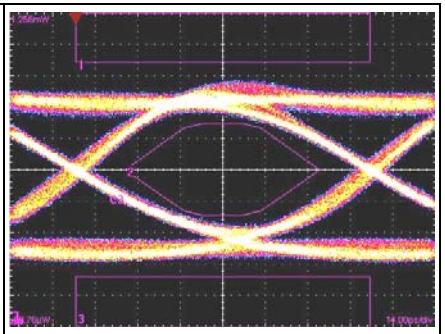
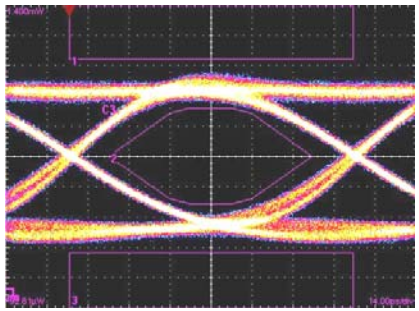
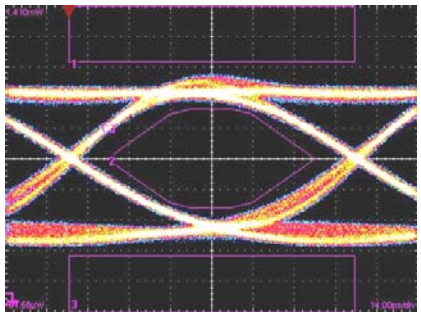
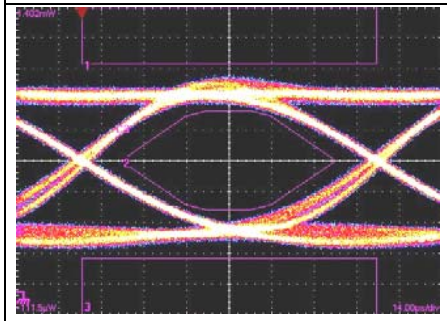
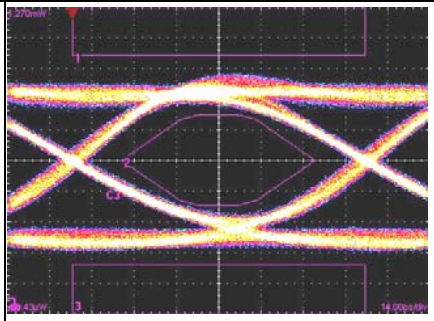


Figure 1. Functional diagram.

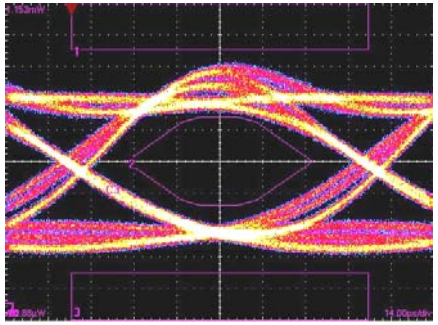
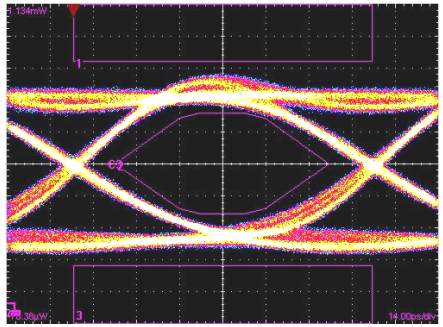
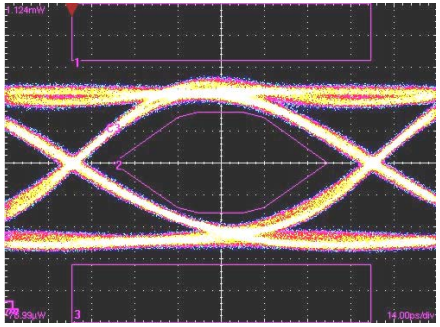
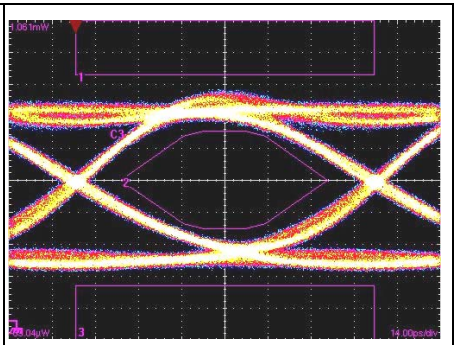
4 Transmitter Performance Data

4.1 Filtered Transmit Eye Diagrams at 10.3125Gbps, PRBS 2^{31}-1 (JDSU VCSEL shown)

 Mask margin: 46%			 Mask margin: 33%	2.95V
Peaking adjustment: none (0) Modulation level: manually adjusted at each temperature to maintain relatively constant extinction ratio. APC loop: operational, bias automatically adjusts to maintain constant power; bias limit set to 9mA. Pad: 0dB (see Figure 1)	 Mask margin: 44%	 Mask margin: 46%		3.3V
 Mask margin: 46%			 Mask margin: 33%	3.65V
0°C	+25°C	+50°C	+85°C	

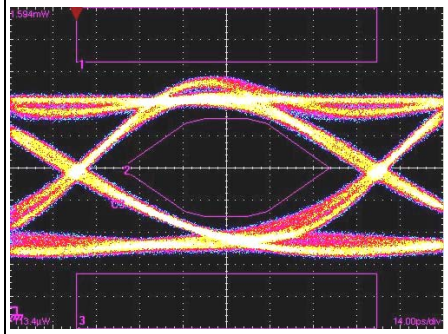
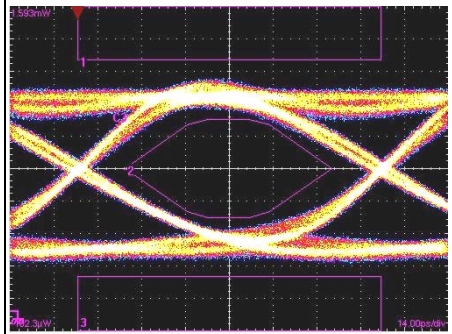
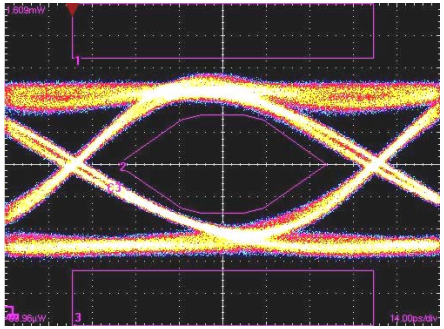
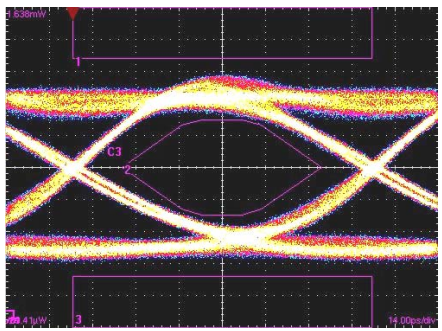
4.2 Filtered Transmit Eye Diagrams at 10.3125Gbps vs. Temperature (Finisar and EMCORE VCSELs shown)

Finisar VCSEL

			
Mask margin: 26%	Mask margin: 44%	Mask margin: 44%	Mask margin: 39%
0ºC	+25ºC	+50ºC	+85ºC

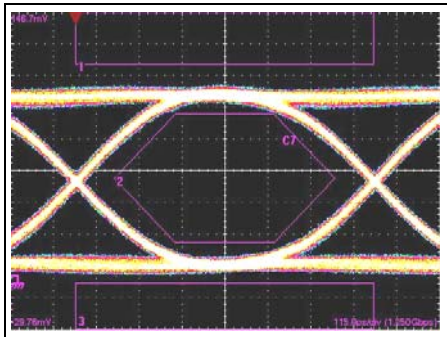
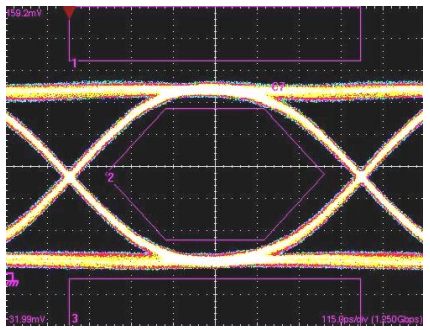
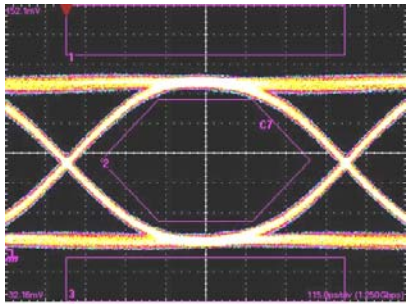
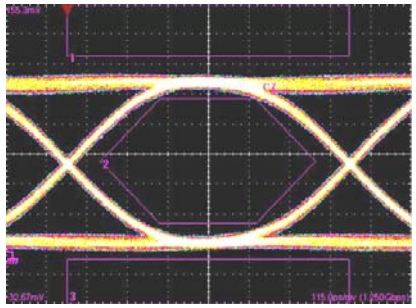
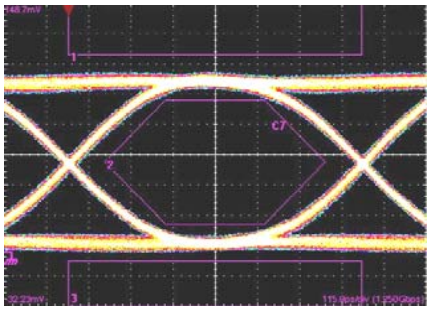
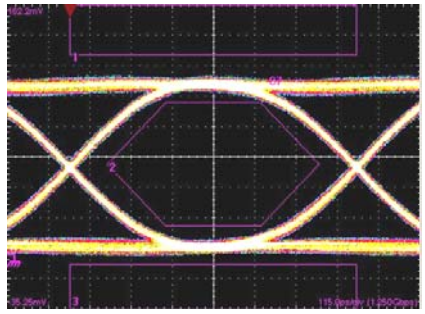
Peaking adjustment: none (0) Pad: 4dB Modulation level: manually adjusted to maintain relatively constant extinction ratio

EMCORE VCSEL

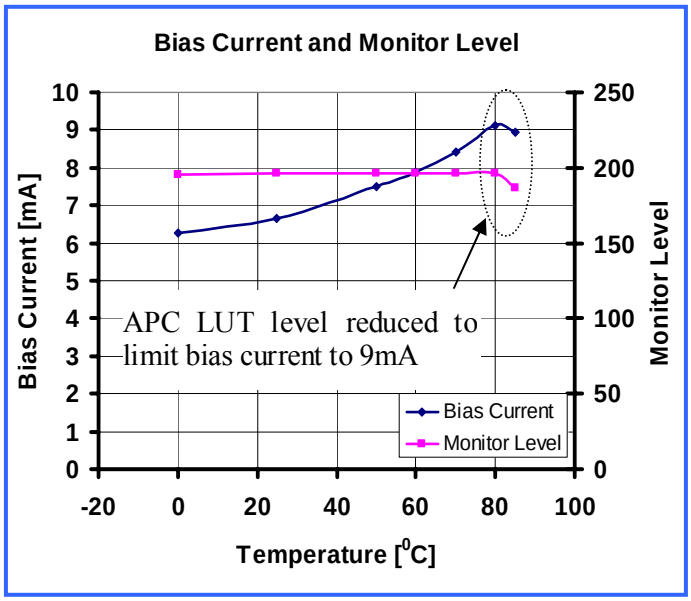
			
Mask margin: 39%	Mask margin: 37%	Mask margin: 39%	Mask margin: 34%
0ºC	+25ºC	+50ºC	+85ºC

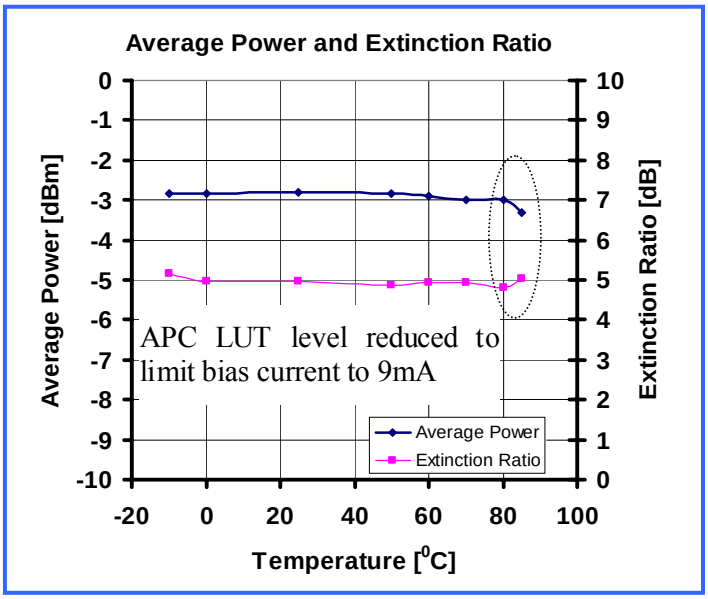
Peaking adjustment: none (0) Pad: 4dB Modulation level: manually adjusted to maintain relatively constant extinction ratio

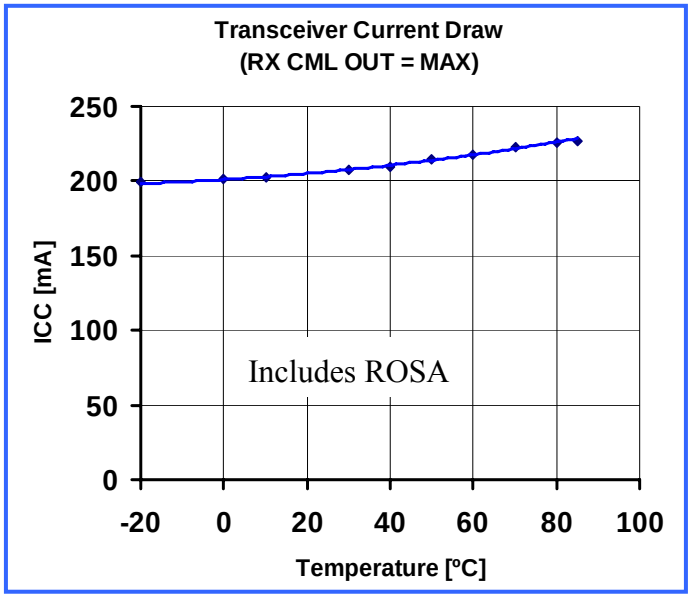
4.3 Filtered Transmit Eye Diagrams at 1.25Gbps, PRBS 2^7-1 (JDSU VCSEL shown)

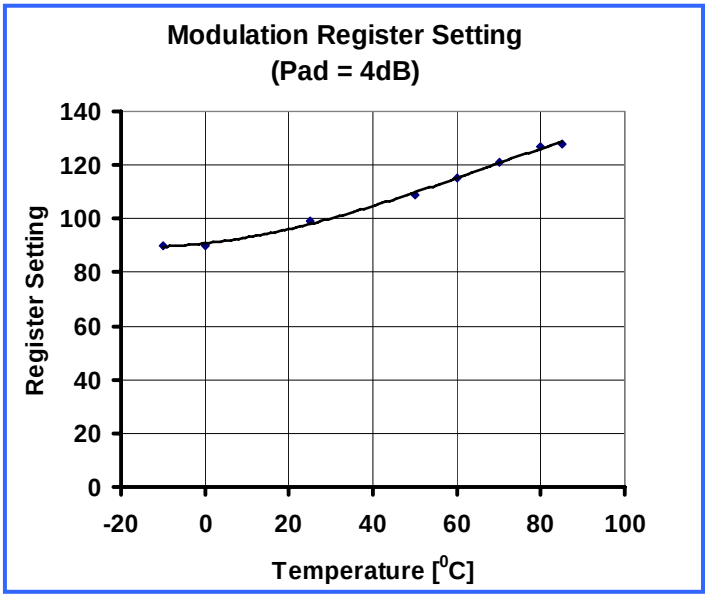
 Mask margin: 44%			 Mask margin: 4%	2.95V
Peaking adjustment: none (0) Modulation level: manually adjusted at each temperature to maintain relatively constant extinction ratio. APC loop: operational, bias automatically adjusts to maintain constant power; bias limit set to 9mA. Pad: 4dB (see Figure 1)	 Mask margin: 44%	 Mask margin: 46%		3.3V
 Mask margin: 44%			 Mask margin: 41%	3.65V
0°C	+25°C	+50°C	+85°C	

4.4 Additional Transmitter Data at 10.3125Gbps (Finisar VCSEL shown)









5 Receiver Performance Data

5.1 Receiver Output Eye Diagrams at 10.3125Gbps, 2^{31}-1 PRBS, -10dBm Input OMA, Nonstressed Source

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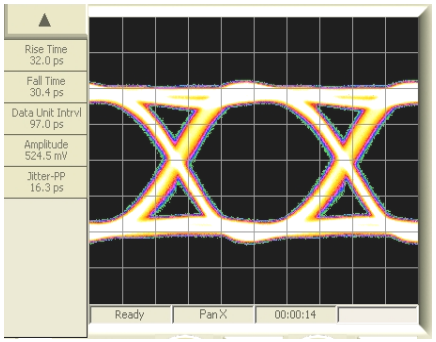
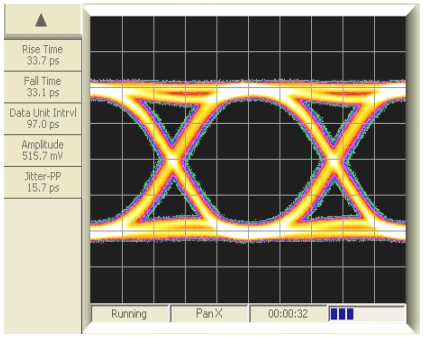
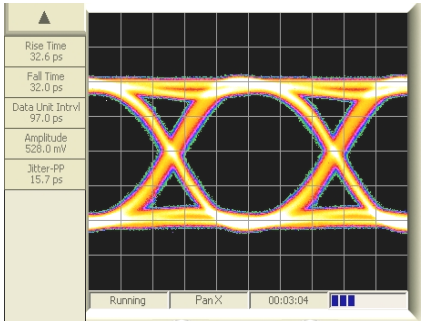
<td> 
</td>
<td>(Finisar ROSA shown)

RS0: high bandwidth (1)

Output De-emphasis: ON

CML Level: 150</td>
<td></td>
<td> 
</td>
<td>2.95V</td>
</tr>
<tr>
<td>Output eyes include jitter from:
Reference transmitter
15 feet of 50µm fiber
Host-board edge connector
3 feet of coax cable
BERT SCOPE</td>
<td> 
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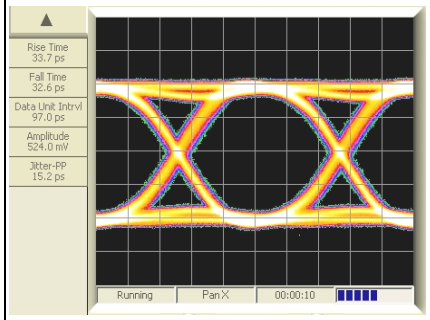
<td> 
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<td></td>
<td>3.3V</td>
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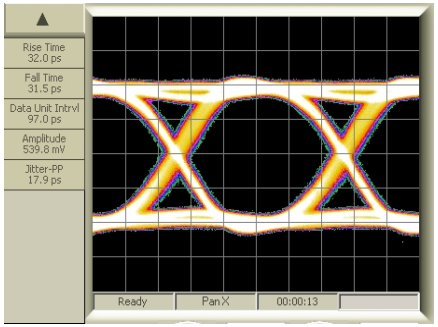
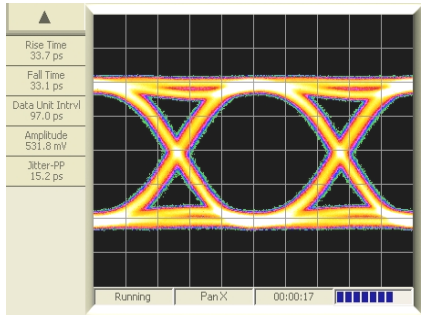
<td> 
</td>
<td>(Finisar ROSA shown)</td>
<td></td>
<td> 
</td>
<td>3.65V</td>
</tr>
<tr>
<td>0 °C</td>
<td>+30 °C</td>
<td>+50 °C</td>
<td>+85°C</td>
<td></td>
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5.2 Receiver Output Eye Diagrams at 1.25Gbps, 2^7-1 PRBS, -15dBm Input OMA, Nonstressed Source

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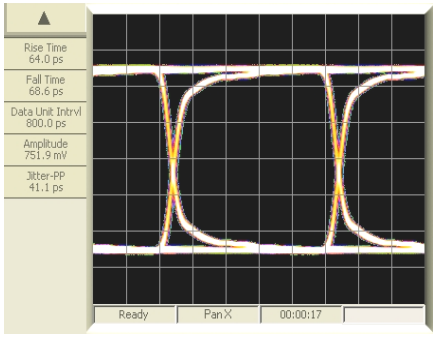
<td> 
</td>
<td>(Finisar ROSA shown)

RS0: low bandwidth (0)

Output De-emphasis: OFF

CML level: 150</td>
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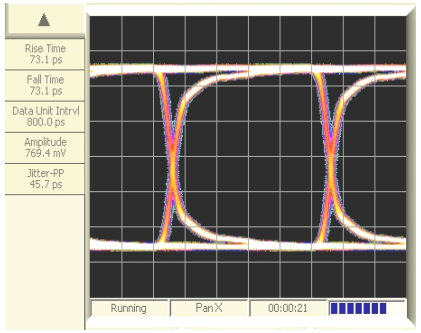
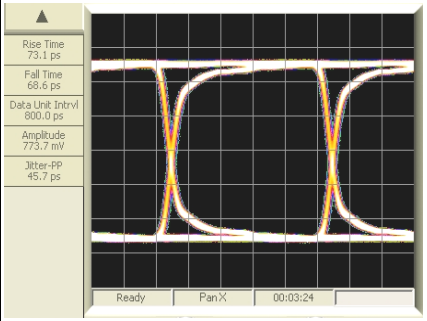
<td> 
</td>
<td>2.95V</td>
</tr>
<tr>
<td>Output eyes include jitter from:

• Reference transmitter
• 15 feet of 50µm fiber
• Host-board edge connector
• 3 feet of coax cable
• BERT SCOPE</td>
<td> 
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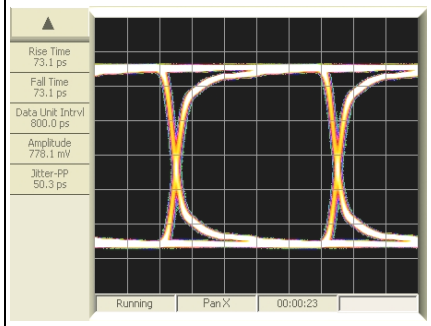
<td> 
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<td>3.3V</td>
</tr>
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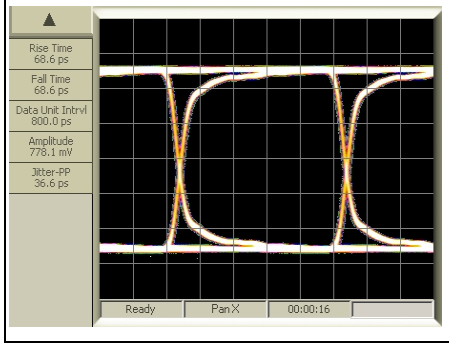
<td> 
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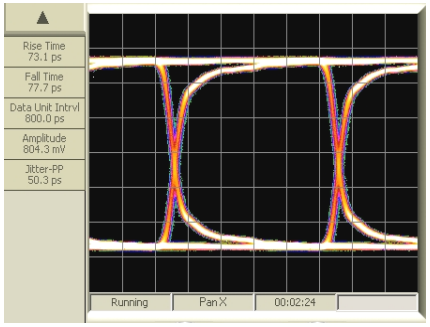
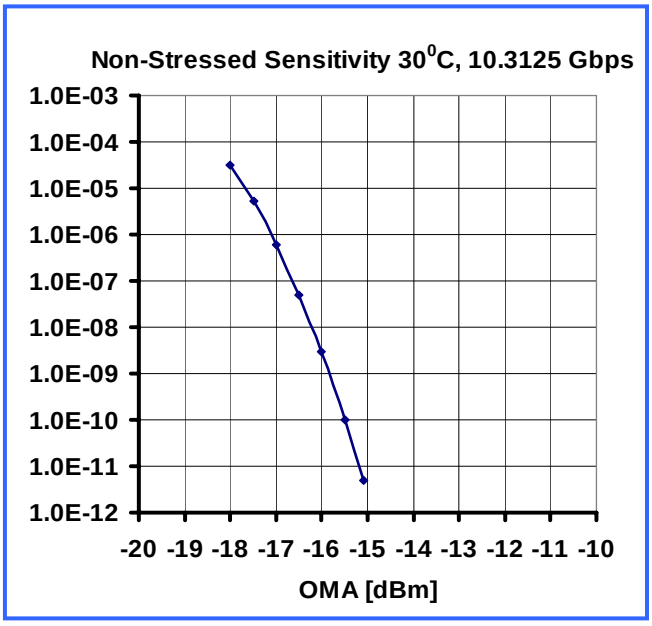
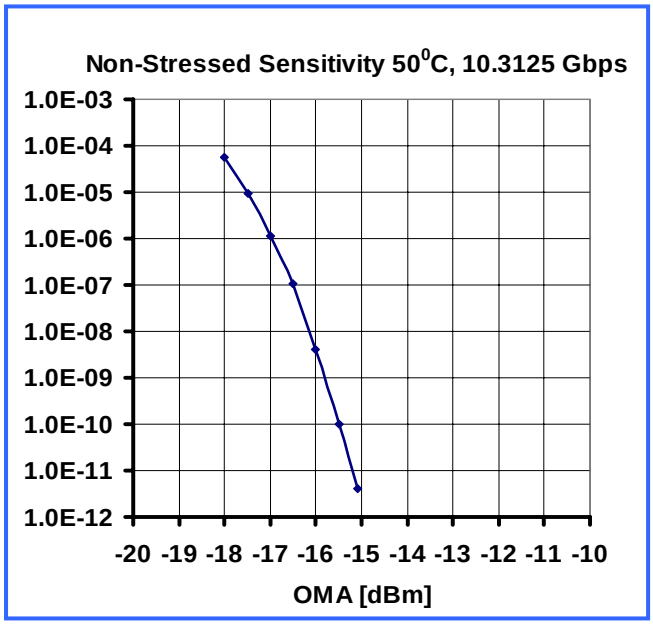
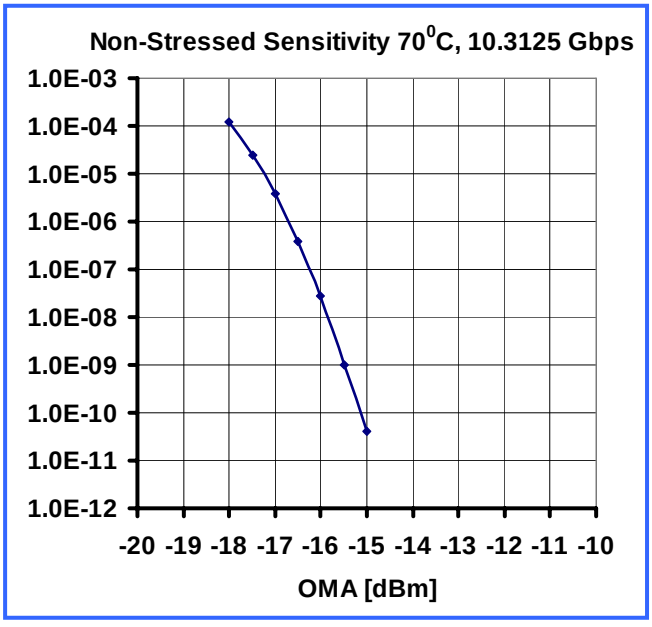
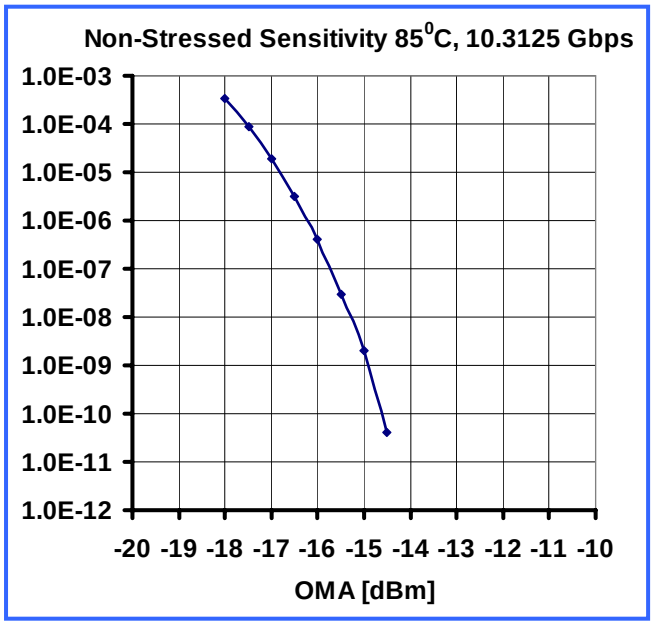
<td>(Finisar ROSA shown)</td>
<td></td>
<td> 
</td>
<td>3.65V</td>
</tr>
<tr>
<td>0 °C</td>
<td>+30 °C</td>
<td>+50 °C</td>
<td>+85°C</td>
<td></td>
</tr>
</table>

5.3 Receiver Sensitivity, 10.3125Gbps, 2^{31}-1 PRBS (Finisar ROSA shown)





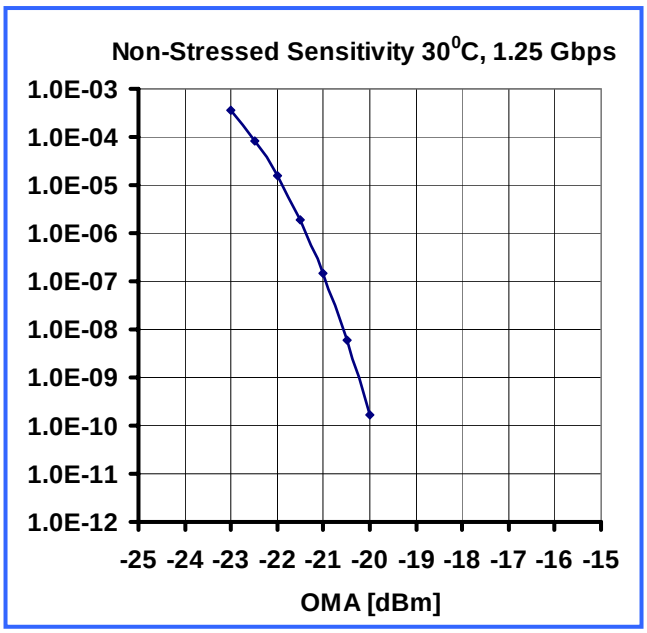


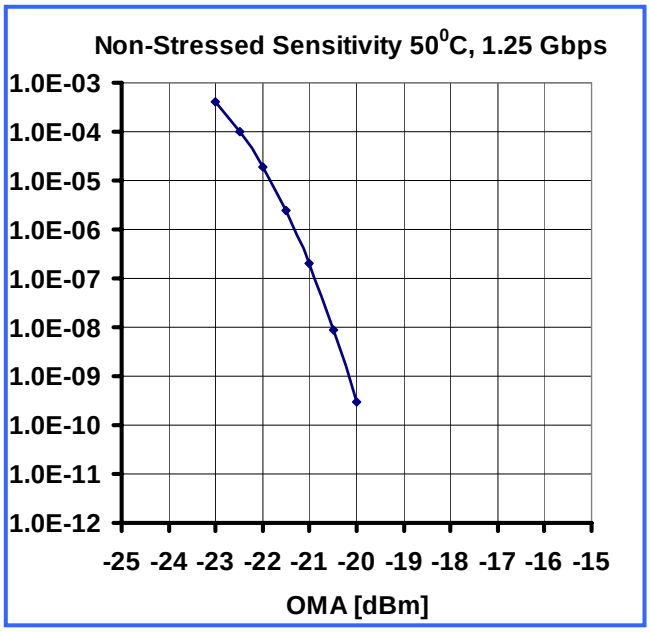


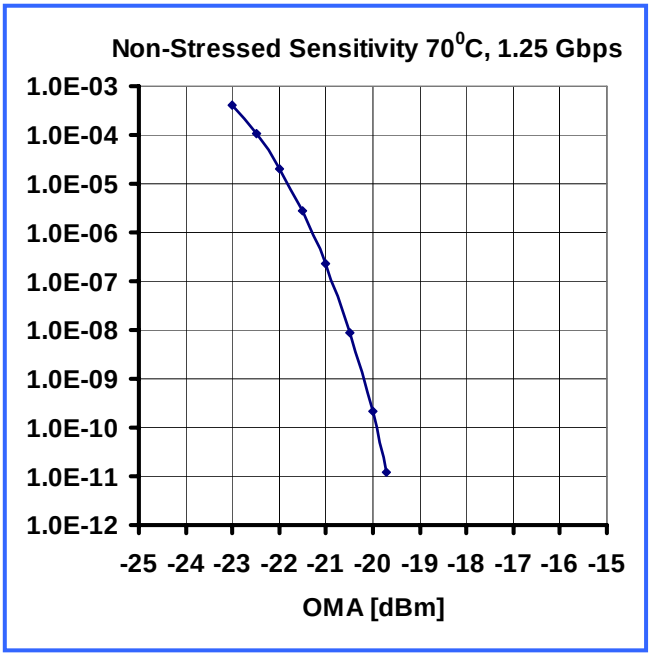
Specification (informative): -11.1dBm[1]

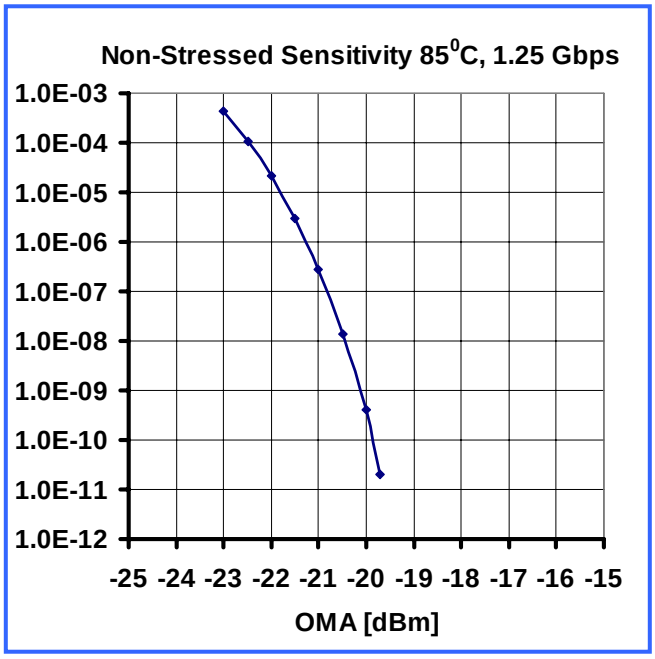
[1] IEEE(S) Std 802.3-2005, page 318, Table 52-9

5.4 Receiver Sensitivity, 1.25Gbps, 2^7-1 PRBS (Finisar ROSA shown)





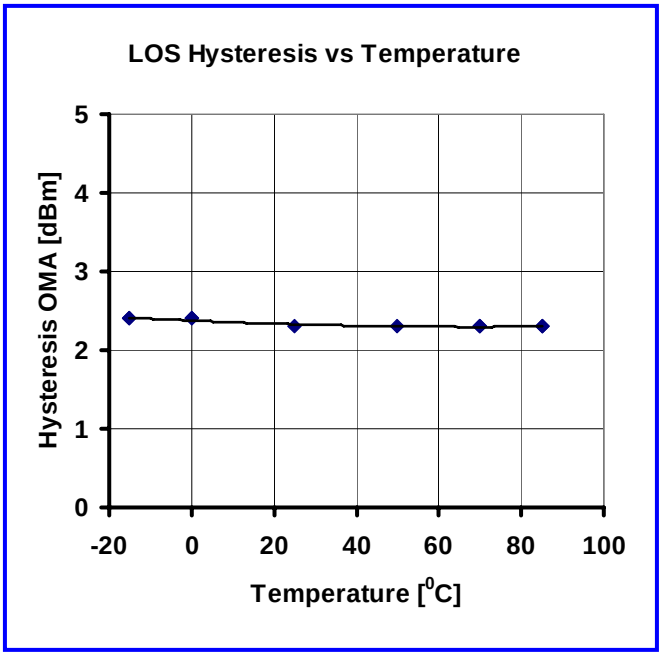


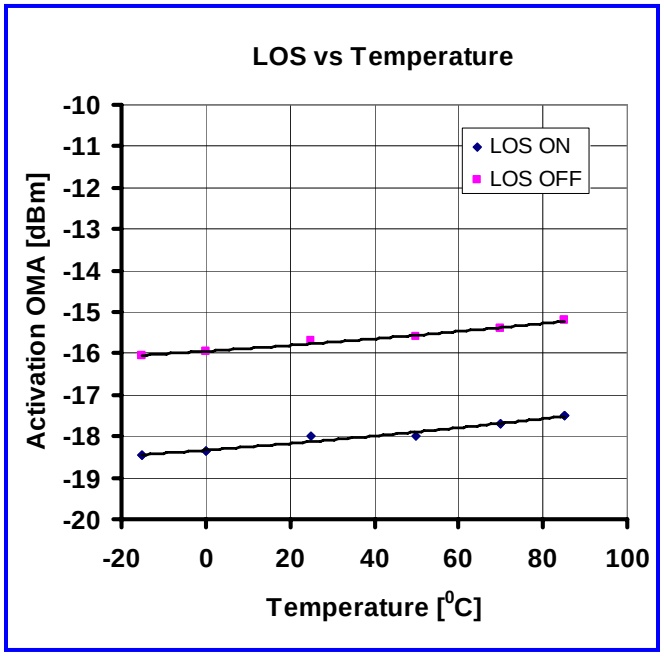


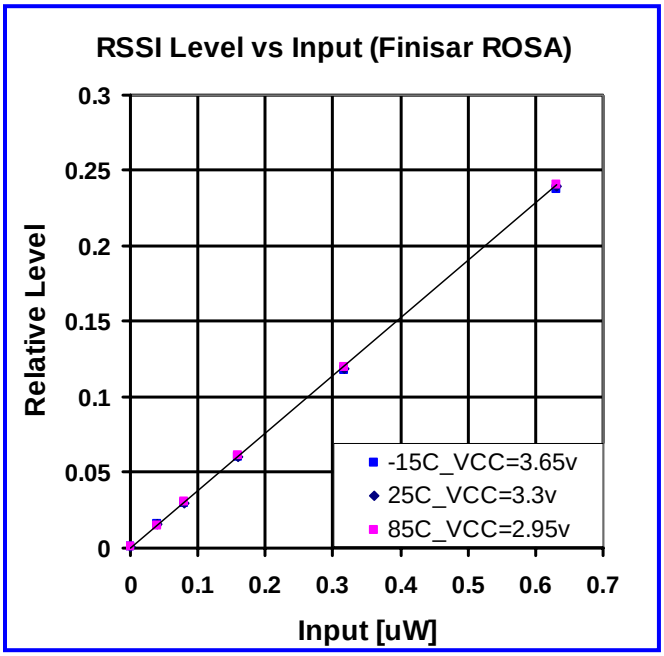
Specification (informative): -15.1dBm[2]

[2] IEEE Std 802.3-2005, page 108, Table 38-4 (Average Power converted to OMA)

5.5 Receiver LOS and RSSI, 10.3125Gbps (Finisar ROSA)







LOS level: 63 (decimal); VCC: 3.3V

6 Applications Information

6.1 Small Form-Factor Pluggable Transceivers

The HFRD-29.12 transceiver design was specifically engineered to meet the requirements of the small form-factor pluggable (SFP+) transceiver Multisource Agreement (MSA). This MSA sets guidelines for the package outline, pin function, and other aspects of the module design. By complying with the standard, modules are mechanically and functionally interchangeable.

6.2 Monitor Functions

HFRD-29.12 provides monitor outputs for RSSI, bias current, temperature, VCC, and VCSEL monitor diode power level. The uncalibrated data is displayed in the Maxim-supplied GUI discussed below. To convert to an internally-calibrated format, the user can program the appropriate registers within the DS1874.

6.3 Layout Considerations

Differential and single-ended transmission lines are designed on the HFRD-29.12 PC board. Changing the PCB layer profile can affect the impedance of these transmission lines and the performance of the reference design. If the layer profile is changed, the transmission line dimensions should be recalculated. Additional details are provided in sections 12 and 13.

6.4 Host-Board Requirements

To fully evaluate the HFRD-29.12, a Maxim Host Board, HFRD-30.1, is recommended. The HFRD-30.1 provides: the controlled impedance interface between the reference design and user's high-speed test equipment, such as the oscilloscope, and the bit error ratio tester (BERT). In addition, the host board enables the user to run the Maxim-provided GUI software through a standard USB connection. More details on this are provided in section 7 titled, "Getting Started."

6.5 Operating Data Rates

The HFRD-29.12 provides compliant sensitivity at data rates of either 1.25Gbps (8B10B coding) or 10.3125Gbps (64/66 coding). The required output power and extinction ratio for the optical signal are also dependent on the data rate selected. When a module sample is shipped to a customer, it is configured for the 10.3125Gbps data rate. The extinction ratio is set in the range of 4.5dB to 5dB. Optical power is set in the range of -1dBm to -3dBm. The customer can test the part at 1.25Gbps, but will need to adjust the modulation and APC levels for the desired extinction ratio and output power.

6.6 Operating Temperature

The operating temperature range of the MAX3799 is from -40°C to +85°C. The recommended operating temperature of the TOSAs and ROSAs varies from one manufacturer to the next. Maximum VCSEL case temperature is generally specified as +85°C. Minimum VCSEL case temperature varies from -40°C to 0°C. The suggested operating temperature range for the HFRD-29.12 is 0°C to +85°C.

6.7 Gerber Files

The Gerber files for this reference design are available by contacting Maxim support at 1-800-988-9872 between 8 a.m. and 5 p.m. Pacific Time, or by accessing our customer support through the website at: https://support.maxim-ic.com/. While Gerber files can be provided, it is still the module designer's responsibility to ensure that the layout meets all of their mechanical and thermal requirements.

6.8 TOSA and ROSA Options

At the time of this publication, there are three TOSA options and two ROSA options for HFRD-29.12. These options are outlined in sections 3.1.3 and 3.1.4. When making a sample request, the customer should indicate which TOSA and ROSA are required. At special request, Maxim may also install a customer's custom TOSA or ROSA, provided that they meet the correct mechanical and electrical specifications.

7 Getting Started

The HFRD-29.12 can be evaluated on any host board; however, to utilize the added benefit of the Maxim-supplied GUI, Maxim's host board, HFRD-30.1, is recommended. (Please refer to Reference Design HFRD-30.1 for complete details on the host board: http://www.maxim-ic.com/products/optical/reference_designs/)

Figure 2 shows the host board and associated connections. Precautions must be taken to ensure safe operation when using a device with a laser diode. Laser-light emissions can be harmful and may cause eye damage. Maxim assumes no responsibility for harm or injury as a result of the use of this reference design. The safe operation of this design is the sole responsibility of the user.

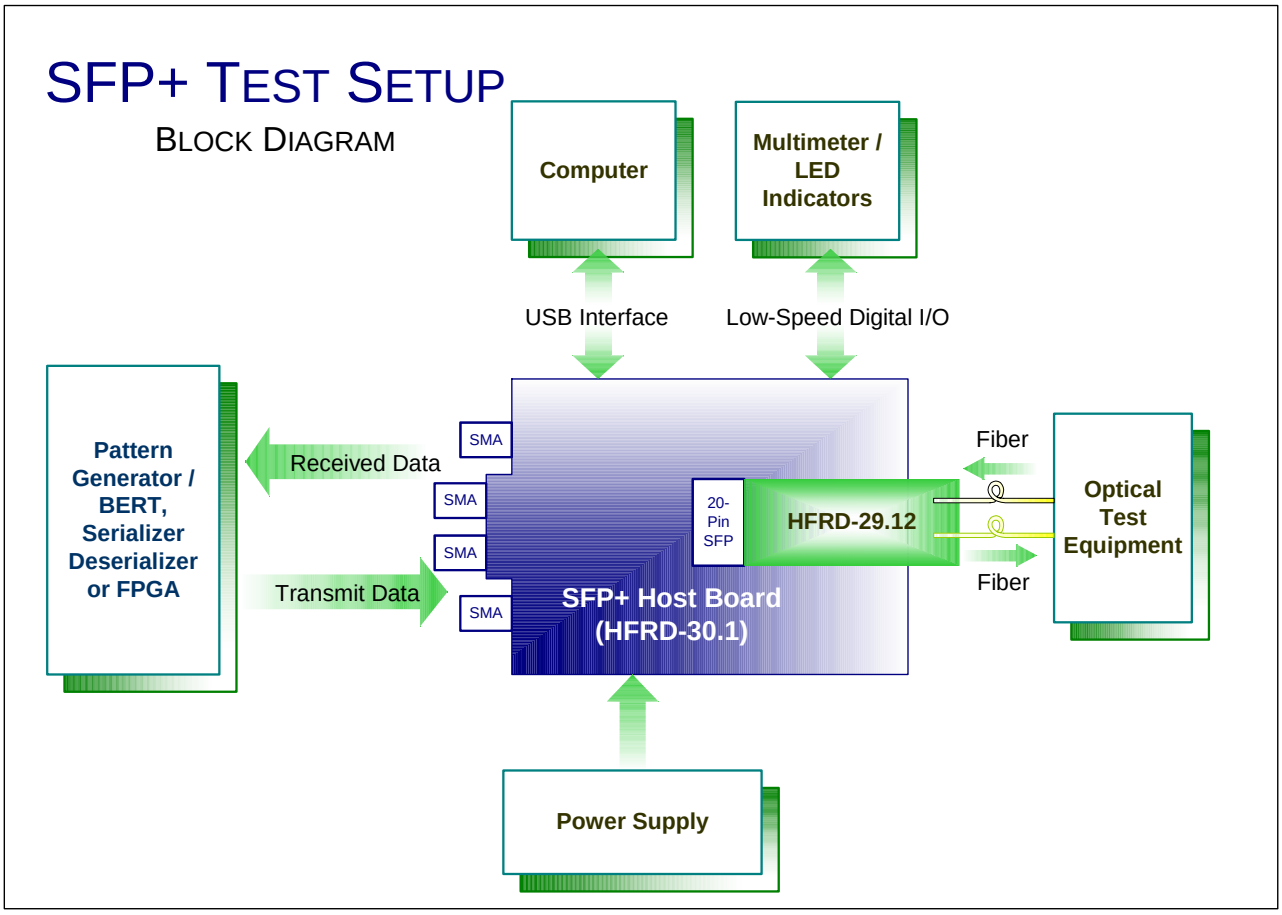


Figure 2. HFRD-29.12 with HFRD-30.1 host PCB.

1) Start with the host board. Attach a differential source such as a pattern generator to the Tx data inputs using equal lengths of high-speed SMA coax cable. The output level of the pattern generator should be set to a nominal level of 1V differential.

2) Connect the Rx data SMA outputs on the host PCB to either an oscilloscope or BERT which is triggered by the pattern generator.

3) Connect a computer to the USB port on the host PCB. The GUI software provided with this reference design should be installed in this computer.

4) Connect a power supply to the 3.3V terminal on the host board. Set the power-supply current limit to 250mA. Do not apply power.

5) Insert the HFRD-29.12 into the host board.

6) Carefully insert an LC multimode fiber-optic cable into the TOSA barrel; take care not to strain the TOSA flex. The optical cable should be secured to prevent damage to the TOSA if the fiber is accidentally moved.

7) Connect the other end of the fiber-optic cable to a high-speed oscilloscope through an optical-to-electrical converter or an optical plug-in module. The optical-to-electrical conversion should have a bandwidth sufficiently large for the operating bit rate and should be able to detect 850nm wavelengths.

Note: The laser supplied with the reference design may be capable of delivering more than 1mW of power. Attenuation may be required if the optical power exceeds the optical-to-electrical device's input power rating.

8) To view the receiver output, attach equal lengths of high-speed SMA coaxial cables to the differential outputs from the host board to the oscilloscope.

9) Connect a multimode fiber with an LC-type ferrule to the ROSA. Follow the same precautions outlined in step 6 above.

10) Connect the other end of the fiber to a high-speed 850nm optical source through an optical attenuator.

11) Apply power to the host board. Current draw should be less than 200mA.

12) The transceiver registers are preset to permit operation without running the GUI. To enable the optical output without running the GUI, connect the Tx disable test point on the host board to ground. The optical transmit eye should be observable on the scope.

13) The receiver output and LOS will also be operational. If an external reference transmitter is used as an optical source to test the receiver, the output electrical eye will be active. The RS0 is pulled high on the host board (wide bandwidth, low gain).

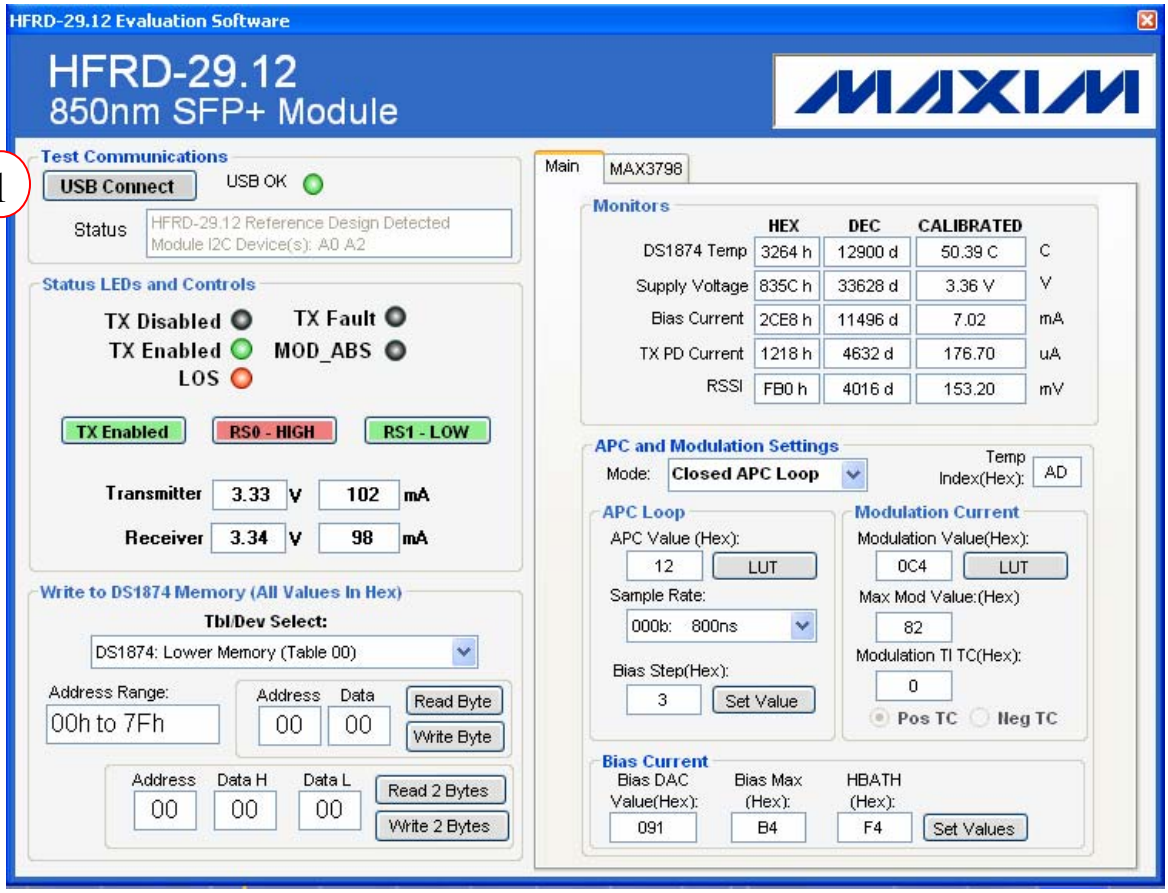
8 SFP+ Evaluation Software

Running the GUI allows the user to access and modify the settings within the DS1874 and MAX3799. The GUI also displays several monitor functions:

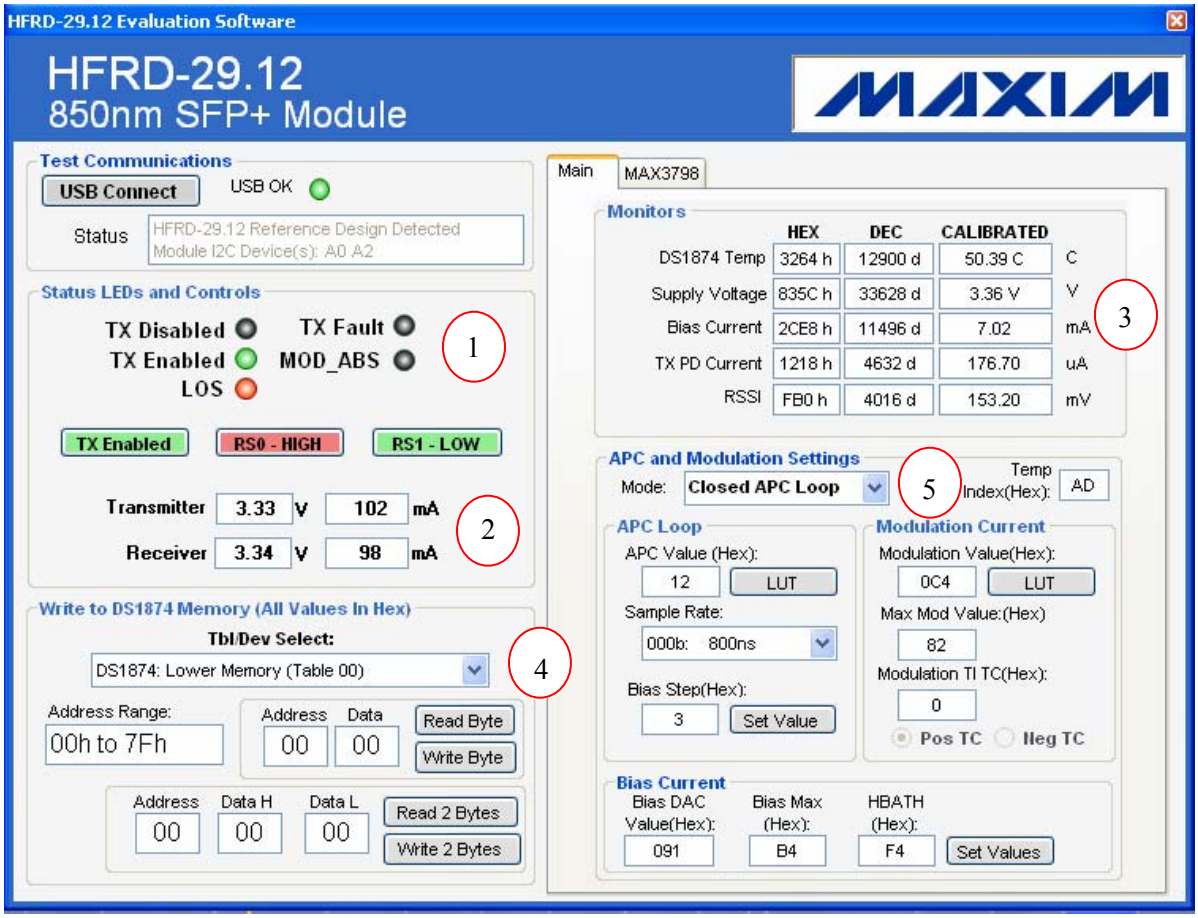
- Temperature
- VCC
- VCSEL monitor level
- Bias current
- RSSI level

VCC, temperature, bias current, and VCSEL monitor current level are all displayed in a calibrated state. The RSSI level is uncalibrated and is displayed in mV. The user, if desired can access the appropriate registers within the DS1874 and calibrate the RSSI to indicate receive power. Alarm threshold levels can also be programmed. The VCSEL monitor level (μA) can also be converted to represent the VCSEL transmit power (μW) by adjusting the calibration coefficients within the DS1874.

Activate the GUI. The screen shown below should appear.



1. USB Connect. Pressing this button initializes the test communication. This button resets the GUI interface, and initializes a test sequence to determine if the HFRD-30.1 is connected to the computer. The software then scans the I^2C bus to determine if any I^2C-addressable modules are connected to the HFRD-30.1 host board.



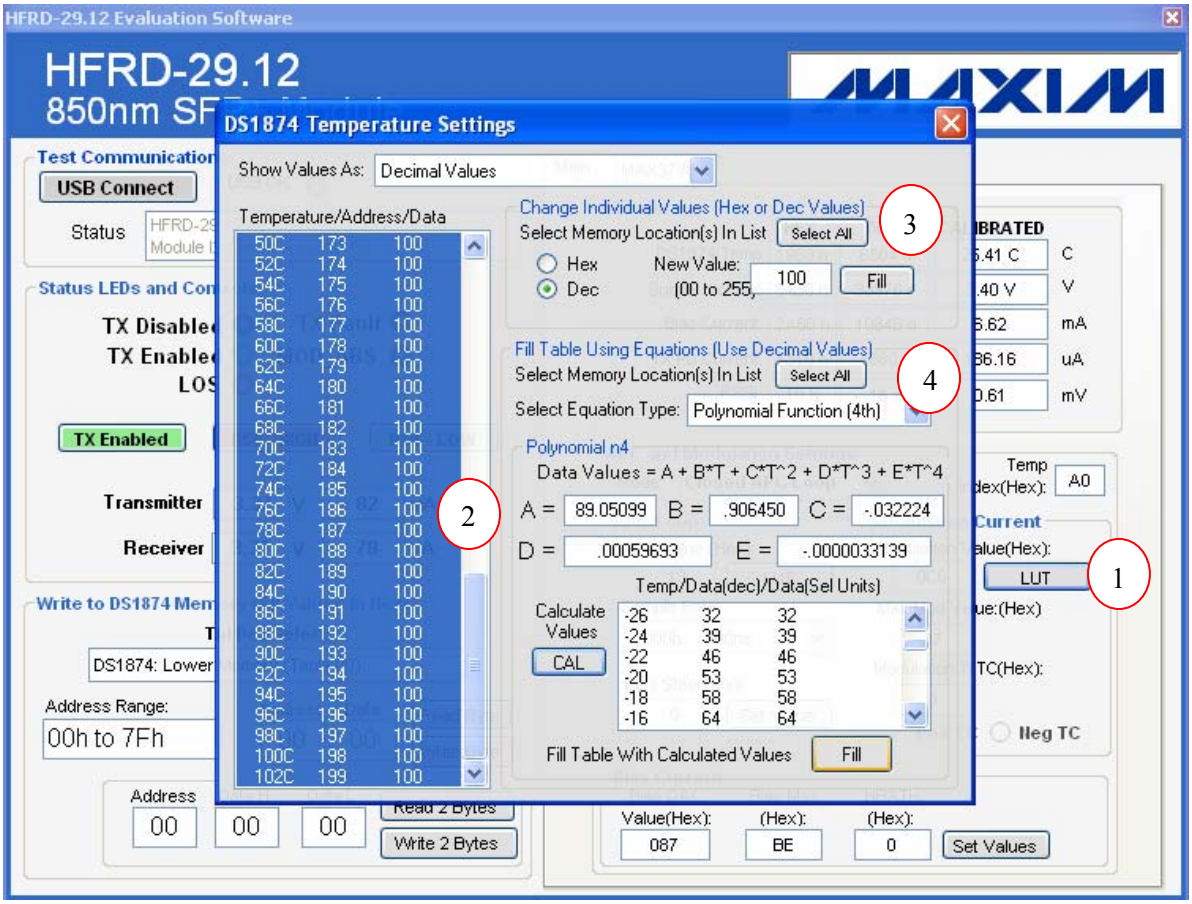
1. Status LEDs and Controls. Pressing **TX Enabled** or **TX Disabled** enables or disables the transmitter. Pressing **RS0** or **RS1** will toggle the output high or low. Transmit status indicators are also displayed.

2. Supply Monitoring. This section displays the voltage and current for the SFP+ module. The transmitter and receiver VCC are connected together inside the SFP+ module. The SFP+ host board splits the current-draw reading, so the total current draw for the module is the sum of the transmit and receiver current.

3. Monitor Displays: This section displays the five monitor functions for DS1874 temperature, DS1874 supply voltage, VCSEL bias current, monitor photocurrent, and RSSI level.

4. DS1874 Memory Access: This interface allows the user to read or write to any table and address within the DS1874.

5. APC and Modulation Settings: This permits the user to easily access the lookup tables (LUTs) for both the APC Value and Modulation Value. It also provides a drop-down menu to set the mode of operation in either open or closed loop. In closed loop the APC Loop LUT determines the bias current setting. Press **LUT** to enable access to the lookup table.

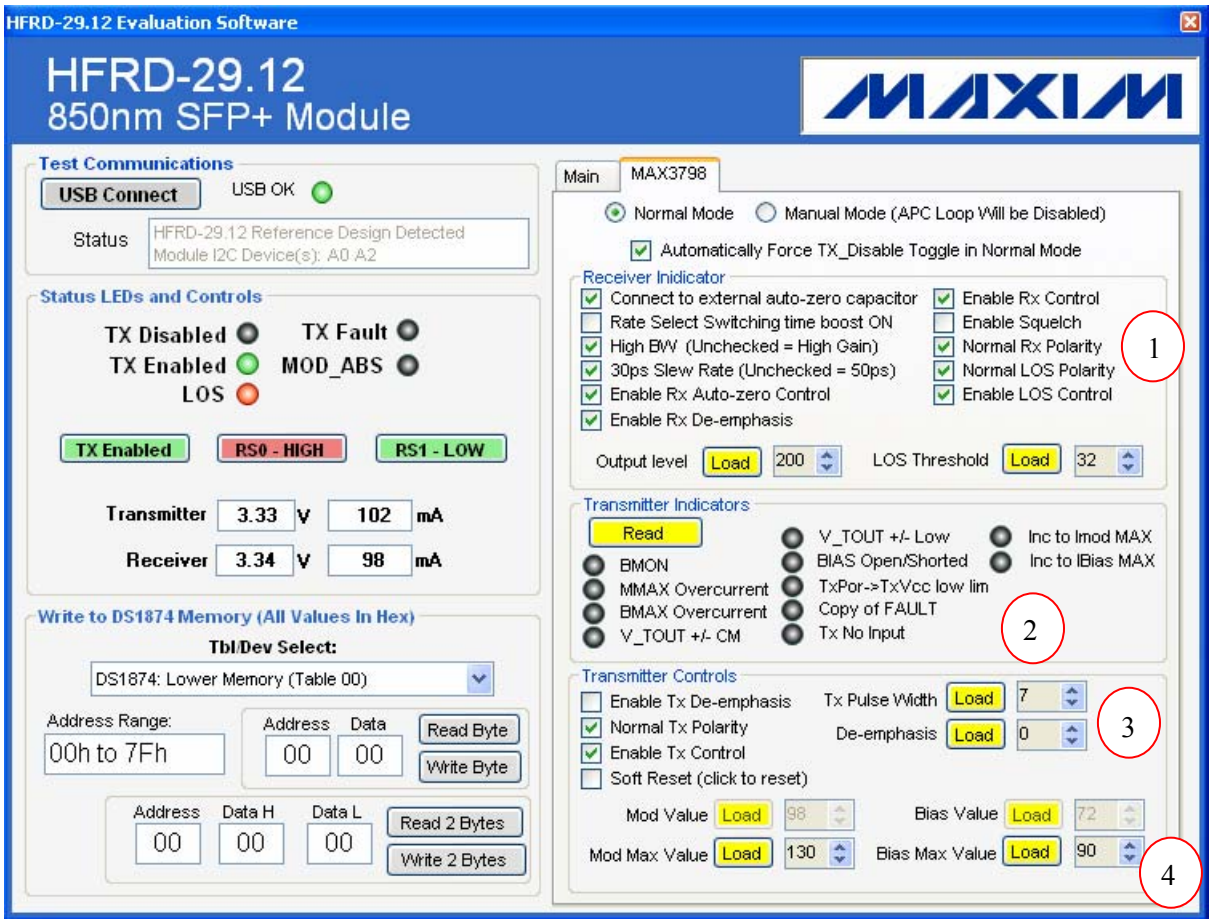


1. LUT: Pressing the **LUT** control for either the APC or Modulation value causes the selected window to appear.

2. Temperature/Address/Data: This area displays the individual LUT register locations for each temperature along with the corresponding setting. In this example the modulation is set to 100 over all temperatures.

3. Change Individual Values: Individual values for a specific temperature can be selected by highlighting the selected values in the Temperature/Address/Data table (2) and then entering the desired value in "New Value." The value entered can be either in Hex or Decimal format. Press **Fill** to enter the values. If filling all locations with the same value is desired, simply press **Select All** followed by **Fill.**

4. Fill Table Using Equations: This gives the option of filling the modulation or APC table with values determined by an equation. Select equation type from linear to fourth-order polynomial using the pull down menu. In the above example, a fourth-order polynomial has been selected. Enter the desired coefficients. Press **Select All** (next to 4) then press **CAL**. The computed values will appear in the table to the right of the **CAL** button. Then press **Fill** located at the bottom of the window. The calculated values will be transferred into a lookup table, overwriting whatever values were stored there.



MAX3798 registers
(also applicable for MAX3799)

1. Receiver Indicator: These are used to set the individual bits for the RXCTRL1, RXCTRL2, and output CML and LOS threshold registers. After a setting is changed, the control is set to automatically force TX Disable which causes the new value to be loaded into the appropriate register for the MAX3798 or MAX3799.

2. Transmitter Indicators: These are updated every time the **Read** button is pressed. Note that the MMax Overcurrent and BMax Overcurrent are not used in the MAX3799.

3. Transmitter Controls: These are used to set the TXCTRL, TX Pulse Width and TX De-emphasis registers. After a setting is changed, the control is set to automatically force TX Disable which causes the new value to be loaded into the appropriate register for the MAX3798 or MAX3799.

4. MAX Settings: The maximum desired value for modulation and bias currents may be entered here.

9 Signal Definitions

Connector Pin	I/O Type	Name	Definition
1, 17, 20		VEET	Module transmitter ground (Note 4)
2	LVTTL OUTPUT	TX_FAULT	Transmitter fault output (Note 1); the transmitter is disabled when TX_FAULT is asserted.
3	LVTTL INPUT	TX_DISABLE	Transmitter disable input; the transmitter is disabled when TX_DISABLE is asserted.
4	LVTTL INPUT / OUTPUT	MOD-DEF2	2-wire serial interface, bidirectional data line (Note 1)
5	LVTTL INPUT	MOD-DEF1	2-wire serial interface clock line (Note 1)
6	LVTTL OUTPUT	MOD-DEF0	Pin is pulled low by the SFP+ module to indicate to the host controller that a module is present (Note 1).
7	LVTTL INPUT	RATE SEL1	Optional bandwidth selection input (not used in HFRD-29.12)
8	LVTTL OUTPUT	LOS	Receiver loss-of-signal output (Note 1); output is high when receiver input signal is below the set threshold (Note 2).
9	LVTTL INPUT	RS0	Sets receiver input mode (0 = low BW; 1 = high BW).
10, 11, 14		VEER	Module receiver ground (Note 4)
12	OUTPUT	RD-	Inverted received data output, AC-coupled inside the SFP+ module
13	OUTPUT	RD+	Noninverted received data output, AC-coupled inside the SFP+ module
15		VCCR	+3.3V receiver power-supply connection; may be internally connected to VCCT inside the SFP+ module (Note: 3).
16		VCCT	+3.3V transmitter power-supply connection; may be internally connected to VCCR inside the SFP+ module (Note: 3).
18	INPUT	TD+	Inverted transmit data input, AC-coupled inside the SFP+ module
19	INPUT	TD-	Noninverted transmit data input, AC-coupled inside the SFP+ module

Note 1: Open collector output. These pins must be pulled high (+2.95V to +3.65V) on the host board through a 4.7kΩ to 10kΩ resistor.

Note 2: LOS function can be inverted, if desired, in the HFRD-29.12.

Note 3: VCCR and VCCT are connected together inside HFRD-29.12.

Note 4: VEER and VEET are connected together inside HFRD-29.12.

10 Component List

Reference	Qty	Value	Description
C1 C3 C8 C11-12	5	0.1uF	CAPACITOR (0201)
C10	1	0.001uF	CAPACITOR (0402)
C14 C23 C25 C28-29 C33 C35 C38	8	0.01uF	CAPACITOR (0402)
C16 C30 C34 C40-42	6	0.01uF	CAPACITOR (0201)
C2 C4 C18 C24 C39	5	0.1uF	CAPACITOR (0402)
C5-6	2	20pF	CAPACITOR (0201)
C7 C19 C36	3	1.0uF	CAPACITOR (0402)
C9 C13	2	1000pF	CAPACITOR (0402)
L1 L3 L7 L9	4		CHIP BEAD, MURATA BLM15HG102SN1
L10 L4	2		CHIP BEAD, MURATA BLM15HB121SN1
L12-13	2	47uH	INDUCTOR (0603) TAIYO YUDEN LBMF1608T470K
L2 L11	2		BEAD, MURATA BLM15BD601SN1
L5 L8	2		BEAD, MURATA BLMHG601SN1
R1 R4 R21	3	1.0k	RESISTOR (0402)
R14-15	2	0	RESISTOR (0201)
R16	1	499	RESISTOR (0402)
R17-18	2	NO POP	RESISTOR (0201)
R19	1	511	RESISTOR (0402)
R2 R8-12	6	5.11k	RESISTOR (0402)
R23 R26	2	NO POP	RESISTOR (0402)
R24-25	2	0	RESISTOR (0402)
R3	1	10.0k	RESISTOR (0402)
R6 R13	2	30.1	RESISTOR (0201)
R7	1	30.1k	RESISTOR (0402)
U1	1		DS1874, SFP+ Controller
U2	1		MAX3799
U3	1		ROSA with Flex
U4	1		TOSA with Flex
U5	1		PMOS TRANSISTOR FAIRCHILD FDN302P

Note 1: For ground reference RSSI operation: R16 = 1kΩ, R23 = 0Ω, R26 = 0Ω, R24-R25 = NO POP (Do Not Populate).

Note 2: To increase buffer attenuator from 0dB to 4dB: R14 to R15 = 24Ω, R17 to R18 = 440Ω.

11 Schematic

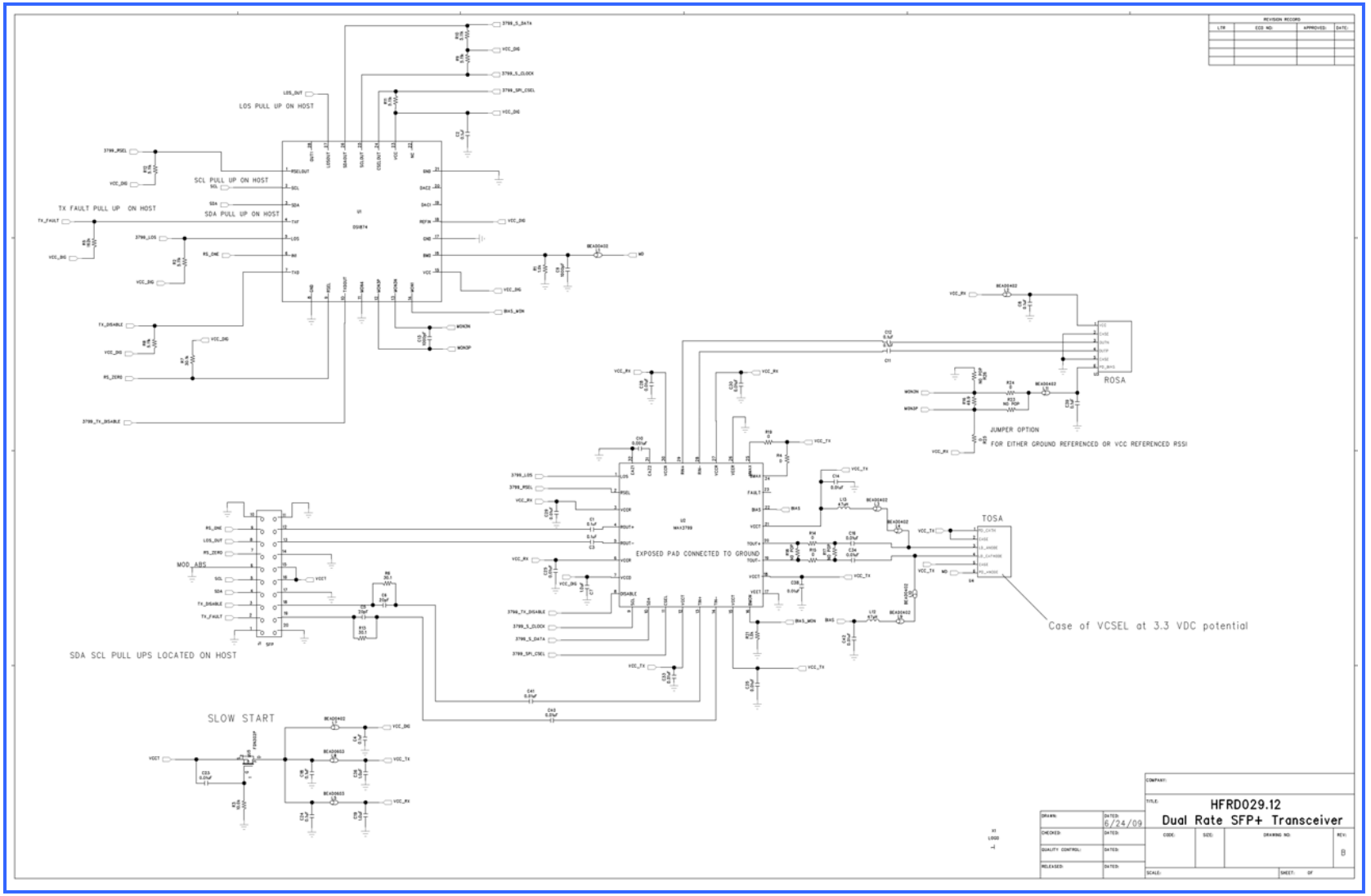


Figure 3. HFRD-29.12 schematic.

12 Board Layout

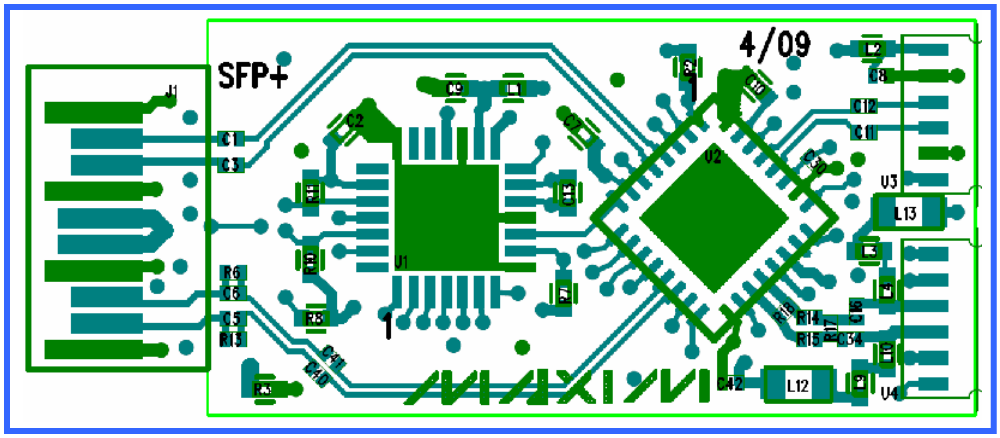


Figure 4. Board layout, component side—Layer 1.

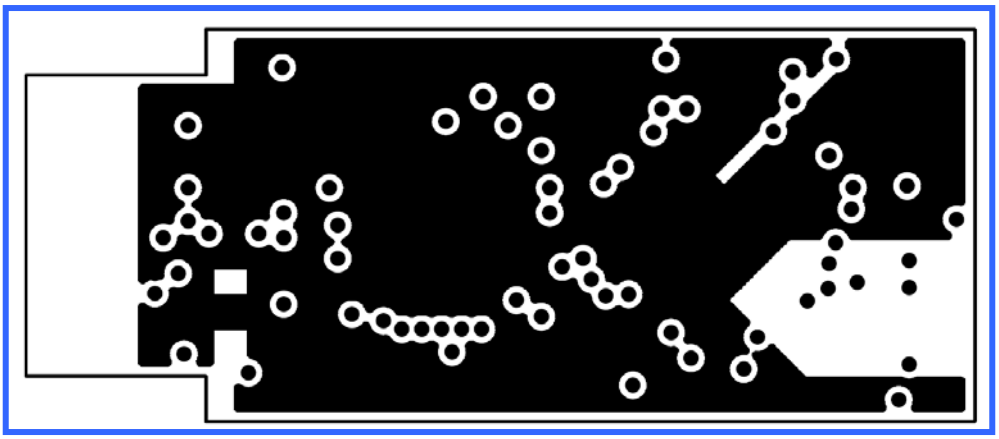


Figure 5. Board layout, ground plane—Layer 2.

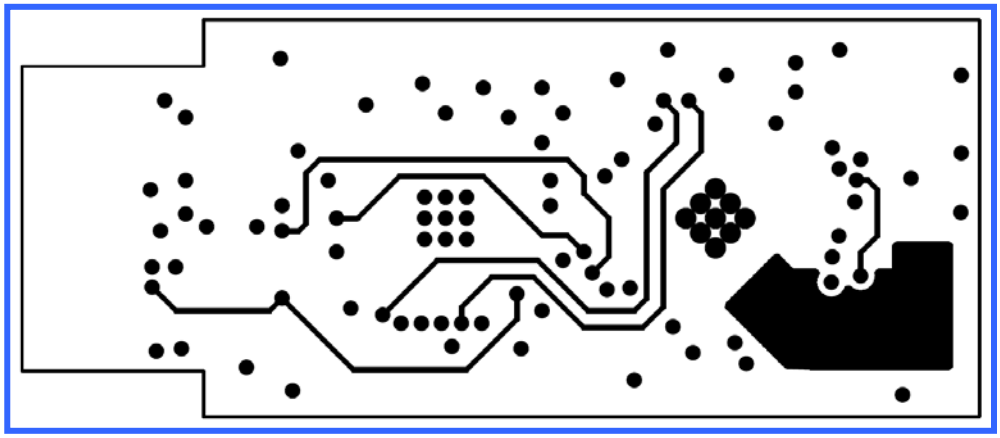


Figure 6: Board layout, miscellaneous routing and VCC—Layer 3.

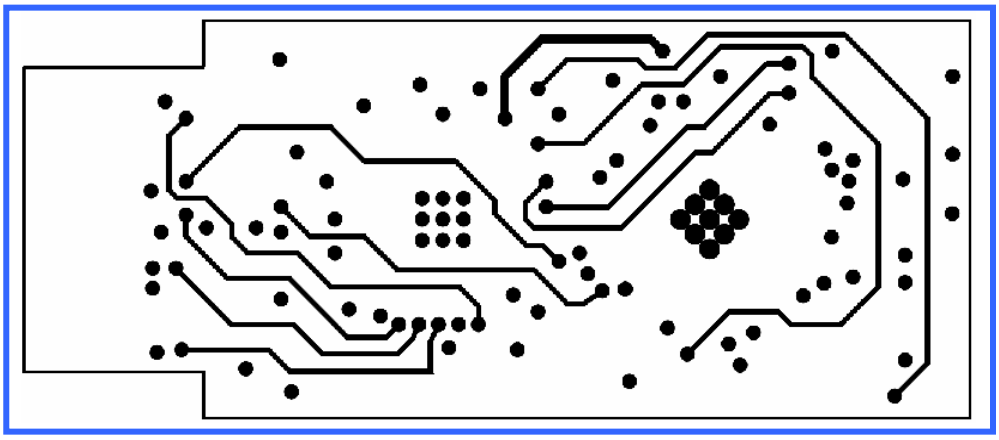


Figure 7. Board layout, miscellaneous routing—Layer 4.

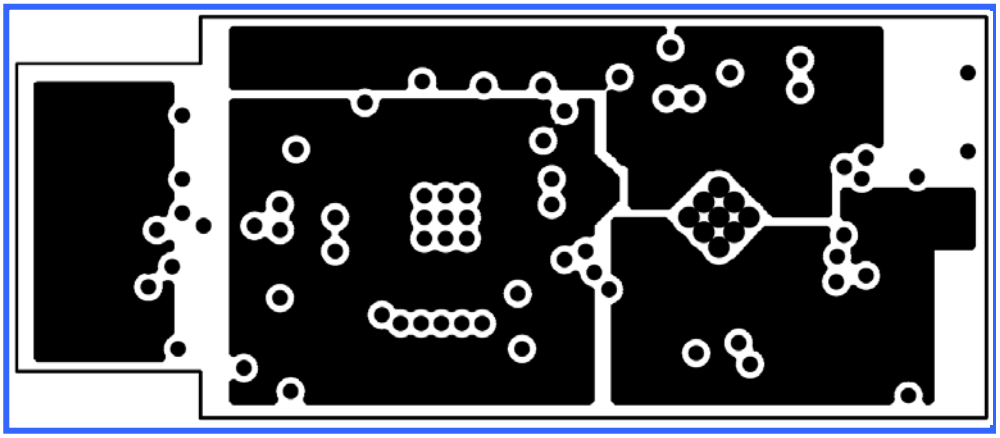


Figure 8. Board layout, VCC plane—Layer 5.

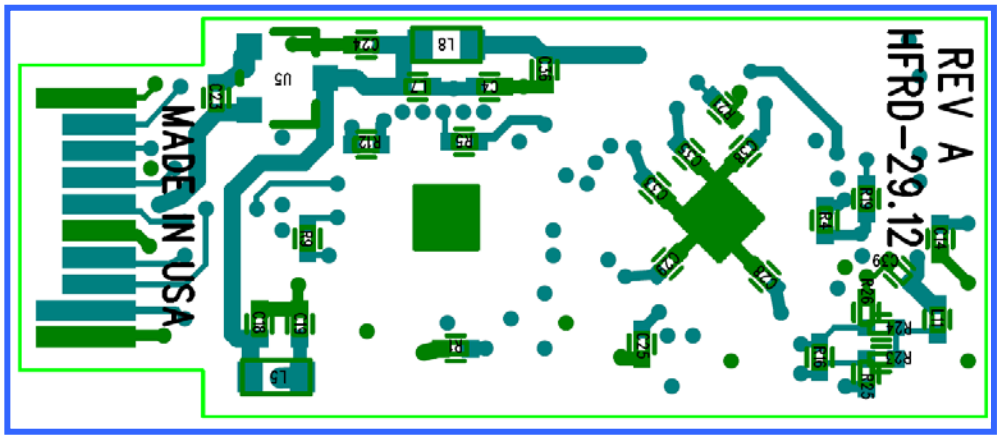


Figure 9. Board layout, solder side—Layer 6.

13 Layer Profile

The HFRD-29.12 includes controlled-impedance transmission lines. The layer profile is shown in Figure 10. The controlled-impedance transmission line connecting the output of the MAX3799 to the TOSA flex is between layer 1 and layer 3. A dielectric constant of 4.3 is assumed.

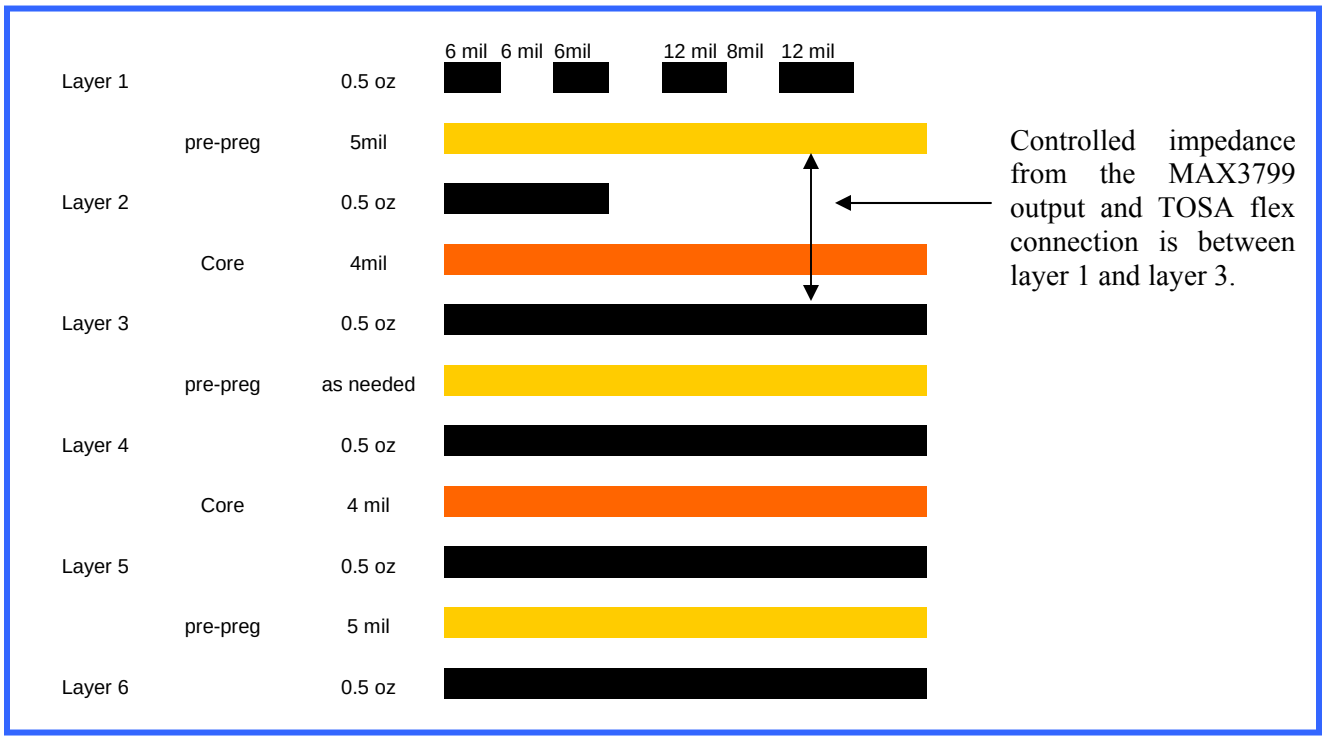


Figure 10. Layer profile for HFRD-29.12.