Click here to ask about the production status of specific part numbers.

MAX25430

Automotive 100W USB-PD Buck-Boost Port Controller and Protector

General Description

The MAX25430 combines an automotive-grade buck-boost controller capable of driving up to 5.0A, a USB-PD Analog Front-End (AFE), Legacy USB Charging support and USB Type-C™ protection for USB host or DFP applications. The USB Type-C protection switches provide automotive system-level ESD and 24V short-circuit protection for D+, D-, CC1, CC2, and VCONN. The device also supports legacy USB 2.0 charging modes including BC1.2, Apple® 2.4A, Apple CarPlay®, Apple MFi and USB On-The-Go (OTG).

The MAX25430B integrates a USB-PD AFE which supports the USB-IF Type-C Port Controller Interface (TCPCI) specification and can interface with any I2C Master in the application.

The MAX25430A provides CC signal passthrough protection for an external USB-PD controller.

G-Suffix devices include intelligent detection and protection to avoid high short-circuit currents flowing from the car battery through the cable shield to ground during fault events, preventing car module damage.

The MAX25430 EVKIT and collateral provides a convenient platform to the design engineer for rapid evaluation with reduced test and firmware development time. The MAX25430 is available in a small 6mm x 6mm 40-pin TQFN package and requires very few external components.

Applications

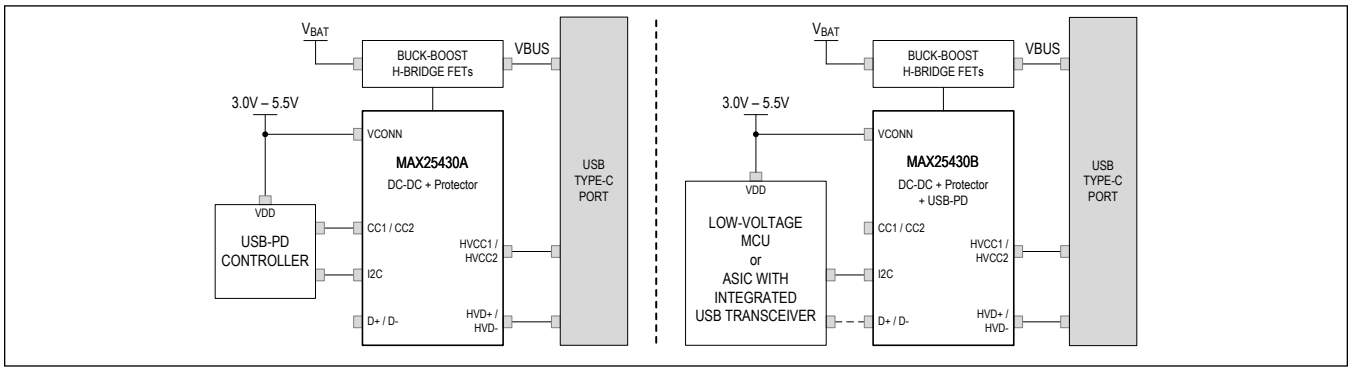
- USB Hubs, Breakout Boxes and Multimedia Hubs
- Dedicated Charging Modules
- Rear-Seat Entertainment Modules

Benefits and Features

- USB-PD PHY That is TCPCI Standard for Use with Any Low-Cost I2C Master Such as Hub IC, MCU or SOC (MAX25430B)
  - Ground-Offset-Adjusted BMC PHY for Maximum Signal-to-Noise Ratio
- Non-TCPC Versions Available for Protecting External USB-PD Controller (MAX25430A)
- Integrated Buck-Boost Controller for External H-bridge
  - 4.5V to 36V Input Operating Range
  - Fixed PDO 5V, 9V, 15V and 20V up to 5.0A
  - 220kHz, 300kHz or 400kHz Switching Frequency
  - External Frequency Synchronization and Spread Spectrum for Reduced EMI
- Integrated and User-Programmable Buck-Boost Output Voltage Adjustment up to 500mΩ of Cable Resistance
- Highest Performance, Safest, and Lowest Cost Passenger Cable-Shield Short-to-Battery Protection
  - Minimizes Short-Circuit Currents with a Small, Single-FET Solution
- Integrated 3.0V to 5.5V 1W Smart, Reliable VCONN Switch with Protection
- Integrated 24V Protection on HVD+, HVD-, HVCC1 and HVCC2
- Integrated Legacy USB 2.0 Charging Support including BC1.2, Apple CarPlay, MFi R33, and OTG
- Integrated ±15kV Air, ±8kV Contact ISO 10605 and IEC 61000-4-2 ESD Protection
- -40°C to 125°C Operating Temperature Range
- 40-Pin (6mm x 6mm) TQFN Package with EP
- AEC-Q100 and AEC-Q006 Qualified

Ordering Information appears at end of data sheet.

Simplified Block Diagram



19-100826; Rev 0; 7/20

Absolute Maximum Ratings

IN to PGND ..... -0.3V to +40V
HVEN, CSP1, CSN1 to PGND ..... -0.3V to V_{IN}+0.3V
LX1 to PGND (Note 1) ..... -0.3V to V_{IN}+0.3V
OUT, CSP2, CSN2 to PGND ..... -0.3V to +30V
LX2 to PGND (Note 1) ..... -0.3V to V_{IN}+0.3V
CSP_ to CSN_ ..... -0.3V to +0.3V
BST1 to LX1, BST2 to LX2 ..... -0.3V to +6V
BST1, DH1 to PGND ..... -0.3V to +46V
BST2, DH2 to PGND ..... -0.3V to +36V
DH_ to LX_ ..... -0.3V to $V_{BST\_}$+0.3V
DL_, COMP, FB to PGND ..... -0.3V to V_{BIAS}+0.3V
BIAS, V_{DD_USB}, V_{DD_IO}, V_{DD_BMC}, to AGND ..... -0.3V to +6V
PGND to AGND ..... -0.3V to +0.3V
HVCC1, HVCC2, HVDP, HVDM to AGND ..... -0.3V to +24V
SHLD_SNS to AGND ..... -0.3V to +24V
CC1, CC2, VCONN to AGND ..... -0.3V to +6V
DP, DM to AGND ..... -0.3V to (V_{VDD_USB}+0.3)V
ADDR, $\overline{ALERT}$, GDRV, FSYNC, to AGND ..... -0.3V to +6V
SCL, SDA to AGND ..... -0.3V to (V_{VDD_IO}+0.3)V
Continuous Power Dissipation (Note 2) 2963mW
Operating Temperature Range ..... -40 °C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Note 2: Multilayer Board; T_A = +70°C, derate 37mW/°C above +70°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

Package Code	T4066+5C
Outline Number	21-0141
Land Pattern Number	90-0055
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	27°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDD_IO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Input Voltage Range on IN	V_{IN}		4.5		36	V
IN Supply Current - Off State	I_{IN_OFF}	V_{IN} = 18V, HVEN = 0V, V_{VCONN} = 0V, OFF State		16		µA
IN Supply Current - Standby State	I_{IN_STDBY}	Powered; Enabled; VBUS OFF		2.3		mA
IN Undervoltage Lockout Threshold	V_{IN_UVLO}	V_{IN} Rising. Default setpoint. Programmable from 4.5V to 8.5V in 0.4V steps with IN_UV_THRESH[3:0] register.		7.3		V

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDD_IO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Undervoltage Lockout Rising Accuracy	$V_{IN\_UVLO\_ACC}$	Setpoint programmable in 0.4V steps with IN_UV_THRESH[3:0] register.	Setpoint-0.3	Setpoint	Setpoint +0.3	V
IN Undervoltage Blanking Time				150		µs
INTERNAL REGULATORS						
BIAS Output Voltage	V_{BIAS}	V_{IN} > 6V, I_{BIAS} = 0mA to 60mA	4.7	5.0	5.4	V
BIAS Dropout Voltage	$BIAS_{DROP}$	V_{IN} = 4.5V, V_{OUT} = 4V, I_{BIAS} = 20mA		0.125	0.25	V
BIAS Undervoltage Lockout	UV_{BIAS}	V_{BIAS} falling	2.7	3.0	3.3	V
BIAS Undervoltage Lockout Hysteresis	UV_{BIAS_HYST}			0.25		V
BIAS Short-Circuit Current Limit	$IBIAS_{SC}$	V_{BIAS} shorted to AGND	100	200		mA
V_{DD_USB} Output Voltage	V_{DD_USB}		3.0	3.3	3.6	V
V_{DD_USB} Overvoltage	$V_{DD\_USB\_OV}$	Rising	3.8	4.0	4.3	V
V_{DD_BMC} Output Voltage	V_{DD_BMC}	MAX25430B only	1.05	1.125	1.2	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		(Note 4), T_J Rising		165		ºC
Thermal Shutdown Hysteresis		(Note 4)		10		ºC
BUCK-BOOST CONTROLLER						
V_{BUS} VOLTAGE	V_{OUT_5V}	VOUT_SEL[1:0] = 00b	5.05	5.15	5.25	
	V_{OUT_9V}	VOUT_SEL[1:0] = 01b	8.8	9.0	9.2	V
	V_{OUT_15V}	VOUT_SEL[1:0] = 10b	14.7	15.0	15.3	
	V_{OUT_20V}	VOUT_SEL[1:0] = 11b	19.6	20.0	20.4	
V_{BUS} Slew Rise & Fall Times During Transitions	T_{SLEW}			0.8		mV/ µsec
Soft Start Ramp Time	T_{START}		4.0	6.5	9.0	ms
Minimum On-Time	T_{ON_MIN}	Buck mode, 400kHz switching		80		ns
Minimum Off-Time	T_{OFF_MIN}	Boost Mode, 400kHz switching		120		ns
Dead Time	DT	Rising and falling edges of DH_ to DL_ and DL_ to DH_		17		ns
DH Pullup Resistance	R_{DH_PU}	V_{BIAS} = 5V, I_{DH} = -100mA		2	4	Ω
DH Pulldown Resistance	R_{DH_PDWN}	V_{BIAS} = 5V, I_{DH} = +100mA		1	2	Ω
DL Pullup Resistance	R_{DL_PU}	V_{BIAS} = 5V, I_{DL} = -100mA		2	4	Ω
DL Pulldown Resistance	R_{DL_PDWN}	V_{BIAS} = 5V, I_{DL} = +100mA		1	2	Ω

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDD_IO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DL1, DL2 Leakage Current	I_{DL_LKG}	V_{DL1} = V_{DL2} = 0V to 5V, T_A = +25°C				1	µA
DH1 Leakage Current	I_{DH1_LKG}	V_{DH1} = V_{LX1} = 0V, T_A = +25°C				1	µA
DH2 Leakage Current	I_{DH2_LKG}	V_{DH2} = V_{LX2} = 0V, T_A = +25°C				1	µA
BUCK-BOOST OSCILLATOR							
Buck-Boost Oscillator Switching Frequency	f_{sw}	FSW[1:0] = 00b			220		kHz
		FSW[1:0] = 01b			300		
		FSW[1:0] = 10b			400		
FSYNC External CLK Input	F_{SYNCI}	Minimum sync pulse width is the percentage of the internal CLK frequency set by FSW & duty cycle >= 30%		80		120	%
Spread Spectrum	SPS	SS_SEL[1:0] = 01b			+/-3		%
		SS_SEL[1:0] = 10b			+/-6		
		SS_SEL[1:0] = 11b			+/-9		
Slope Compensation Peak Ramp Voltage	V_{SLOPE_PK}	Peak Ramp Voltage per switching period. Default setpoint shown. Programmable from 100mV to 800mV in steps of 100mV with SLP[2:0] register.			400		mV
BUCK-BOOST CURRENT SENSE							
Input Current Limit Threshold	V_{OC1}	V_{CSP1} - V_{CSN1} rising			50	60	mV
Output Runaway Limit Threshold	V_{OC2}	V_{CSP2} - V_{OUT} rising, V_{OUT} > 0V			75	90	mV
CS Negative Limit Threshold	V_{OC3}	$\lvert V_{CSP2} - V_{OUT} \rvert$ rising, V_{OUT} > 4.5V		-26	-20	-14	mV
Output Overcurrent Detection Threshold	$I_{LIM\_OUT\_PRG}$	R_{CS2} = 2.5mΩ	VOUT_ILIM[1:0] = 00b		3.3		A
			VOUT_ILIM[1:0] = 01b		4.3		
			VOUT_ILIM[1:0] = 10b and 11b		6		
Output DC Current Shutdown Detection Threshold	I_{OUT_OCP}	R_{CS2} = 2.5mΩ			7.5		A
CABLE COMPENSATION							
Cable Comp Loop Gain-V_{ADJ}		10mV < V_{OUT} - V_{CSN2} < 100mV, GAIN[5:0] = 111111b			25		V/V
R-Cable Adjustment /LSB	R_{COMP_LSB}				8		mΩ
HVEN & SYNC I/O Pins							
V_{IH} Threshold	V_{IH}	V_{HVEN} or V_{SYNC} Rising		2.0			V
V_{IL} Threshold	V_{IL}	V_{HVEN} or V_{SYNC} Falling				0.5	V

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDD_IO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVEN Input Leakage	I_{HVEN_LKG}	V_{HVEN} = 5.5V, T_A = +25°C			+1	µA
SYNC Pulldown Resistance	$R_{SYNC-PD}$			1		MΩ
VCONN SWITCH						
V_{CONN} Valid Voltage Range	V_{VCONN}		3.0		5.5	V
V_{CONN} Switch ON Resistance	R_{ON_VCONN}	V_{VCONN} = 5.0V and V_{VCONN} = 3.3V, $I_{HVCC\_}$ = 0.25A		430	860	mΩ
V_{CONN} Overcurrent Threshold (Low)	$I_{VCONN\_OCP\_L1}$	Measured on CC1 and CC2. V_{VCONN} = 5.0V. VCONN_OCP_SEL = 0b.		250		mA
	$I_{VCONN\_OCP\_L2}$	Measured on CC1 and CC2. V_{VCONN} = 3.3V. VCONN_OCP_SEL = 1b.		360		
V_{CONN} Overcurrent Threshold (High)	$I_{VCONN\_OCP\_H}$	Measured on CC1 and CC2. V_{VCONN} = 3.3V and V_{VCONN} = 5.0V.		700		mA
V_{CONN} Startup Time at 90%	t_{VCONN_ON}	Time from VCONN switch enable to CC settled at 90% of final value with V_{VCONN} = 5.0V		80		us
V_{CONN} Leakage Current	I_{VCONN_LKG}	V_{CONN} switch disabled. V_{VCONN} = 5.0V.			5	uA
V_{CONN} Fast UV Comparator Trip Threshold	$V_{VCONN\_FAST\_UV}$	V_{CONN} enabled, measured at V_{CONN} pin, V_{VCONN} falling.	Setpoint -0.25	Setpoint	Setpoint + 0.25	V
USB TYPE-C/CURRENT LEVEL CHARACTERISTICS						
CC DFP Default Current Source	$I_{DFP\_DEF\_CC}$		64	80	96	µA
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC}$		166	180	194	µA
CC DFP 3.0A Current Source	$I_{DFP3.0\_CC}$		304	330	356	µA
CC PASS-THROUGH ANALOG SWITCHES						
Analog Signal Range			0		5.5	V
CC Switch ON Resistance	R_{ON_CC}	Resistance from CC1 to HVCC1 or CC2 to HVCC2		4		Ω
HVCC OV Protection Trip Threshold	V_{OV_HVCC}		5.65	5.80	5.95	V
HVCC Overvoltage Blanking Timeout Period	t_{FP_HVCC}	From OV condition to switch opened		1.0		µs
CC Switch ON Leakage	$I_{CC\_ON\_LKG}$	CC Switch ON, CC pull-up voltage 5.5V; Leakage to GND.			10	µA
HVCC Pin OFF Leakage	$I_{HVCC\_OFF\_LKG}$	HVCC switch OFF; $V_{HVCC\_}$ = 20V; HVCC_ pins leakage to GND.			25	µA
HVCC Open Termination Impedance	Z_{OPEN}	Impedance to GND	500			kΩ

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDD_IO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HVCC Discharge Resistance	R_{DCH_HVCC}			3.0	6.2	kΩ
USB-PD BMC (MAX25430B ONLY)						
BMC TX Rise Time	tRise	10% to 90% with no load on CC wires	300	430		ns
BMC TX Fall Time	tFall	90% to 10% with no load on CC wires	300	430		ns
BMC TX Swing	VSwing	Applies to no load and with max load defined by cable/receiver model	1.05	1.125	1.2	V
BMC Driver Output Impedance	zDriver	Source output impedance	33	48	75	Ω
BMC Receiver noise filter	tRXFilter	Time Constant of noise filter in RX path	100			ns
Receiver Input Impedance	ZBMCRX			2		MΩ
Receiver Detect rising Threshold	VBMCRxDet_Rth		0.645	0.685	0.725	V
Receiver Detect falling Threshold	VBMCRxDet_Fth		0.565	0.605	0.645	V
DP, DM ANALOG USB SWITCHES						
Analog Signal Range			0		VDD_USB	V
Protection Trip Threshold	$V_{OV\_D\_L}$	V_{HVDP}/V_{HVDM} rising. Only for AUTO_CDP_DCP_MODE[1:0] = 01b (Auto-CDP mode)	3.65	3.85	4.05	V
	$V_{OV\_D\_H}$	V_{HVDP}/V_{HVDM} rising. All other modes	4.0	4.15	4.30	
Protection Response Time	t_{FP_D}	V_{HVEN} = 4.0V, V_{HVDP} = V_{HVDM} = 3.3V to 4.3V step, RL = 15kΩ on DP and DM, delay to V_{DP} = V_{DM} < 3V		2		µs
Data Switch Differential Bandwidth	BW_{D_DIFF}	USB TEST_PACKET @ 240MHz fundamental; -3dB BW		1000		MHz
On-Resistance Switch A	R_{ON_SA}	I_L = 10mA, $V_{D\_}$ = 0V to VDD_USB. VDD_USB = 3.3V		4	8	Ω
On-Resistance Match between Channels Switch A	ΔR_{ON_SA}	I_L = 10mA, $V_{D\_}$ = 1.5V or 3.0V			0.25	Ω
On-Resistance Flatness Switch A	$R_{FLAT(ON)A}$	I_L = 10mA, $V_{D\_}$ = 0V or 0.4V			0.25	Ω
On Resistance of HVDP/HVDM short	R_{SHORT}	V_{DP} = 1V, I_{DM} = 500µA		90	180	Ω
HVDP/HVDM On Leakage Current	I_{HVD_ON}	V_{HVDP} = V_{HVDM} = 3.6V or 0V	-7		+7	µA
HVDP/HVDM Off Leakage Current	I_{HVD_OFF}	V_{HVDP} = 18V or V_{HVDM} = 18V, V_{DP} = V_{DM} = 0V			100	µA

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDD_IO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DP/DM Off-Leakage Current	I_{D_OFF}	V_{HVDP} = V_{HVDM} = 18V, V_{DP} = V_{DM} = 0V	-1		+1	µA
USB 2.0 HOST CHARGER DETECTION, DP/DM						
Input Logic High	V_{IH_CD}		2.0			V
Input Logic Low	V_{IL_CD}				0.8	V
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V	50	85	150	µA
Data Detect Voltage High	V_{DAT_REFH}		0.4			V
Data Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data Detect Voltage Hysteresis	V_{DAT_HYST}			60		mV
Data Source Voltage	V_{DAT_SRC}	I_{SRC} = 200µA	0.5		0.7	V
V_{BUS} ADC (MAX25430B ONLY)						
ADC Resolution	Res_ADC			10		Bits
ADC V_{BUS} LSB	V_{OUT_LSB}			25		mV
ADC Acquisition Time	t_{ACQ_ADC}			1		ms
V_{BUS} OUTPUT MONITORS						
V_{BUS} OV	$V_{BUS\_OV\_PROG}$	Programmable in 1.25% steps from +8.75% to 17.5% by changing the VBUS_OV_THRESH[2:0] register.		+12.5%		%
V_{BUS} UV	$V_{BUS\_UV\_PROG}$	Programmable in 1.25% steps from -8.75% to -17.5% by changing the VBUS_UV_THRESH[2:0] register.		-12.5%		%
V_{BUS} Removal Detect Threshold	vSafe0V	Falling	0.6	0.75	0.8	V
V_{BUS} Removal Detect Hysteresis	vSafe0V	Rising Hysteresis		0.05		V
SHIELD SHORT-TO-BATTERY CONTROL (G-SUFFIX ONLY)						
GDRV Unloaded Output Voltage High	$V_{GDRV,\ H}$		4.5		5.5	V
GDRV Output Voltage High	$V_{GDRV,LOAD}$	I_{GDRV} = 10uA (sink)	4			V
GDRV Output Voltage Low	$V_{GDRV,\ L}$	I_{SINK} = 1mA (pullup)			0.8	V
I^2C DIGITAL INPUTS (SDA, SCL) AND V_{DD_IO} SUPPLY INPUT						
Input Leakage Current (SCL, SDA)		V_{PIN} = 5.5V, 0V	-5		5	µA
Logic High (SCL, SDA)	V_{IH}		0.7xV_{VDD_IO}			V
Logic Low (SCL, SDA)	V_{IL}				0.3xV_{VDD_IO}	V

Electrical Characteristics (continued)

(V_{IN} = 14V, V_{HVEN} = V_{IN}, V_{VCONN} = 5V, V_{VDD_IO} = 3.3V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hysteresis (SCL, SDA)				300		mV
VDD_IO Input Voltage Range	V_{VDD_IO}		1.8		5.0	V
ADDR RESISTOR CONVERTER						
ADDR current leakage	I_{ADDR_LKG}	V_{ADDR} = 0V to 5V			±5	µA
Minimum Guaranteed Decoding Window Range			-5		5	%
DIGITAL OUTPUTS ($\overline{ALERT}$, SDA)						
Output-High Leakage Current		Pullup 0V and 5.5V	-10		10	µA
Output Low Level		Sinking 1mA			0.4	V
I^2C DYNAMIC CHARACTERISTICS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Set-Up Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			ns
DATA Valid time	$t_{SU;DAT}$				0.45	µs
DATA Set-Up time	$t_{SU;DAT}$		50			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Noise suppression on SCL and SDA	NS_{I2C}			50		ns
ESD PROTECTION (ALL PINS)						
ESD Protection Level	V_{ESD}	Human Body Model		±2		kV
ESD PROTECTION (HVDP, HVDM, HVCC1, HVCC2, SHLD_SNS)						
ESD Protection Level	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±15		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air-Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		

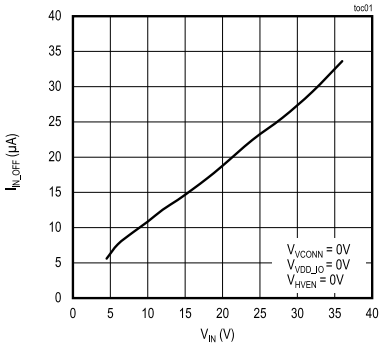
Note 3: Specifications with minimum and maximum limits are 100% production tested at T_A = +25°C and are guaranteed over the operating temperature range by design and characterization. Actual typical values may vary and are not guaranteed.

Note 4: Guaranteed by design and bench characterization. Limits are not production tested.

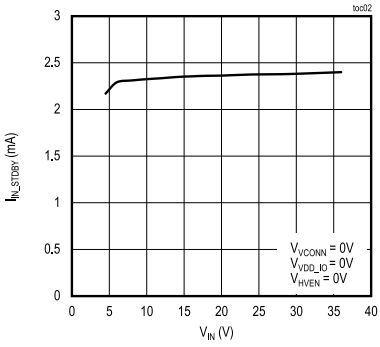
Typical Operating Characteristics

(V_{IN} = 14V; V_{HVEN} = V_{IN}; V_{VCONN} = 5V; V_{VDD_IO} = 3.3V; T_A=25°C, unless otherwise noted)

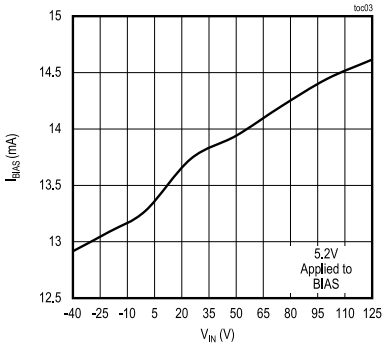
SHUTDOWN CURRENT vs. INPUT VOLTAGE



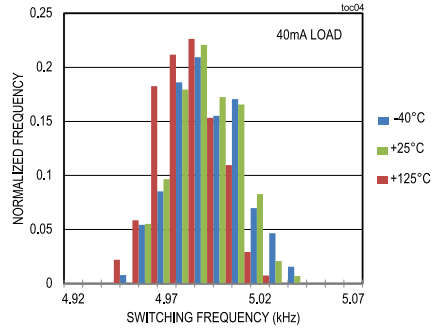
STANDBY CURRENT vs. INPUT VOLTAGE



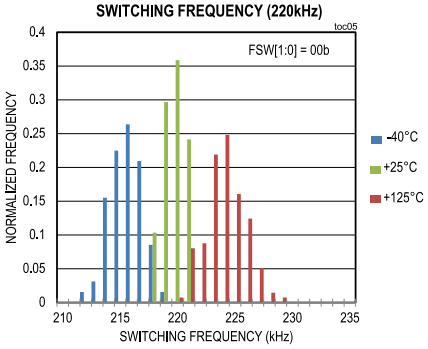
BIAS CURRENT vs. TEMPERATURE



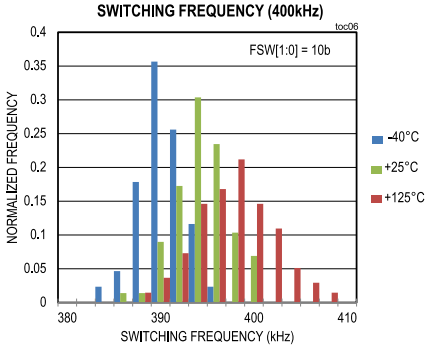
BIAS VOLTAGE VS TEMP



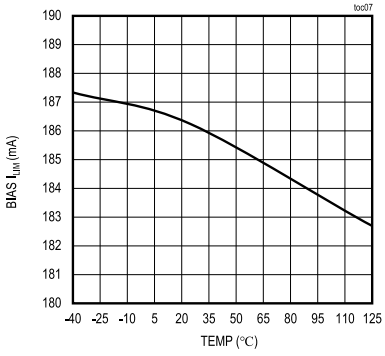
SWITCHING FREQUENCY (220kHz)



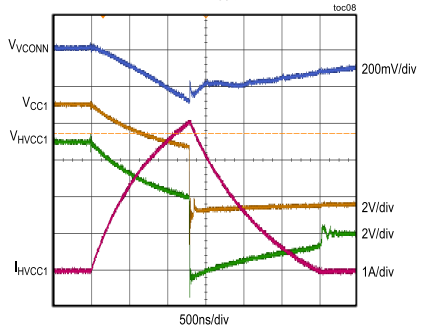
SWITCHING FREQUENCY (400kHz)



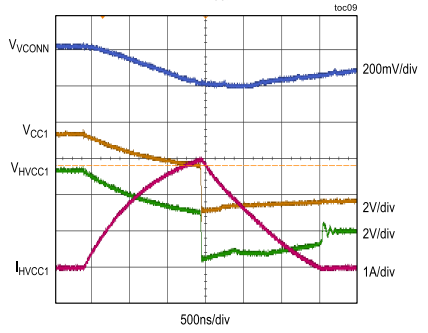
BIAS I_{LIM} vs. TEMPERATURE



VCONN SHORT-TO-GROUND RESPONSE (V_{VCONN} = 5V)



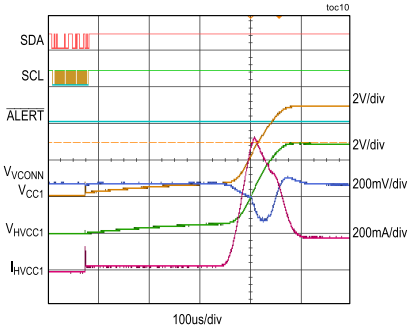
VCONN SHORT-TO-GROUND RESPONSE (V_{VCONN} = 3.3V)



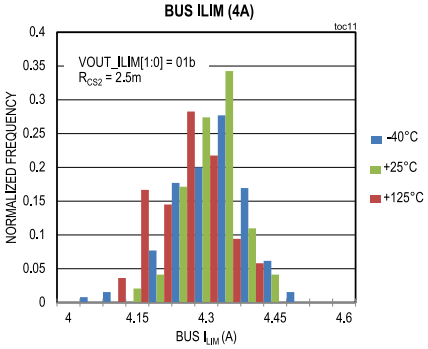
Typical Operating Characteristics (continued)

(V_{IN} = 14V; V_{HVEN} = V_{IN}; V_{VCONN} = 5V; V_{VDD_IO} = 3.3V; T_A=25°C, unless otherwise noted)

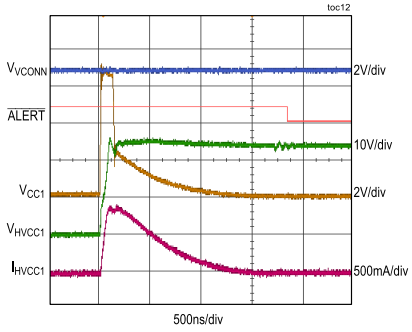
VCONN ENABLED INTO COMPLIANT LOAD (V_{VCONN} = 5V)



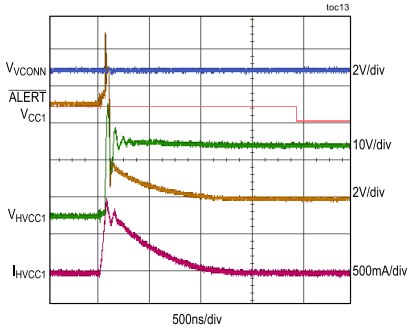
BUS ILIM (4A)



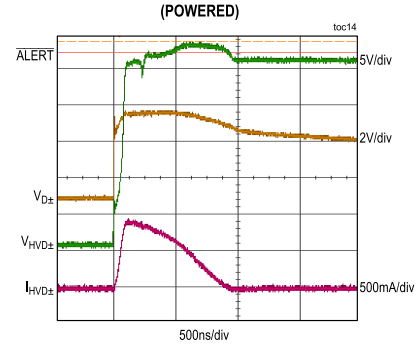
HVCC SHORT-TO-VBUS 24V (POWERED) (VCONN OFF)



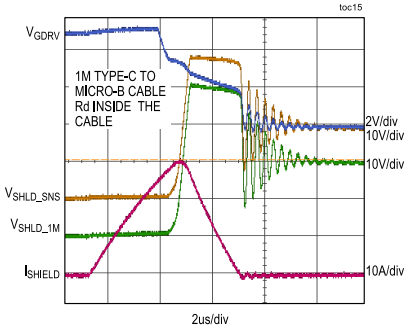
HVCC SHORT-TO-VBUS 24V (POWERED) (VCONN ON)



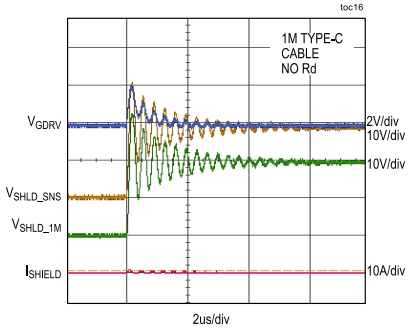
HVD± SHORT-TO-VBUS 24V (POWERED)



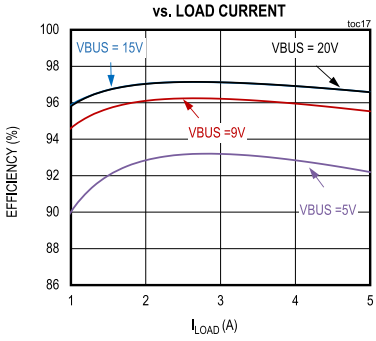
SHIELD SHORT-TO-VBUS 24V



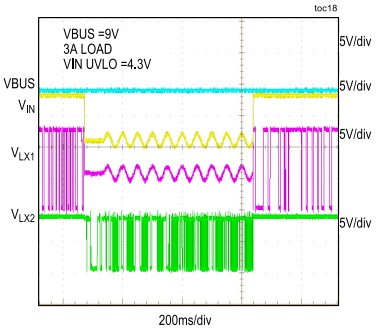
SHIELD SHORT-TO-VBUS 24V



BUCK-BOOST EFFICIENCY vs. LOAD CURRENT



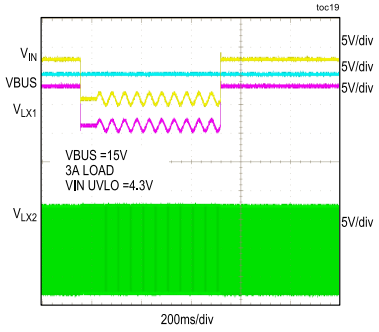
WARM CRANK



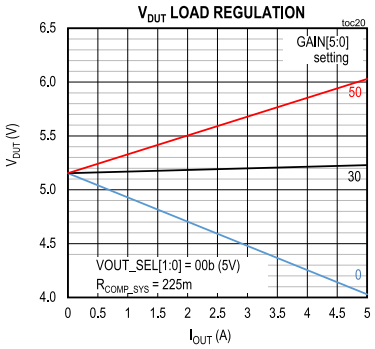
Typical Operating Characteristics (continued)

(V_{IN} = 14V; V_{HVEN} = V_{IN}; V_{VCONN} = 5V; V_{VDD_IO} = 3.3V; T_A=25°C, unless otherwise noted)

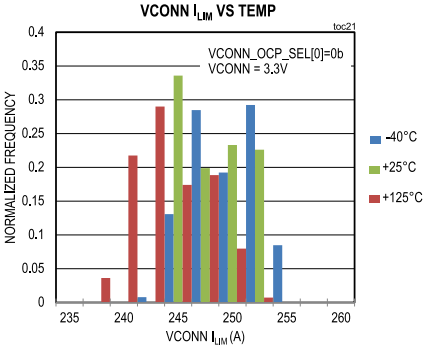
WARM CRANK



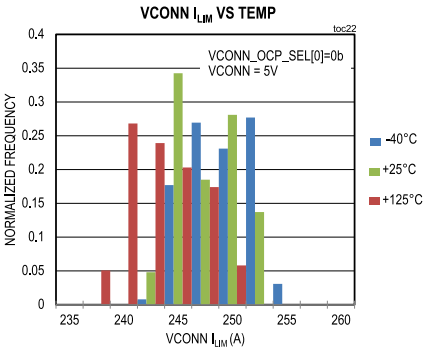
V_{DUT} LOAD REGULATION



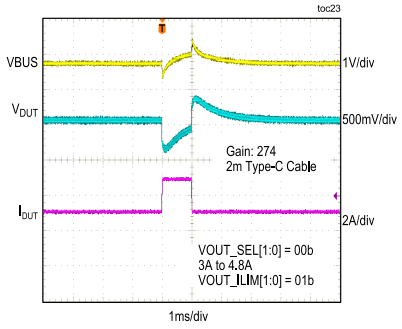
VCONN I_{LIM} VS TEMP



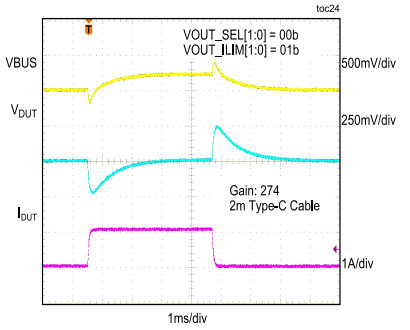
VCONN I_{LIM} VS TEMP



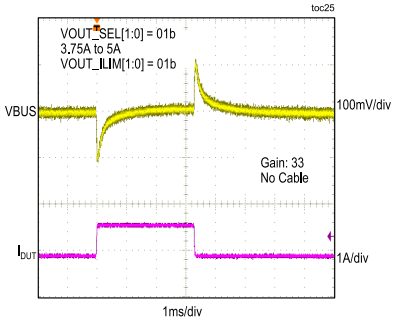
MFi R33 OVERCURRENT RESPONSE



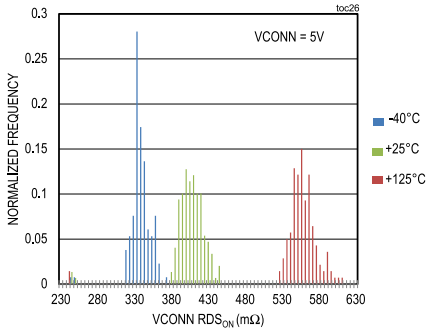
LOAD STEP RESPONSE 80mA to 1A



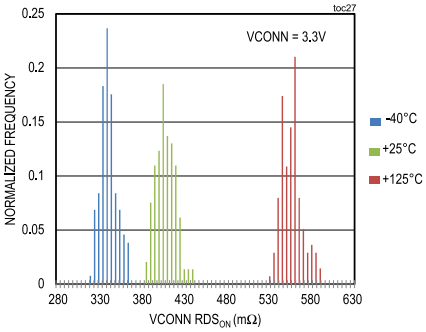
USB-PD LOAD TRANSIENT



VCONN RDSON vs. TEMP

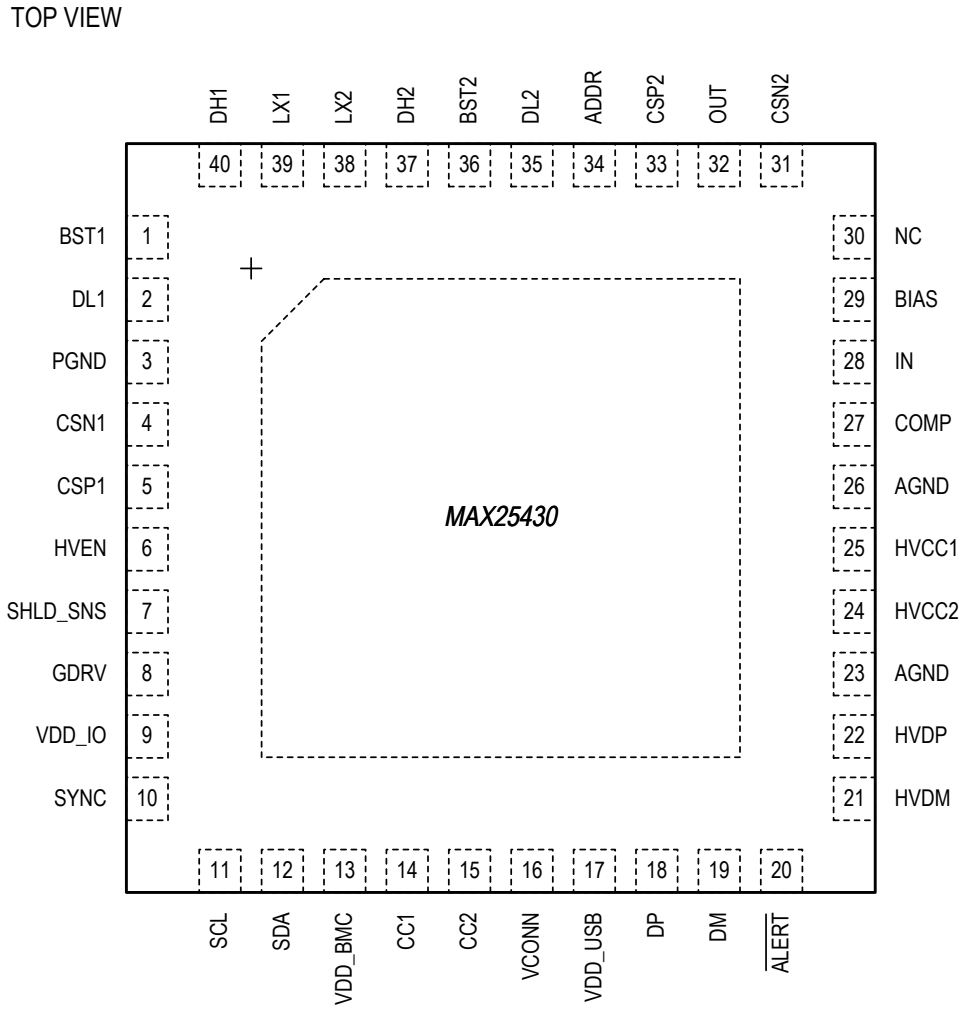


VCONN RDSON vs. TEMP



Pin Configuration

MAX25430



Pin Description

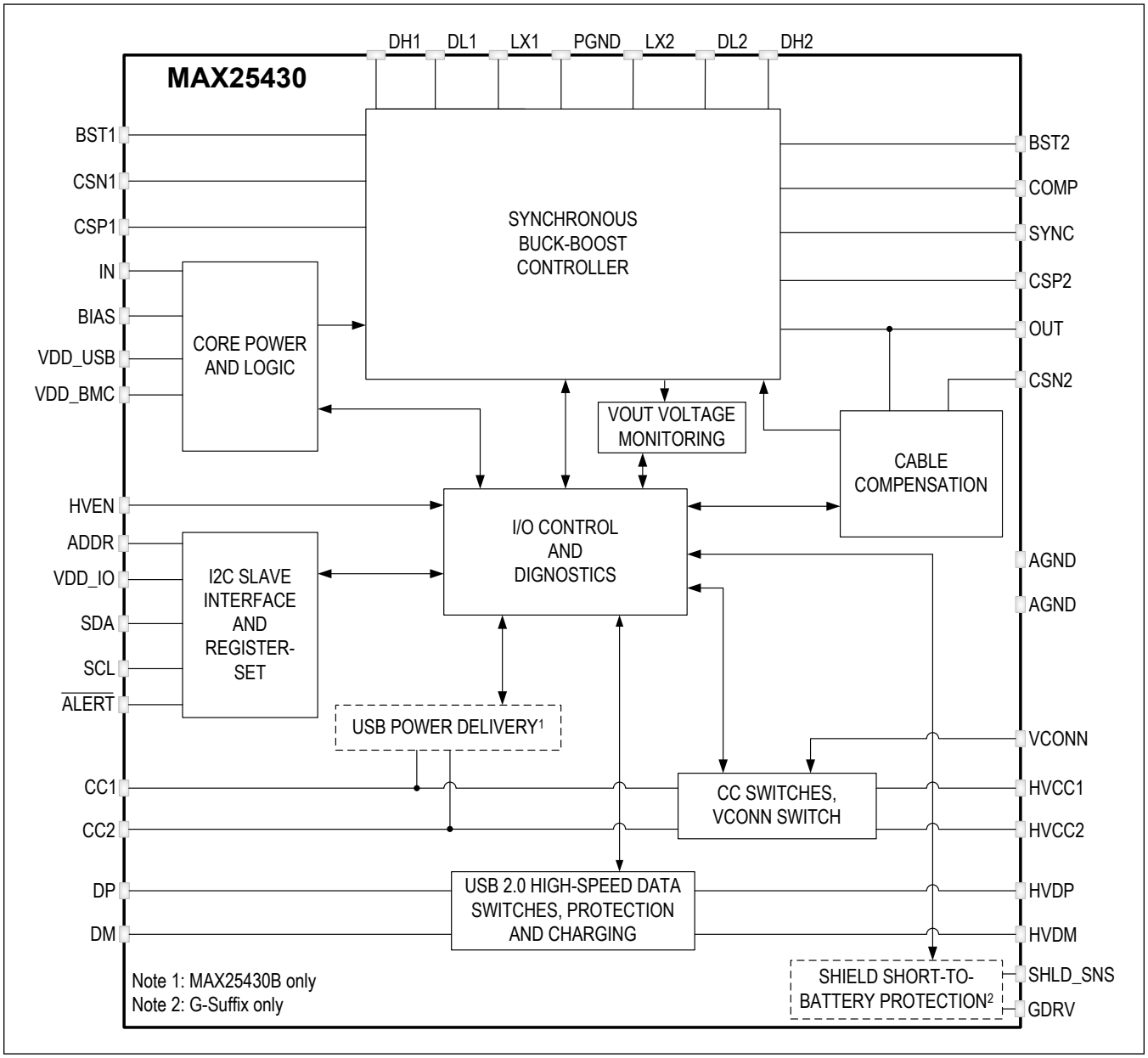
PIN	NAME	FUNCTION
1	BST1	Bootstrap Capacitor Pin for High-Side Driver of LX1 Node. Connect a 0.1µF capacitor between BST1 and LX1.
2	DL1	Buck Low-Side Gate Drive Output. Connect to gate of Q_{b1} external N-Channel FET.
3	PGND	Buck-Boost Power Ground. Connect directly to GND. Connect to GND pour underneath IC.
4	CSN1	Negative Terminal of the Input High-side Current-Sense Amplifier. Connect CSN1 as close to R_{CS1} as possible using a Kelvin sense routing.
5	CSP1	Positive Terminal of the Input High-Side Current-Sense Amplifier. Connect CSP1 as close to R_{CS1} as possible using a Kelvin sense routing.
6	HVEN	High Voltage Enable Input. Driving HVEN high powers-up the IC. This pin can be connected directly to Battery Voltage or Car Accessory Power. This pin can also be driven by a 3.3V or 5V general purpose output from a microcontroller.
7	SHLD_SNS	Shield Short-to-Battery Protection Sense Pin. Available on G-Suffix devices only. In order to protect against shield short-to-battery events, connect SHLD_SNS to the drain of the external shield n-channel FET, which is connected to the SHIELD and GND pins of the USB Type-C receptacle. If not used, or for non-shield short-to-battery devices (F-Suffix), connect to IC GND.
8	GDRV	Shield FET Gate Drive Output. Available on G-Suffix devices only. Connect to the gate of an external n-channel FET to protect against shield short-to-battery events. If not used, or for non-shield short-to-battery devices (F-Suffix), connect a 1MΩ resistor from GDRV to IC GND.
9	V_{DD_IO}	External Input Supply For I^2C Interface. Bypass with 10nF ceramic capacitor to GND.
10	SYNC	Optional Switching Frequency Input/Output for Synchronization with Other Switching Regulators. Leave as input and no connect if not used.
11	SCL	I^2C Clock Pin. Connect to V_{DD_IO} through a pullup resistor.
12	SDA	I^2C Data Pin. Connect to V_{DD_IO} through a pullup resistor.
13	V_{DD_BMC}	MAX25430B: Internal 1.125V regulated supply output. Powers the internal BMC TX driver output. Bypass with 1µF ceramic capacitor to GND. Do not connect external loads to VDD_BMC. MAX25430A: Connect V_{DD_BMC} to GND.
14	CC1	MAX25430A: Protected CC1. Connect to upstream CC1 Configuration Channel of the external USB-PD Controller. MAX25430B: No Connect.
15	CC2	MAX25430A: Protected CC2. Connect to upstream CC2 Configuration Channel of the external USB-PD Controller. MAX25430B: No Connect.
16	VCONN	VCONN Input Supply. Connect to existing 5V or 3.3V supply. Bypass with 10µF ceramic capacitor to GND when using a 3.3V supply. Bypass with 1µF ceramic capacitor to GND when using a 5V supply. Connect to GND if not used.
17	VDD_USB	Regulated Output of the Internal 3.3V LDO. V_{DD_USB} is used for clamping during overvoltage events on HVD+ or HVD-. The regulator also supplies the internal V_{BUS} 10-bit ADC on MAX25430B devices. Bypass V_{DD_USB} with a 1µF ceramic capacitor as close to the pin as possible and with a low-impedance return path to GND. Do not connect external loads to V_{DD_USB}.
18	DP	Protected D+ USB 2.0 Data Path. For CDP applications, connect to low-voltage USB transceiver or HUB IC D+ connection. For DCP applications, connect to GND.
19	DM	Protected D- USB 2.0 Data Path. For CDP applications, connect to low-voltage USB transceiver or HUB IC D- connection. For DCP applications, connect to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
20	$\overline{ALERT}$	Open-Drain Interrupt Output. Indicates alerts to the I^2C Master. Connect a 100kΩ pullup from $\overline{ALERT}$ to V_{DD_IO}.
21	HVDM	High-Voltage-Tolerant D- Connection to Downstream USB Type-C Connector or Captive Cable.
22	HVDP	High-Voltage-Tolerant D+ Connection to Downstream USB Type-C Connector or Captive Cable.
23, 26	AGND	Analog Ground Pin. Connect directly to GND. Connect to GND pour underneath IC.
24	HVCC2	High-Voltage-Tolerant CC2 Connection to Downstream USB Type-C Connector or Captive Cable.
25	HVCC1	High-Voltage-Tolerant CC1 Connection to Downstream USB Type-C Connector or Captive Cable.
27	COMP	Error Amplifier Output. Connect the Type-2 feedback loop compensation network between COMP and AGND.
28	IN	Supply Input for Main IC Power and Internal BIAS Linear Regulator. Bypass IN to GND locally with a 1µF and a 100nF ceramic capacitor.
29	BIAS	Regulated Output of the Internal 5.0V LDO. BIAS powers the internal circuitry. Bypass with a 4.7µF ceramic capacitor from BIAS to AGND.
30	NC	Not Internally Connected. To ensure PCB design retro-compatibility with future USB-PD PPS pin-to-pin compatible products, Maxim recommends placing component footprints for a Type-2 compensation network from the NC pin to AGND. See Future-Proofing Your Design for PPS section. Connect a 0Ω resistor from NC to GND on MAX25430.
31	CSN2	Negative Terminal of the Cable Compensation Current-Sense Amplifier. CSN2 connects to the negative terminal of the cable compensation sense resistor R_{CS3}. Referenced to OUT.
32	OUT	Negative Terminal of the High-Side Output Current-Sense Amplifier and Input to the Internal Feedback Resistor Network. Connect OUT as close to R_{CS2} as possible using a Kelvin sense routing. OUT is also the positive terminal of the cable compensation sense resistor R_{CS3}.
33	CSP2	Positive Terminal of the High-Side Output Current-Sense Amplifier. Connect CSP2 as close to R_{CS2} as possible using a Kelvin sense routing. Referenced to OUT.
34	ADDR	I^2C Slave Address Selection. Connect a resistor to ground to select the last two address bits. Refer to I2C Slave Addressing section for selecting the ADDR resistor.
35	DL2	Boost Low-Side Gate Drive Output. Connect to gate of Q_{b2} external N-Channel FET.
36	BST2	Bootstrap Capacitor Pin for High-Side Driver of the LX2 Node. Connect a 0.1µF capacitor from BST2 to LX2.
37	DH2	Boost High-Side Gate Drive Output. Connect to gate of Q_{t2} external N-Channel FET.
38	LX2	Boost-Side Switching Output Node. LX2 is Hi-Z when the buck-boost is disabled.
39	LX1	Buck-Side Switching Output Node. LX1 is Hi-Z when the buck-boost is disabled.
40	DH1	Buck High-Side Gate Drive Output. Connect to gate of Q_{t1} external N-Channel FET.
-	EP	Exposed Pad. EP must be connected to the ground plane of the PCB.

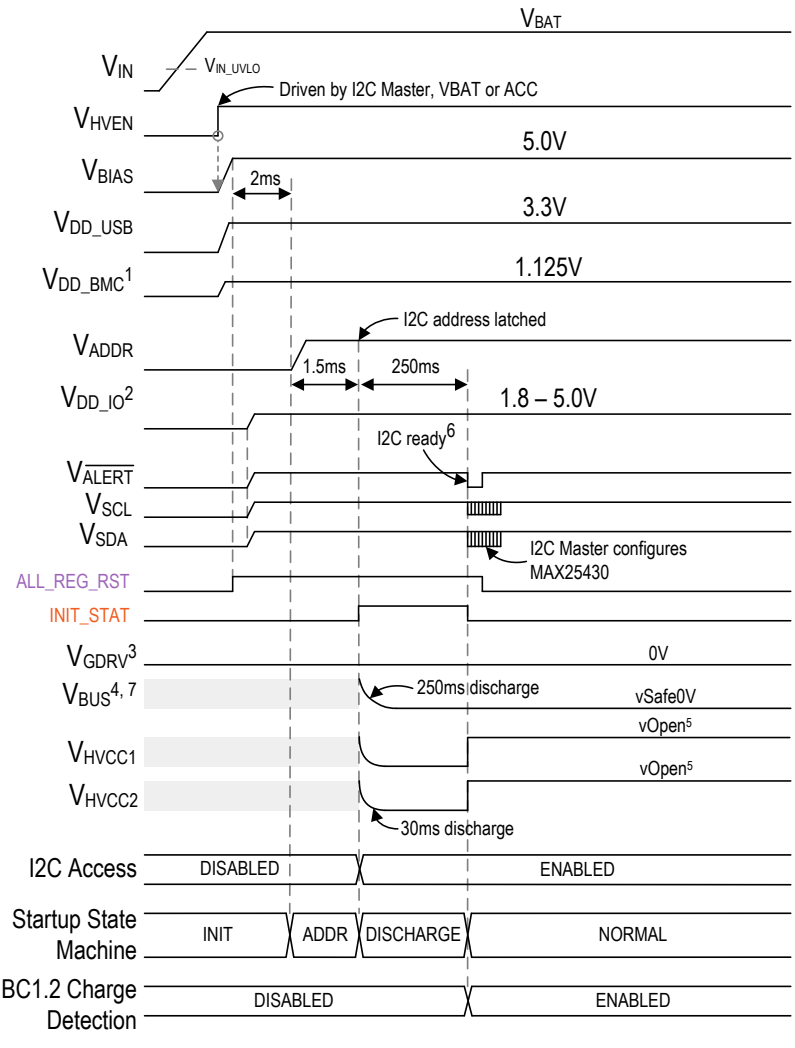
Functional Diagrams

Functional Block Diagram



Functional Diagrams (continued)

Power-up Sequence



Note 1: MAX25430B only.
Note 2: Externally powered. VDD_IO does not gate MAX25430 power-up.
Note 3: G-Suffix only. GDRV will stay low until a device is attached.
Note 4: VBUS will stay at vSafe0V until the TCPM sends the enable command.
Note 5: MAX25430A: External PD Controller turns its Rp pull-ups on.
MAX25430B: Internal Rp pull-ups on.
Note 6: $\overline{\text{ALERT}}$ pin will stay high until startup discharge sequence is complete.
Note 7: Gray areas are undefined voltages.

Key
7: Read Only
6: Write 1 to Clear, Read

IOS Sections

Detailed Description

The MAX25430 is a USB-PD charging and protection solution for multimedia hub, rear-seat entertainment module, and head-unit applications. Combined with either a microcontroller or a USB power delivery controller it is a two-chip solution for dedicated charging module applications. MAX25430 provides all the functionality for USB-PD car battery to V_{BUS} regulation, configuration channel communication, BC1.2 Charge Detection, and USB 2.0 Hi-Speed protection. The devices integrate all the protection needed in an automotive application for a USB-PD application.

The MAX25430 offers the design engineer two options for firmware development. MAX25430B can operate with a SOC, USB Hub IC, or microcontroller whereas MAX25430A is designed to operate with a USB power delivery controller. The MAX25430 EVKIT offers a platform where the design engineer can begin early firmware development.

Recent advancements in the automotive infotainment market demand high-efficiency and low foot-print power delivery solutions. The push for lower BOM cost has driven USB power applications to integrate more features and responsibilities into a single IC. The proliferation of battery-powered portable devices has resulted in an increase in the number of USB ports in an automobile to charge the battery of the devices. In a USB Type-C solution where a dedicated microcontroller is used for detection and protocols, the use of multiple dedicated microcontrollers for each USB port increases the cost and size of the solution. This challenge is solved by using a single microcontroller as a USB Type-C Policy Manager (TCPM) that is operating as a master, and multiple USB Type-C port controllers operating as slaves. The TCPM and TCPC communicate with each other using I^2C.

The MAX25430B is an advanced automotive integrated USB power delivery solution that combines the TCPC along with other USB features such as Type-C, Power Delivery (PD), BC1.2, Apple® and Samsung® charging port emulator. All MAX25430 devices implement Maxim's proprietary current-mode buck-boost H-bridge controller that can achieve a target USB output voltages with high-efficiency while operating with a wide range of input voltages. The buck-boost controller in MAX25430 has robust protection mechanisms such as overvoltage, undervoltage, overcurrent, short-to-ground, short-to-battery, overtemperature, and automotive ESD protection. The MAX25430 has internal gate drivers implemented to drive external power FETs to accommodate high-power USB requirements. The MAX25430 has an intelligent voltage adjustment circuit that can adjusts the output voltage of the buck-boost converter such that the voltage on the USB receptacle is within specifications regardless of the output current.

All MAX25430 devices have integrated data switches and CC switches that protect the upstream USB Transceiver and/or PD Controller from high-voltage events on the cable or the receptacle. All devices also have an integrated VCONN switch to supply power on one of the unused CC pins in different configurations. The high-voltage DP/DM pins (HVDP/HVDM) and CC pins (HVCC1/HVCC2) are monitored and protected for overvoltage conditions such as ESD or short-to battery/V_{BUS} events. With reference to the configuration requested by the TCPM, MAX25430B has the capability to source different currents on the HVCC pins for a Type-C interface and also supports Biphase Mark Coding (BMC) communication using integrated USB-PD analog front-end (AFE) circuits.

Features

- Integrated Buck-Boost DC-DC controller with drivers to drive 4 external MOSFETs in an H-Bridge configuration
  - 4.5V to 36V (40V Load Dump) Input Voltage allows operation in “cold-crank” and start/stop conditions
  - Common USB-PD VBUS voltage outputs up to 5.0A
    - MAX25430A and MAX25430B offer 5V, 9V, 15V and 20V fixed voltages
  - 3 Switching Frequency options for scalable efficiency, adjustable EMI interference avoidance and power optimization including 220kHz, 300kHz and 400kHz
  - Forced-PWM at Light or No-Load conditions for reduced EMI through USB cable
  - Spread Spectrum option for EMI Reduction
  - SYNC Input and SYNC Output for frequency parking and multi-port applications
  - Reduced inrush current with Soft-Start
  - Thermal Shutdown
- Integrated USB-PD VBUS Features
  - Programmable VBUS Over-Current Protection Limits

  - Programmable VBUS Under-Voltage Protection Limits
  - Programmable VBUS Over-Voltage Protection Limits
  - Digital Voltage Scaling (DVS) for smooth, predictable voltage transitions
  - Integrated USB VBUS Discharge
- Integrated Watchdog timer for guaranteed safe operation
- Integrated Output Voltage Adjustment for Cable Voltage Drop on Captive-Cable Applications
  - Programmable Voltage Gain Up to 3 Meters/Up to 500mΩ of cable resistance
- 1MHz I2C Slave Interface with $\overline{\text{ALERT}}$ pin
  - TCPCI compliant register set
  - MAX25430 specific registers for alerts, advanced diagnostic and management
  - Maskable alerts for application specific behavior
  - Selectable I2C address for multi-port applications
- MAX25430A devices provide an integrated 2-input to 2-output USB Type-C CC1 & CC2 4Ω (typ.) switches for external USB-PD Controller
- MAX25430B devices provide a single-port Type-C DFP Port Controller (TCPC) compliant USB Power Delivery PHY for an external TCPM
  - Designed to comply with Type-C, USB-PD and TCPC specifications
    - USB Type-C Revision 1.3
    - USB Power Delivery Revision 2.0, and Revision 3.0 Version 1.2
    - USB Inter-Block Specification Revision 2.0 Version 1.1
  - Implements Type-C Configuration Channel (CC) interface and USB-PD Physical layer functions to a Type-C Port Manager (TCPM) that handles PD Policy management
    - Type-C Cable plug orientation detection
    - Type-C Detection supporting default, 1.5A or 3.0A current capabilities
  - 10-bit SAR ADC for VBUS Voltage Monitoring
  - Programmable VBUS Alarm Thresholds
- Integrated 1W 450mΩ (typ.) VCONN switch and VCONN Over-Current Protection removing need for dedicated VCONN DC-DC and use of common voltage rail in the application
  - 3.0V to 5.5V input voltage support
  - 1W threshold OCP protection
  - Fast VCONN input Under-Voltage Protection
  - Intelligent soft-start and Auto-Retry for non-compliant VCONN loads
  - Integrated VCONN Discharge on HVCC1 and HVCC2 pins
  - I2C Control saves two GPIOs on the USB-PD Controller
- Integrated Module Input Fuse Protection
  - Programmable VIN Under-Voltage Protection Threshold
  - Fast detection of fuse blow condition
  - Quick alert reporting to I2C master for resolution
- Integrated Protection for Cable Shield-Short-to-Battery faults preventing cable, passenger device and car module damage.
  - Fast detection of cable shield over-current
  - Fast turn-off of external protection switch
  - Safe dissipation of inrush energy
  - Fault reporting and auto-retry for fault removal
- Integrated Automotive Protection on VBUS output
  - Fixed 7.5A VBUS Circuit-Breaker Limit
  - Automatic Short-to-GND Fault Detection and Diagnostic
- Supports USB BC1.2 Charging Downstream Port (CDP) Dedicated Charging Port (DCP), and High-Speed Passthrough Modes

  - USB D+/D- Protection and Host Charger Emulator
  - Integrated HVDP/HVDM Apple® and Samsung® Charge Detection Termination Resistors
  - Compatible with USB On-The-Go Specification and Apple CarPlay®
  - Supports Chinese Telecommunication Industry Standard YD/T 1591-2009
  - Integrated 1GHz 3dB BW Data Switches supporting USB 2.0 480Mbps/12Mbps/1.5Mbps communication
  - Auto-DCP mode compatible with Oppo® and OnePlus® devices.
- Apple® MFi R33 Overcurrent Compatible
- Integrated Robust High-Voltage Protection for the USB-PD or TCPM controller from events at the receptacle or captive cable
  - 24V (MAX) Over-Voltage Protection on HVCC1/HVCC2
  - 24V (MAX) USB 2.0 Over-Voltage Protection on HVD+/HVD-
  - Automatic Fault Detection and Retry
  - Fault Indication via Active-Low Open-Drain $\overline{\text{ALERT}}$ Output (maskable)
  - Short-to-Battery and Short-to-Vbus Protection
- Automotive Grade ESD Protection on USB HVD+, HVD-, HVCC1, HVCC2 and SHLD_SNS pins
  - ±15kV Air/±8kV Contact IEC 61000-4-2
  - ±15kV Air/±8kV Contact ISO 10605

MAX25430A and MAX25430B Differences

Table 1. Differences Between MAX25430A and MAX25430B Devices

Function	MAX25430A	MAX25430B
Startup	No Difference	
Buck-Boost and V_{BUS} Power	No Difference	
CC Protection Switches	No Difference	
USB Data Switches & Charge Detection	No Difference	
Cable Shield Short-to-Battery Protection (G-Suffix only)	No Difference	
VCONN	No Difference	
I^2C	No Difference	
Watchdog	No Difference	
Fault Reporting, Action and Recovery	No Difference	
Type-C Interface (Rp, VRd/VRa)	No	Yes
USB Power Delivery PHY (BMC Driver)	No	Yes
V_{DD_BMC} Internal Supply	Off	On (1.125V)
V_{BUS} ADC & Alarms	No	Yes

Document Conventions

Whenever "MAX25430" is mentioned in this document, the corresponding description, figure or diagram applies to all MAX25430 devices.

Whenever "MAX25430A" is mentioned in this document, the corresponding description, figure or diagram only applies to MAX25430A devices.

Whenever “MAX25430B” is mentioned in this document, the corresponding description, figure or diagram only applies to MAX25430B devices.

Whenever “G-Suffix” is mentioned in this document, the corresponding description, figure or diagram only applies to MAX25430 devices with the G-Suffix.

References

Table 2 shows the references specifications, their locations and the common names they are referred to in this document.

Table 2. References

Referred to In This Document	Title	Location
The USB-PD Specification	Universal Serial Bus Power Delivery Specification Revision 3.0, Version 1.2 June 21, 2018	http://www.usb.org
The USB Type-C™ Specification	Universal Serial Bus Type-C Cable and Connector Specification Release 1.3 July 14, 2017	http://www.usb.org
The TCPCI Specification	Universal Serial Bus Type-C™ Port Controller Interface Specification Revision 2.0, Version 1.1 March 2020	http://www.usb.org
The USB 2.0 Specification	Universal Serial Bus Specification Revision 2.0 April 27, 2000	http://www.usb.org
The USB 3.x Specification	Universal Serial Bus 3.2 Specification Revision 1.0 September 22, 2017	http://www.usb.org
The USB BC1.2 Specification	Battery Charging Specification Revision 1.2 December 7, 2010	http://www.usb.org

Power-Up and Enabling

When a valid voltage is applied to IN and HVEN is high, MAX25430 goes through its power-up sequence as described in the *Power-up Sequence* functional diagram.

The MAX25430 power-up sequence is done when $\overline{ALERT}$ asserts low after HVEN went high with V_{IN} > UVLO. The V_{DD_IO} input must be within a valid voltage to perform I^2C communication with MAX25430 and provide a pullup voltage to the $\overline{ALERT}$ pin.

IN Supply Input

IN is the input supply for MAX25430 and the external H-bridge buck-boost converter. The MAX25430 can operate with a V_{IN} voltage in the range of 4.5V to 36V and is load-dump tolerant up to 40V. A 1µF ceramic capacitor with appropriate voltage rating should be connected for decoupling from IN to GND. An additional 100nF closer to the IN pin is recommended for improved high-frequency decoupling for internal circuitry.

To prevent large input current tripping an upstream automotive fuse during high output power at low input voltage, the MAX25430 integrates a programmable input undervoltage lockout. When the input voltage is below the undervoltage lockout threshold, the buck-boost controller is turned off, which prevents high current being drawn at the input. The undervoltage lockout is set by the IN_UV_THRESH[3:0] register. This voltage can be programmed in the range of 4.5V to 8.5V in steps of 0.4V. The default setting for the undervoltage lockout threshold is 7.3V and can be changed on the fly after power-up via I^2C. The UVLO threshold includes a blanking time of 150µs (typ.), which prevents the device from turning off during input voltage transients.

High Voltage Enable Input (HVEN)

HVEN is used as the main enable to the device and initiates MAX25430 start-up and configuration. If HVEN is at a logic-low level, the device enters the Off mode, with low quiescent current level on IN. HVEN is compatible with inputs from 3.3V logic, up to automotive battery voltages.

BIAS Linear Regulator Output

The device includes an internal 5V linear regulator (BIAS) that provides power to the internal circuit blocks. The IC powers

up once the voltage on BIAS crosses the undervoltage-lockout (UVLO) rising threshold and shuts down when BIAS falls below the UVLO falling threshold. Connect a 4.7µF ceramic capacitor from BIAS to GND for proper operation of the linear regulator. Refer to *PCB Layout Guidelines* for more information.

External loads, such as an MCU or PD Controller, can be connected to BIAS as a power supply as long as:

- The total BIAS current, including internal circuitry, is below 60mA. Make sure to account for the internal buck-boost drivers current consumption when the H-bridge is switching. The usable current for external loads varies depending on operating conditions.
- The power dissipated by the internal BIAS LDO does not cause MAX25430 to exceed the maximum Continuous Power Dissipation or Junction Temperature as specified in the Absolute Maximum Ratings section.

V_{DD_USB} Linear Regulator Output

The MAX25430 integrates a 3.3V low-dropout linear regulator. The V_{DD_USB} output is used as a clamping voltage during high-voltage events such as short-to-battery or ESD strikes on HVDP/HVDM pins. The V_{DD_USB} output is also used to power the internal V_{BUS} 10-bit ADC on MAX25430B devices. This regulator uses the 5V BIAS regulator as its input. Connect a 1µF ceramic capacitor from V_{DD_USB} to GND for proper operation of the linear regulator. Refer to *USB PCB Layout Guidelines* for more information.

MAX25430 includes an output undervoltage comparator that sets the read-only VDD_USB_UV status bit when the regulator output goes below $V_{DD\_USB\_UV}$ = 2.7V (typ).

An output overvoltage comparator is also included, which sets the read-only SHIELDING status bit when the regulator output goes above $V_{DD\_USB\_OV}$ = 4.0V (typ).

The V_{DD_USB} 3.3V LDO cannot be used to power external loads.

V_{DD_BMC} Linear Regulator Output (MAX25430B only)

The MAX25430B integrates a 1.125V (typ.) regulated voltage reference required for BMC communication. Connect a 1µF ceramic capacitor from V_{DD_BMC} to GND for proper operation of the linear regulator. Refer to *USB PCB Layout Guidelines* for more information. Connect the pin directly to GND on MAX25430A devices.

V_{DD_IO} Input

The V_{DD_IO} pin must be connected to the external 1.8V, 3.3V or 5.0V V_{DD} rail used for I^2C communication by the I^2C Master (MCU, HUB or PD-Controller).

V_{DD_IO} is used as the pullup voltage for SCL, SDA and $\overline{ALERT}$ pin.

I^2C communication can begin as soon as the power-up sequence is done (i.e. $\overline{ALERT}$ asserts low after HVEN goes high with $V_{IN} > U_{VLO}$) and the V_{DD_IO} input is within a valid voltage.

In an application where neither 1.8V, 3.3V or 5.0V external supplies are available, V_{DD_IO} pin can be tied to V_{DD_USB} or BIAS directly. It is recommended to place a 10nF ceramic capacitor from V_{DD_IO} pin to GND to provide local decoupling. The V_{DD_IO} input voltage can withstand a maximum voltage of 6V.

VCONN Supply Input

The device requires an external supply on the VCONN input to provide the required power for the VCONN switch. The input voltage range for the VCONN input is 3.0V to 5.5V but in the actual application, the input voltage will be either 3.3V or 5.0V. Refer to the *VCONN Switch* section for more information on this feature.

Buck-Boost Controller

The MAX25430 integrates a buck-boost controller and drivers that provide power from the car battery to V_{BUS}. The buck-boost controller operates for input voltage ranges from 4.5V to 36V, and is 40V load-dump tolerant.

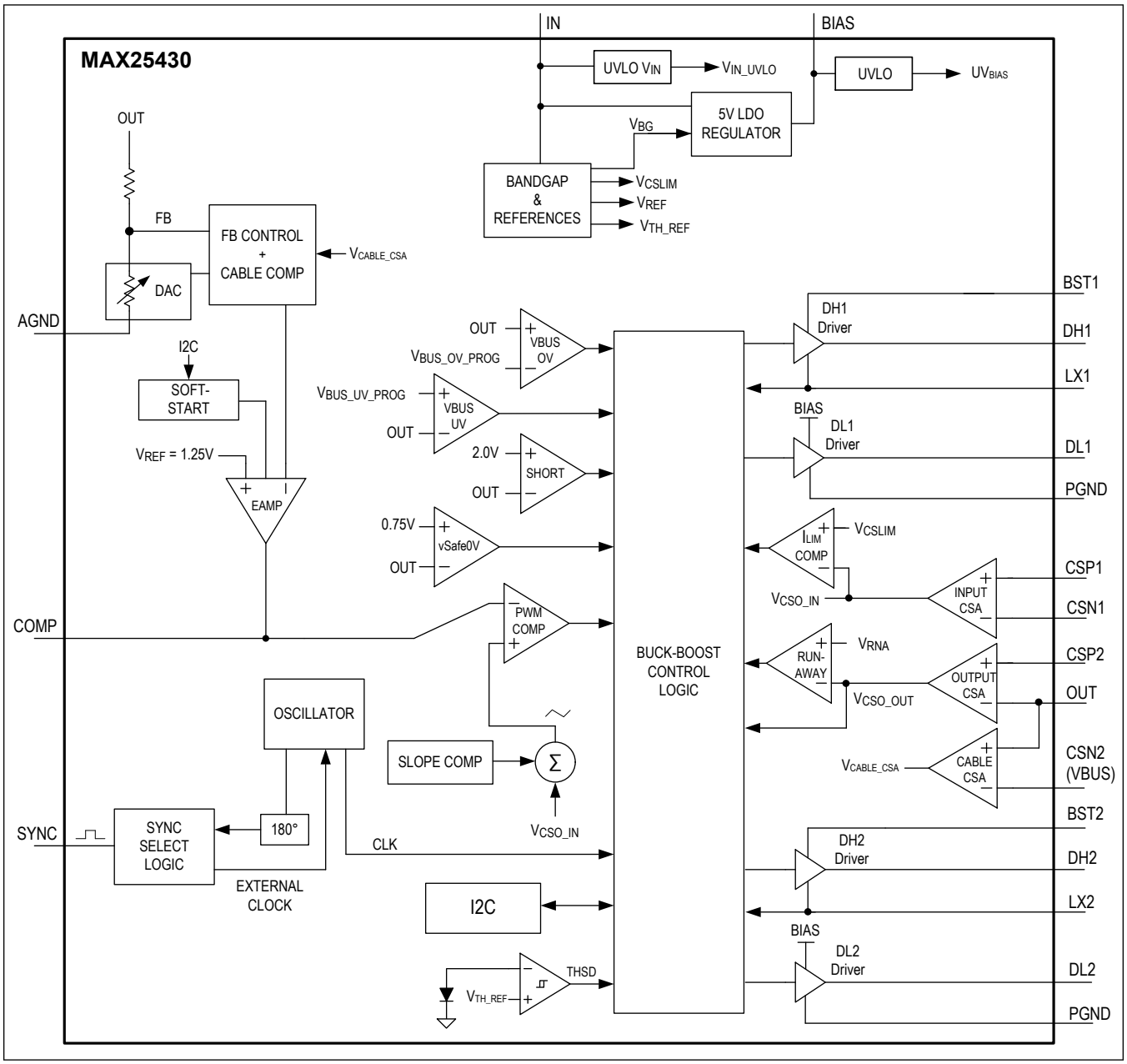


Figure 1. Buck-Boost Block Diagram

The integrated buck-boost controller operates in either a buck or a boost depending on the input and output voltage. The buck-boost will transition seamlessly between these modes to maintain a constant output voltage. This seamless four-switch buck-boost transition method ensures V_{BUS} does not droop during V_{IN} transients and helps achieve excellent

efficiency, load regulation, and line regulation. The architecture consists of a peak current-mode control loop that senses the inductor current using an external current-sense resistor on the input side (R_{CS1}). The slope compensation value can be adjusted in steps of 100mV by the SLP[2:0] register from 100mV to 800mV so as to prevent sub-harmonic oscillations. The switching frequency is also set by writing to the FSW[1:0] register. Three switching frequency options 220kHz, 300kHz and 400kHz are available in the device. To alleviate EMI problems the IC integrates a programmable spread spectrum on the switching frequency oscillator. The SS_SEL[1:0] register is used to set the desired amount of spread spectrum. The spread spectrum can be programmed to be ±3%, ±6% and ±9% of the set switching frequency. The output voltage is fed back to the controller using an internal resistor divider on the OUT pin. The buck-boost control-loop is compensated externally using an RC network on the COMP pin. An output current-sense resistor (R_{CS2}) between CSP2 and OUT provides programmable overcurrent protection (V_{BUS} I_{LIM}, V_{BUS} OCP), as well as protection from runaway currents (V_{OC2}), short-to-battery, short-to-ground conditions and excessive negative currents. A third and optional current sense resistor (R_{CS3}) can be placed between OUT and CSN2 to provide USB cable/voltage drop compensation in order to maintain a constant V_{BUS} voltage at the user port across output current variations.

Enabling VBUS

Before enabling V_{BUS}, ensure the I^2C Master performs the following initial configuration after power-up:

1. The V_{BUS} overcurrent limit has been set accordingly. Always use a higher threshold than the maximum operating output current. Refer to *VBUS Overcurrent Detection*.
2. The cable compensation gain has been selected to offset any PCB trace/connector and/or cable drop. Refer to the *Cable Compensation*.
3. The slope compensation peak ramp voltage is correctly set per the system requirements. Refer to *Slope Compensation*.
4. The switching frequency and desired spread spectrum settings are correctly set per the system requirements. Refer to *Switching Frequency and Spread Spectrum*.
5. The SYNC pin direction is selected. By default, the SYNC pin acts as an input. Refer to *Synchronization Input/Output (SYNC)*.
6. The V_{BUS} undervoltage and overvoltage thresholds and masks are correctly configured for the application. By default, the 12.5% UV/OV thresholds are selected. Refer to the *VBUS_THRESH* register description.
7. No fault has been reported by the MAX25430 through the SHIELDING bit or dedicated V_{BUS} Fault flags. Refer to *Fault Table (Maxim Auto-Shield)*.
8. V_{BUS} needs to be at vSafe0V first before being enabled. Make sure VSAFE0V bit in the EXTENDED_STATUS[7:0] register reads logic '1'.
9. If a V_{BUS} pre-bias condition exists, the I2C Master needs to attempt a Force Discharge first using MAX25430 integrated force discharge functionality. MAX25430 will issue an I^2C error if V_{BUS} is not at vSafe0V prior to being enabled. Refer to the *VBUS Discharge* and *Fault Table (Maxim Auto-Shield)*.

To comply with the USB-IF TCPCI specification MAX25430 will only source V_{BUS} when the proper command is received from the I^2C Master. In order to enable V_{BUS} :

1. First, write 0x77 (SourceVbusDefaultVoltage) to the COMMAND[7:0] register. MAX25430 will then soft-start to vSafe5V (5.15V typ). Once at vSafe5V, only then can the I^2C Master request for non-5V outputs.
2. Select the desired non-default output voltage by writing to the VOUT_SEL[1:0] register.
3. Write 0x88 (SourceVbusHighVoltage) to the COMMAND[7:0] register. MAX25430 will then transition to the non-default voltage with a USB-PD compliant slew rate.

For more information on specific commands and actions to be performed with MAX25430 to comply with USB Type-C and USB power delivery, contact Maxim Integrated.

Soft-Start

The buck-boost output is enabled by the I^2C master by writing to the COMMAND register. When enabled, the controller will soft-start by gradually ramping up the output voltage from vSafe0V to vSafe5V (5.15V typ.). This soft-start feature reduces inrush current during startup. Soft-start is guaranteed into compliant USB loads. Only after the voltage reaches vSafe5V can the buck-boost output voltage be adjusted to other voltage options by the I^2C master. The typical soft-start time is 6.5ms.

Switching Frequency and Spread Spectrum

The MAX25430 provides a programmable switching frequency and spread spectrum via I^2C. The internal oscillator frequency is set by the FSW[1:0] register. The switching frequency can be programmed to 220kHz, 300kHz or 400kHz.

The spread spectrum can be enabled and adjusted by writing to the SS_SEL[1:0] register. The spread spectrum can be programmed to ±3%, ±6%, ±9% centered on f_{SW}. The default oscillator frequency at power-up is 400kHz with no spread spectrum.

The table below shows the variation of the switching frequency for each spread spectrum setting.

Table 3. Spread-Spectrum Settings vs Switching Frequency

f_{SW}	Spread-Spectrum Modulation Frequency		
	3% Setting	6% Setting	9% Setting
220kHz	±0.67kHz	±1.33kHz	±2.0kHz
300kHz	±0.91kHz	±1.82kHz	±2.73kHz
400kHz	±1.21kHz	±2.42kHz	±3.64kHz

Synchronization Input/Output (SYNC)

MAX25430 integrates a clock synchronization input/output to be used in two-port applications or with other power supplies in the module. The benefits of the synchronization between two switching power supplies are two-fold:

- Reduced input capacitance requirement due to 180-degree out-of-phase current demands which leave time for the input capacitors to recharge between each cycle.
- Reduced EMI due to less input current ripple. This translates to a smaller inductor required for the module input EMI filter.

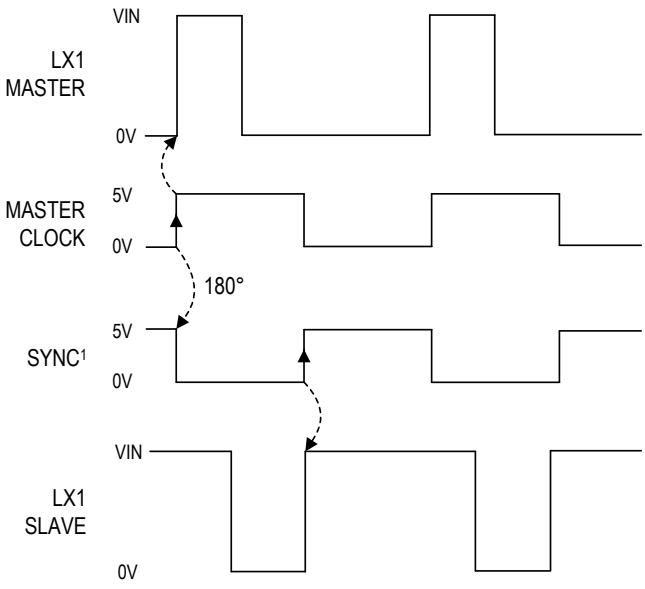
Both the reduced input capacitance requirement and reduced input current ripple help reduce significantly system cost.

The SYNC pin can be configured via I2C as either an input or an output through the SYNC_DIR register. SYNC_DIR is a one-bit register which is set by default to logic '1'. In this case, the SYNC pin on the MAX25430 is expecting an external input signal to synchronize its oscillator to the input on the SYNC pin. If there is no input on this pin, the buck-boost operates with the internal oscillator. Connect SYNC to GND and configure it as an input if not used.

The SYNC_DIR register can be set to logic '0' by the I^2C Master. In this case, the SYNC pin acts as an output and it generates a fixed 50% duty cycle pulse at the Master's switching frequency that is phase shifted by 180 degrees, as shown below. Note only Buck operation is shown. The SYNC feature also supports Boost and Buck/Boost operation.

The internal spread spectrum is disabled if SYNC is configured as an input and synchronized to an external clock.

When configured as an output, the SYNC signal will include the spread spectrum modulation for the Slave to synchronize to.



Note 1: Master's SYNC pin configured as output and tied to Slave's SYNC pin configured as input.

Figure 2. SYNC Operation Diagram

Input Current Limit

MAX25430 features a peak input current limit. The device will limit the input current if the sensed voltage drop across the input current-sense resistor (V_{CSP1}-V_{CSN1}) is above the fixed V_{OC1} threshold (50mV typ.). The current threshold can be selected with the input current-sense resistor value R_{CS1}. Refer to the "Current-Sense Resistors Selection" section.

An input overcurrent event will set the IN_OC status bit to logic '1', which is read only, and will stay set as long as the overcurrent condition is present.

MAX25430 will report the event to the VNDR_ALERT bit in the ALERT_H register if the IN_OC_MASK is unmasked.

$\overline{ALERT}$ pin will assert low if IN_OC_MASK and MSK_VNDR_ALRT bits are unmasked during an overcurrent event.

V_{BUS} Overcurrent Detection

The MAX25430 allows configuration of the V_{BUS} DC overcurrent threshold by the VOUT_ILIM[1:0] bits of the PWR_OUT_CONTROL register. The R_{CS2} external current sense resistor is used to sense the buck-boost output current waveform. The output current information is then averaged and compared to an I^2C programmable threshold. The MAX25430 does not actually limit the output current, instead, if the output current exceeds the programmed threshold for more than 16 ms, the MAX25430 will turn off its output to protect itself and the sink. This allows compatibility with the MFi Overcurrent Specification introduced in the R30 revision in 2018.

Refer to the *Fault Table (Maxim Auto-Shield)* for more information on action, reporting and recovery upon a V_{BUS} I_{LIM} fault.

Table 4 shows the three discrete DC overcurrent detection thresholds available on MAX25430 and the corresponding port current range recommended for each setting. Refer to Typical Operating Characteristics for distribution of the V_{BUS} I_{LIM} threshold.

Table 4. V_{BUS} Current-Limit Detection Thresholds

VOUT_ILIM[1:0]	Overcurrent threshold setting (with R_{CS2} = 2.5mΩ)	Recommended Port Current Rating
00	3.3A	$I_{OUT} \le 2.4A$
01	4.3A	$2.4A < I_{OUT} \le 3.0A$
10, 11	6.0A	$3.0A < I_{OUT} \le 5.0A$

An additional current-limit detection is sensed when IOUT reaches as high as 7.5A (typ.) which will immediately cause the buck-boost controller to turn off.

Refer to *Fault Table (Maxim Auto-Shield)* for more information on action, reporting and recovery upon a V_{BUS} OCP Fault.

V_{BUS} Short-to-GND Comparator

The buck-boost output is protected against a short-to-ground condition. A short-to-ground event is detected when OUT goes below 2.0V (typ.) while V_{BUS} is being sourced. In this case the buck-boost controller is turned off immediately. Refer to Fault Action A in the *Fault Types* table.

Integrated V_{OUT} Pulldown

While the buck-boost is disabled, an active pulldown of 16kΩ (typ.) is switched on to keep V_{BUS} at vSafe0V.

Cable Compensation

The Infotainment Head-Unit contains the electronics and is located in the dashboard. The USB port is a passive implementation located in the center console connected via 3m of cable. To charge mobile devices, the USB current capability could be as high as 5A. Stringent USB port supply voltage limits increase the need for compensation as the voltage drop is not acceptable. The voltage drop compensation is implemented by measuring the current and feeding back the current information to the internal feedback block of the converter. In this implementation, the load regulation of the power supply is effectively changed to compensate a voltage drop on a power line.

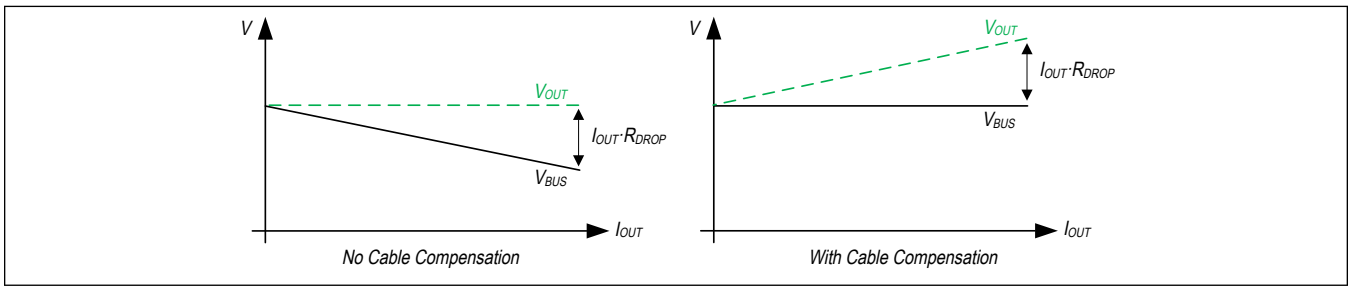


Figure 3. Cable Compensation Benefit

The MAX25430 compensates voltage drops for up to 500mΩ from parasitic resistance present from the OUT pin to the user cable, including but not limited to the USB captive cable, PCB trace and in-line connectors. The cable compensation is designed for the following V_{BUS} voltage and current configurations: 5V, 9V, 15V and 20V at up to 5A. The gain of the cable compensation circuit can be adjusted via I^2C by changing the values in GAIN[5:0] in the cable comp control register CABLE_COMP_CONTROL. The R_{CS3} external current-sense resistor is required when using the cable compensation feature.

Thermal Shutdown

The thermal shutdown protection limits the temperature the device is allowed to reach before forced shutdown. If the die temperature exceeds 165°C, the device will shut down and will need to cool down. Once the device has cooled down by 15°C the device is automatically enabled again (as long as HVEN is still high and V_{IN} is above UVLO). The thermal overload protects the device in the event of overheating. For continuous operation, do not exceed the absolute maximum junction temperature of 150°C. For more information regarding actions and recovery steps taken upon a

thermal shutdown fault, refer to *Fault Table (Maxim Auto-Shield)* and *Fault Types* sections.

USB Type-C and Power Delivery

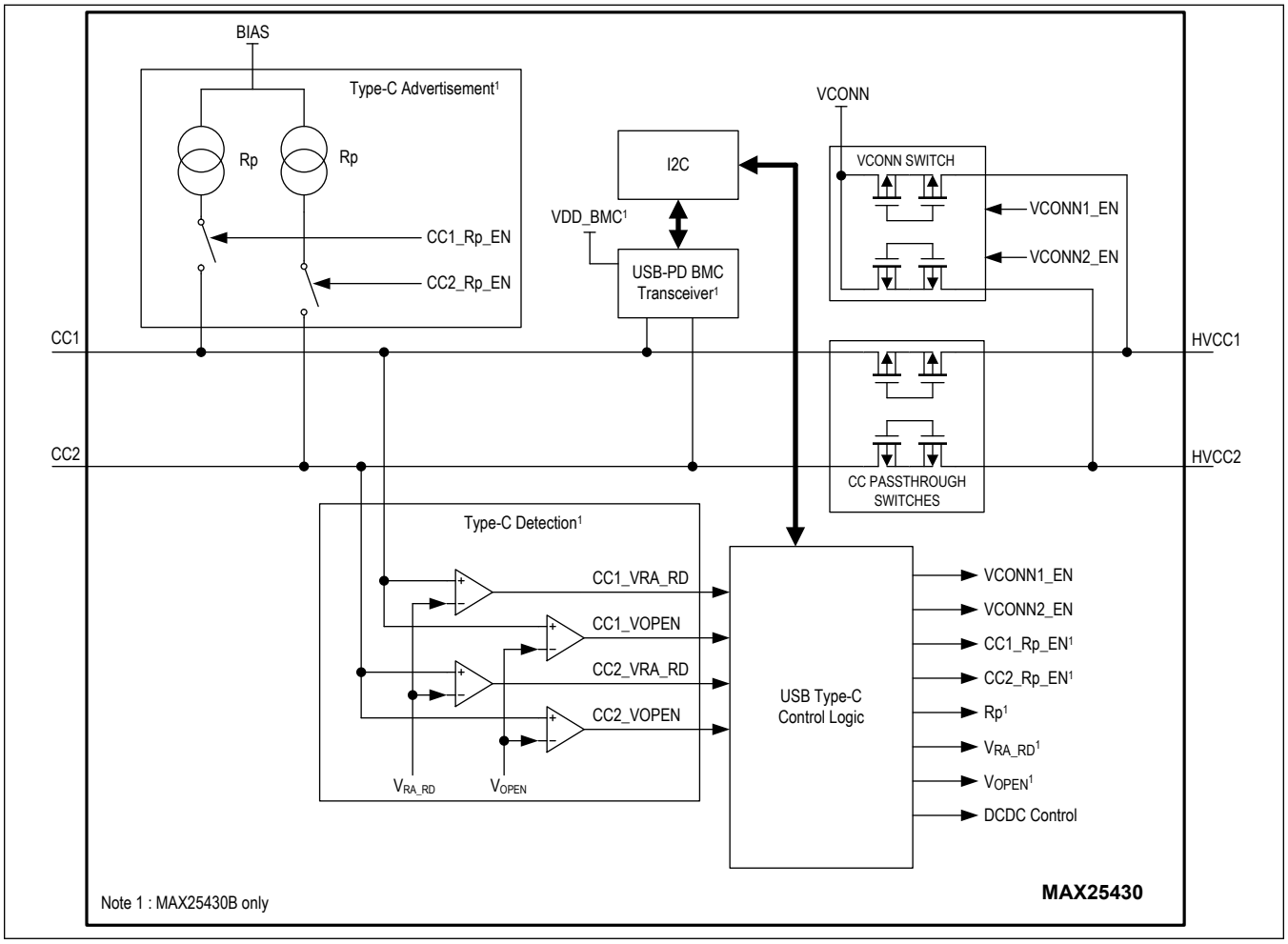


Figure 4. USB Type-C Functional Block Diagram

Detailed functional breakdown of functional block diagrams and operation is provided in the following sections.

Configuration Channel (CC1 and CC2)

To maintain the USB host/device relationship, Type-C requires a configuration channel (CC). It is through the CC lines that current capabilities are advertised and detected, as well as how the host detects the cable orientation, which is required for USB 3.0 and active cables. In the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the source-to-sink connection.

Functionally, the configuration channel (CC) is used to serve the following purposes:

- Detect attach of USB ports, e.g. a source to a sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure V_{BUS}: USB Type-C Current modes or USB power delivery
- Configure VCONN

- Discover and configure optional Alternate and Accessory modes

In a Type-C application, the CC lines utilize combinations of pullups and pulldowns to detect Type-C device attachment, advertise the current capabilities of the source, and detect the type and orientation of the cable and the device. There are three possible pull-ups (Rp) which represent the three source current capabilities – Default, 1.5A, and 3A. There are two possible device pulldown resistors (Ra and Rd) to provide device and cable information to the host. This configuration allows for simultaneous advertisement and detection. The Type-C specification also allows for dynamic Rp changes without any resets.

CC Pass-Through Switches

The Type-C block includes the CC-to-HVCC Pass-Through switches that provide a protected communication path between the USB-PD controller and handheld device. Refer to *CC Passthrough Switch* section for more information.

VCONN Switch

While there are two HVCC pins that must be monitored on the host receptacle, there is only one CC wire running through the Type-C cable. This is how orientation can be determined. This leaves the second HVCC pin available for other uses. The Type-C specification allows the unused HVCC pin to operate as VCONN, a low power source intended to power active cables which may include authentication ICs or super-speed muxes.

MAX25430 includes complete support for VCONN power control and protection. When a power source within the acceptable operating voltage is connected to the VCONN pin, MAX25430 can connect the voltage source to the appropriate HVCC pin. Back-to-back VCONN FETs provide overvoltage and overcurrent protection to the VCONN source in addition to controlling the application of VCONN per the Type-C specification.

The advantage of MAX25430 is the ability to provide VCONN power from a low-power system supply to a wide-range of E-marked cables (i.e. using the same supply used to power the USB-PD Controller or MCU), essentially reducing the current budget needed for supplying VCONN and hence reducing the cost and solution size.

However, certain VCONN loads draw currents that exceed the Type-C specification of 1W maximum, shortly after VCONN is sourced. This causes unwanted inrush currents and droops on the system supply, ultimately causing a module reset.

To overcome this limitation while being able to provide Type-C required 1W VCONN, MAX25430 implements a dual-threshold overcurrent protection with specific debounce timers and a Fast UV comparator on the VCONN pin. The first overcurrent threshold (OCP Low) is programmable to either 250mA or 360mA (typ.) with a debounce of 400µs, which allows exceeding the 1W limit momentarily and during startup of the VCONN load circuitry. The second OCP threshold (OCP High) threshold is fixed and set to 700mA typ. and has a debounce of 5µs which protects the system supply from non-compliant VCONN loads and/or short circuits. A Short-to-Ground diagnostic circuitry is also implemented in order to detect if a short to ground condition is present before closing the VCONN switch and avoid collapsing the upstream supply.

Enabling VCONN

1. Program the VCONN OCP LOW setting by writing to the VCONN_OCP_SEL bit. Use 250mA for a 5V supply and 360mA for a 3.3V supply.
2. Program the VCONN UV setting by writing to the VCONN_IN_UV_THRESH bit. UV settings of 4.65V and 3.05V are recommended for 5V supply and 3.3V respectively.
3. Make sure the VCONN supply is enabled and above the VCONN UV programmed threshold. Read the VCONN_IN_UV status bit to verify. For 3.3V operation, the I^2C Master will need to clear this register since the default VCONN UV threshold is 4.65V.
4. Unmask Fault and Status bits as desired.
5. Select the HVCC channel where VCONN is needed by setting the Cable polarity bit PLUG_ORNT in the TCPC_CONTROL register.
6. Set the VCONN _EN bit to logic '1' to enable VCONN in the POWER_CONTROL register.
7. If VCONN has successfully started up, the MAX25430 will set the POWER_STATUS.VCONN_PRESENT bit to indicate VCONN is being sourced.
8. Monitor the OCP and UV fault flags.

9. To disable VCONN, set VCONN_EN to logic '0'.

VCONN Startup

Once the VCONN input is within its operating range and after VCONN is enabled on a HVCC Channel, the diagnostic current is enabled on the corresponding channel and the short-to-ground comparator is active and monitoring HVCC. If HVCC is above the short to ground threshold (typically 0.5V), the VCONN switch is soft-started and the diagnostic current turned off after 500µs. MAX25430 will indicate VCONN has soft-started successfully by setting POWER_STATUS.VCONN_PRESENT to logic '1'.

After VCONN is enabled on a HVCC channel, the IC monitors for additional faults related to VCONN operation.

VCONN Short-to-Ground Detection (STG Detection)

Every time VCONN starts or re-starts, MAX25430 checks for a short to ground condition. An actual hot short-to-ground condition will usually trip the VCONN UV fault or VCONN OCP High first. If a short-to-ground condition is maintained, the VCONN switch will not soft-start.

When a VCONN short-to-ground (STG) condition is detected, the 30mA diagnostic current (typ.) is enabled for 8ms (typ.). If HVCC rises above the short-to-ground threshold during the 8ms, the VCONN switch is soft-started normally. If the HVCC voltage does not go above the short-to-ground threshold by the end of the 8ms, the MAX25430 disables the diagnostic current source, then waits for 16ms before re-enabling it again and repeating the cycle until either the short-to-ground condition is removed or VCONN is disabled via I^2C. The short-to-ground retry time is fixed at 16ms and cannot be changed.

VCONN Reverse Overvoltage (Reverse OV)

On the first VCONN Reverse OV fault, the VCONN switch is immediately turned off, the diagnostic current is enabled on the corresponding channel and the short-to-ground comparator is active and monitoring HVCC.

MAX25430 reports the fault by setting the VNDR_ALRT.SHIELDING status bit on the first fault and as long as the fault condition is present. Once the fault clears, the VCONN switch will attempt to re-start autonomously after the time set in the RETRY_TMR register, as long as the VCONN _EN bit is still set to logic '1'.

VCONN Auto-Retry

Due to the fact that the VCONN supply is a shared supply, asynchronous system loads can happen while sourcing VCONN. For this reason, a VCONN Auto-Retry feature is implemented to minimize the software interaction when sourcing VCONN with a shared supply.

If a VCONN load tries to draw an excessive amount of current for more than the debounce time, the VCONN switch will automatically open to avoid drooping the upstream power supply, then will retry automatically. After three consecutive faults, the $\overline{\text{ALERT}}$ pin will assert indicating the I^2C Master to take action if needed.

The auto-retry feature is only active for the VCONN OCP and VCONN UV faults.

VCONN Overcurrent Protection (OCP Low/High)

On the first VCONN OCP fault and after the debounce time, the VCONN switch is immediately turned off, the diagnostic current is enabled on the corresponding channel and the short-to-ground comparator is active and monitoring HVCC.

If another OCP fault is detected, the fault process repeats again. After three consecutive faults, the VCONN_OCP_FAULT bit will be latched and the retry timer will start (default 16ms). Once the timer expires, the SHIELDING bit is set and the process repeats again with the fault counter restarting. Note that only the I^2C Master can clear the VCONN_OCP_FAULT bit.

Upon the VCONN_OCP_FAULT bit being set, the I^2C Master can take action to clear the bit, then disable VCONN. The I^2C Master can proceed without powering the non-compliant E-marked cable until a new cable is detected.

VCONN Undervoltage (UV)

On the first UV fault, the VCONN switch is immediately turned off, the diagnostic current is enabled on the corresponding channel and the short-to-ground comparator is active and monitoring HVCC. If the fault is no longer present the VCONN switch will be soft-started normally as described in the VCONN Startup section above.

However, if another UV fault is detected, the fault auto-retry is engaged and the fault process repeats again. After three

consecutive faults, the VCONN_IN_UV status bit is set and the retry timer will start (default 16ms). Once the timer expires, the process repeats again with the auto-retry fault counter restarting at 0.

Upon the VCONN_OCP_FAULT bit being set, the I^2C Master can take action to clear the bit, then disable VCONN. The I^2C Master can proceed without powering the non-compliant E-marked cable until a new cable is detected.

MAX25430 reports the fault by setting the VCONN_IN_UV status bit on the third fault and as long as the fault condition is present.

VCONN Automatic Discharge

To comply with the Type-C specification, the corresponding HVCC pin will be discharged for 1ms every time VCONN is disabled.

Legacy Devices

The Type-C specification ensures inter-operability with Type-A/Type-B devices by defining requirements for legacy adapters. As a DFP, relevant adapters will connect from the Type-C receptacle to either a Type-B plug or to a Type-A receptacle, which can then be used with any legacy Type-A cable. A compliant legacy adapter of this type must include an Rd termination inside the adapter. In this case, MAX25430 will detect a Type-C attachment whenever the adapter is connected, regardless of whether a portable device is connected. The portable device will see the DFP as a BC1.2 port (when configured as such). Refer to *BC1.2 Charge Detection* section for additional information.

Port Controller and Power Delivery (MAX25430B only)

Port Controller Interface (TCPCI) (MAX25430B only)

MAX25430B devices implement a Type-C Port Controller Interface (TCPCI) as defined in the USB Type-C Port Controller Interface Rev. 2.0 Ver. 1.1.

TCPCI is the interface between a USB Type-C Port Manager (TCPM) and a USB Type-C Port Controller (TCPC).

The goal of the TCPCI is to provide a defined interface between a TCPC and a TCPM to standardize and simplify USB Type-C Port Manager implementations.

The TCPC is a functional block which encapsulates V_{BUS} and VCONN power controls, USB Type-C CC logic, the USB PD BMC physical layer and protocol layer other than the message creation.

Contact Maxim Integrated for more information on how to program the TCPM to work with MAX25430B.

BMC Transmitter (MAX25430B only)

MAX25430B supports USB-PD message transmission and reception (Tx/Rx) through the BMC interface (Bi-Phase Mark Coding) on the HVCC channels. The BMC communication is used by the source and sink to exchange USB-PD messages. The BMC communication is single ended and occurs between two port partners (a source and a sink) after a Type-C attachment has been successfully made. The CC line that is going through the USB Cable is used by the two port partners to communicate using BMC.

The BMC transmitter driver overdrives the DC bias voltage on the HVCC pin that is set for device attachment while transmitting. The BMC transmitter driver will return to a Hi-Z state when not transmitting.

Note: MAX25430B meets the BMC eye diagram specifications as defined in the USB Power Delivery Specification. MAX25430B's BMC driver is referenced to the SHLD_SNS pin and therefore, BMC communication will not be affected by the IR drop caused by the external Shield Short-to-Battery FET, if used.

For more information on the BMC Protocol and Signaling, refer to the USB Power Delivery Specification Revision 3.0, Version 1.2.

Sink Tx Ok (MAX25430B Only)

When a PD contract is established, the sink shall ignore Rp current advertisement as USB-PD takes precedence over Type-C.

After a PD Contract, the TCPM can change the Rp advertisement of the TCPC to signal Sink Tx Ok. Rp advertisement is therefore used as a low level signaling feature. This feature was added in USB-PD Revision 3.0.

V_{BUS} 10-bit ADC (MAX25430B only)

The ADC is only available on the MAX25430B variant.

Topology: SAR

Resolution: 10-bit

Sampling: Continuous

Operation:

The ADC sampling is disabled at POR. To enable sampling, write logic '0' to bit D6 (VBUS_VOLT_MON_EN) of the POWER_CONTROL register 0x1C. To stop ADC sampling, write logic '1' to bit D6 of the POWER_CONTROL register 0x1C.

ADDR	REGISTER NAME	POR	D7	D6	D5	D4	D3	D2	D1	D0
0x1C	POWER_CONTROL	0x60		VBUS VOLTAGE MONITORING ENABLE	DISABLE VOLTAGE ALARMS	AUTO DISCHARGE ON DISCONNECT ENABLE		FORCE DISCHARGE ENABLE	VCONN POWER SUPPORTED	VCONN ENABLE

Note: Register Access Read/Write Read Only

Figure 5. POWER_CONTROL Register for ADC Control

The conversion result after each sample is stored in registers VBUS_VOLTAGE_L and VBUS_VOLTAGE_H and can be accessed via an I2C read transaction. MAX25430B maintains synchronization of the 10-bit result between the VBUS_VOLTAGE_L and VBUS_VOLTAGE_H registers by latching the VBUS_VOLTAGE_H value at the time of the VBUS_VOLTAGE_L is read. Therefore, an I2C Read Word transaction starting at VBUS_VOLTAGE_L address is recommended. Refer to the *I2C Interface* section for more information on the Read Word transaction.

ADDR	REGISTER NAME	POR	D7	D6	D5	D4	D3	D2	D1	D0
0x70	VBUS_VOLTAGE_L	0x00	ADC d7	ADC d6	ADC d5	ADC d4	ADC d3	ADC d2	ADC d1	ADC d0
0x71	VBUS_VOLTAGE_H	0x00							ADC d9	ADC d8

Note: Register Access Read/Write Read Only

Figure 6. VBUS_VOLTAGE Register for ADC Result

A 10-bit value for the ADC conversion result is obtained by combining bits D[1:0] of the VBUS_VOLTAGE_H register with bits D[7:0] of the VBUS_VOLTAGE_L register.

ADC_Result = (UInt16)((VBUS_VOLTAGE_H & 0x03) * 256) + VBUS_VOLTAGE_L)

To convert the ADC_Result to the measured VBUS Voltage, multiply it by 0.025.

V_{BUS} Alarms (MAX25430B only)

The 10-bit ADC conversion results are compared with the alarms thresholds set by the TCPM. Those Alarms are used to alert the TCPM during USB-PD V_{BUS} voltage transitions. To enable V_{BUS} alarms, write a logic '0' to VBUS_VOLT_MON_EN bit in the POWER_CONTROL register.

MAX25430B V_{BUS} alarms are compliant with the USB-PD specification. Contact Maxim Integrated for more information on how to program the V_{BUS} alarms.

vSafe0V Comparator

To comply with the Type-C specification, MAX25430 implements a vSafe0V comparator to indicate when V_{BUS} (sensed on the OUT pin) is below the vSafe0V threshold. Unlike the V_{BUS} discharge stop threshold, the vSafe0V threshold is fixed to 0.75V falling, with a 50mV hysteresis (typical).

The I^2C master can check the status of the vSafe0V comparator by reading the VSAFE0V bit in the EXTENDED_STATUS[7:0] register located in the TCPCI compliant register section.

A logic '1' of this bit signifies V_{BUS} is at or below vSafe0V threshold. A logic '0' signifies VBUS is above the vSafe0V threshold. This status bit is read-only and non-latched.

Whenever the VSAFE0V bit changes and the MSK_VSAFE0V is set to '1' (unmasked), the EXTENDED_STATUS alert bit will be set.

The vSafe0V status is valid only when the V_{BUS} Detection Enabled bit (VBUS_DET_EN) located in the POWER_STATUS[7:0] register becomes a '1'. The VBUS_DET_EN bit is read-only and indicates the MAX25430 is

monitoring for V_{BUS} Present and vSafe0V thresholds.

V_{BUS} Present Comparator

In order to enable the V_{BUS} Present comparator, the TCPM must send the EnableVbusDetect command (0x33) to the COMMAND register.

Whenever the VBUS_DET_EN read-only bit becomes logic '1' , MAX25430 the V_{BUS} Present comparator is active and monitoring the OUT pin. If the voltage sensed on OUT goes above 4V (typ.), the MAX25430 will set the VBUS_PRESENT bit in the POWER_STATUS register to Alert the TCPM that V_{BUS} is present on the Type-C connector.

To disable the comparator, the TCPM must send the DisableVbusDetect command (0x22). Note that the EnableVbusDetect and DisableVbusDetect commands will also enable and disable the vSafe0V comparator, respectively.

V_{BUS} Discharge

When V_{BUS} is disabled, the residual charge stored in the buck-boost output capacitance must be removed to comply with the Type-C specification. The MAX25430 has an internal discharge path that when activated, discharges V_{BUS} to a set threshold. Figure 7 shows the discharge internal circuitry used for both Force- and Auto-Discharge Features. The V_{BUS} Force and Auto-Discharge functions are compliant with the USB-PD and TCPCI specifications.

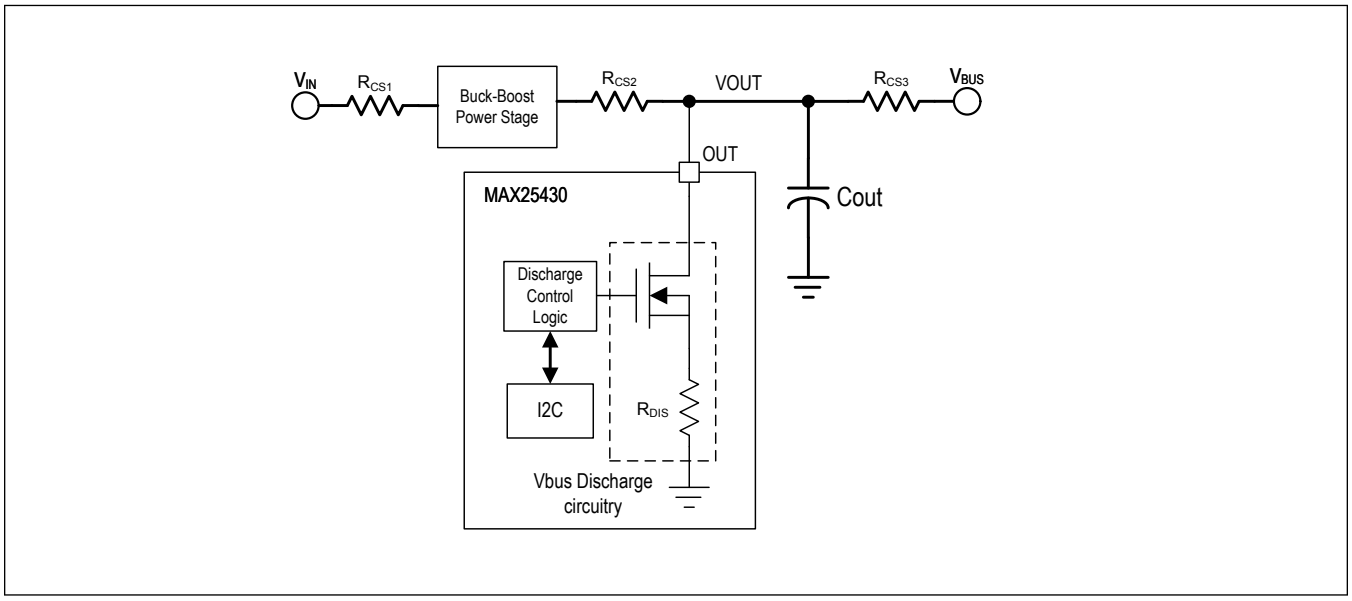


Figure 7. V_{BUS} Discharge Block Diagram

V_{BUS} Force Discharge

Whenever the FORC_DISCH_EN bit D2 in the POWER_CONTROL register is set from logic '0' to '1', the 125Ω discharge R_{DIS} is switched on and the discharge monitoring starts. MAX25430 will automatically disable the Force Discharge circuit (without clearing FORC_DISCH_EN bit) once the voltage on V_{OUT} has reached the value indicated by the 10-bit VBUS_STOP_DISCH_THRESHOLD register.

If V_{OUT} does not reach the programmed Stop threshold (default 0.8V) within 650ms, the discharge stops to avoid possible overheating and flags the FORCE_DISCH_FAIL bit. Which, if un-masked, sets the FAULT_STAT bit in the ALERT_H register. If FAULT_STAT is un-masked, $\overline{ALERT}$ will be asserted. A typical use case of the V_{BUS} force discharge is after a device disconnect when using a PD-Controller with MAX25430A or a hard reset when using either MAX25430A or MAX25430B.

Refer to the TCPCI specification for more information on the V_{BUS} Force Discharge function.

V_{BUS} Auto Discharge

The V_{BUS} Auto-Discharge Function (MAX25430B devices only) is enabled by setting the AUTO_DISCH_DISC_EN bit D4 to 1 after a device attach. When the MAX25430 detects a device disconnect, the 125Ω discharge resistor R_{DIS} will be switched on automatically and the discharge monitoring will start. If V_{OUT} does not reach the programmed Stop threshold (default 0.8V) within 650ms, the discharge stops to avoid possible overheating and flags the AUTO_DISCH_FAIL bit. Which, if un-masked, sets the FAULT_STAT bit in the ALERT_H register. If FAULT_STAT is un-masked, $\overline{ALERT}$ will be asserted.

Refer to the TCPCI specification for more information on the V_{BUS} Auto-Discharge function.

ADDR	REGISTER NAME	POR	D7	D6	D5	D4	D3	D2	D1	D0
0x1C	POWER_CONTROL	0x60		VBUS VOLTAGE MONITORING ENABLE	DISABLE VOLTAGE ALARMS	AUTO DISCHARGE ON DISCONNECT ENABLE		FORCE DISCHARGE ENABLE	VCONN POWER SUPPORTED	VCONN ENABLE

Note: Register Access Read/Write Read Only

Figure 8. POWER_CONTROL Register for V_{BUS} Discharge

Both MAX25430A and MAX25430B devices incorporate a threshold comparator to determine when the voltage on VBUS has reached vSafe0V. The state of the vSafe0V comparator is continuously indicated by Bit D0 of the EXTENDED_STATUS register (0x20). Bit D0 is set to logic '1' when VSAFE0V is true and cleared to logic '0' when the voltage of V_{BUS} is above the vSafe0V threshold. Refer to *vSafe0V Comparator* for more information.

The blue curve below shows a V_{BUS} discharge reaching the programmed stop threshold before the 650ms timeout and is therefore successful, no error flag is set. The red curve shows a discharge that did not reach the stop threshold on time and therefore is flagged as fail on either the FORCE_DISCH_FAIL or AUTO_DISCH_FAIL depending on the type of discharge used.

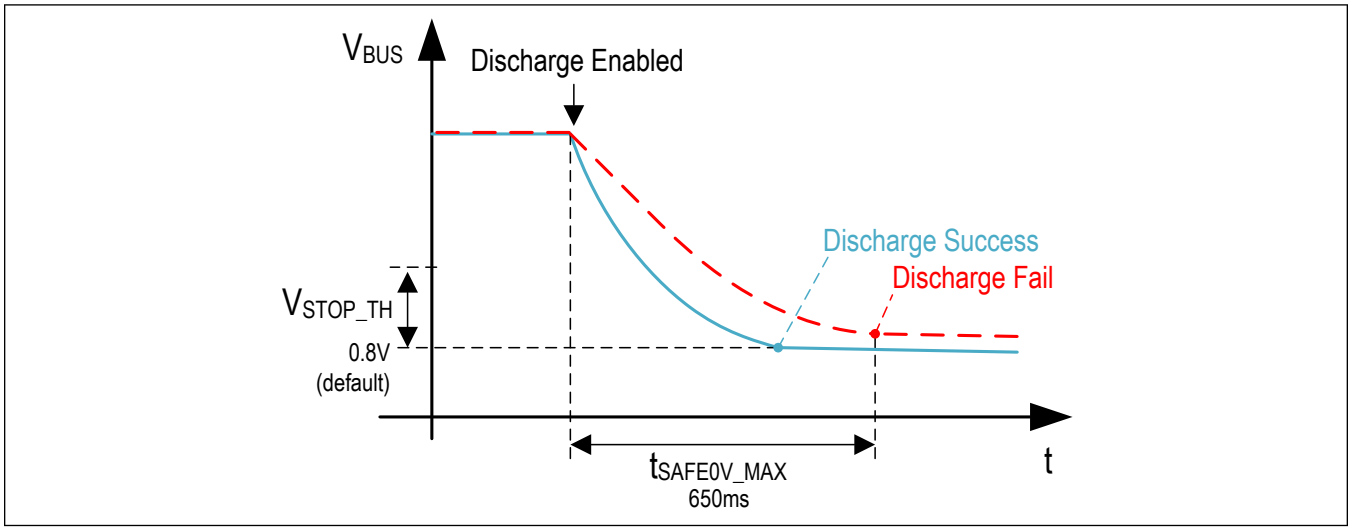


Figure 9. VBUS Discharge Timing Diagram

Note: t_{SAFE0V} maximum value is defined in the USB-PD specification.

Table 5. Discharge Times for Different Output Voltages

V_{BUS}	Typical Discharge Time to vSafe0V (Capacitance: 3x68µF + 5x10µF = 254µF)
vSafe5V	50ms
9.0V	75ms
15.0V	120ms
20.0V	150ms

BC1.2 Charge Detection

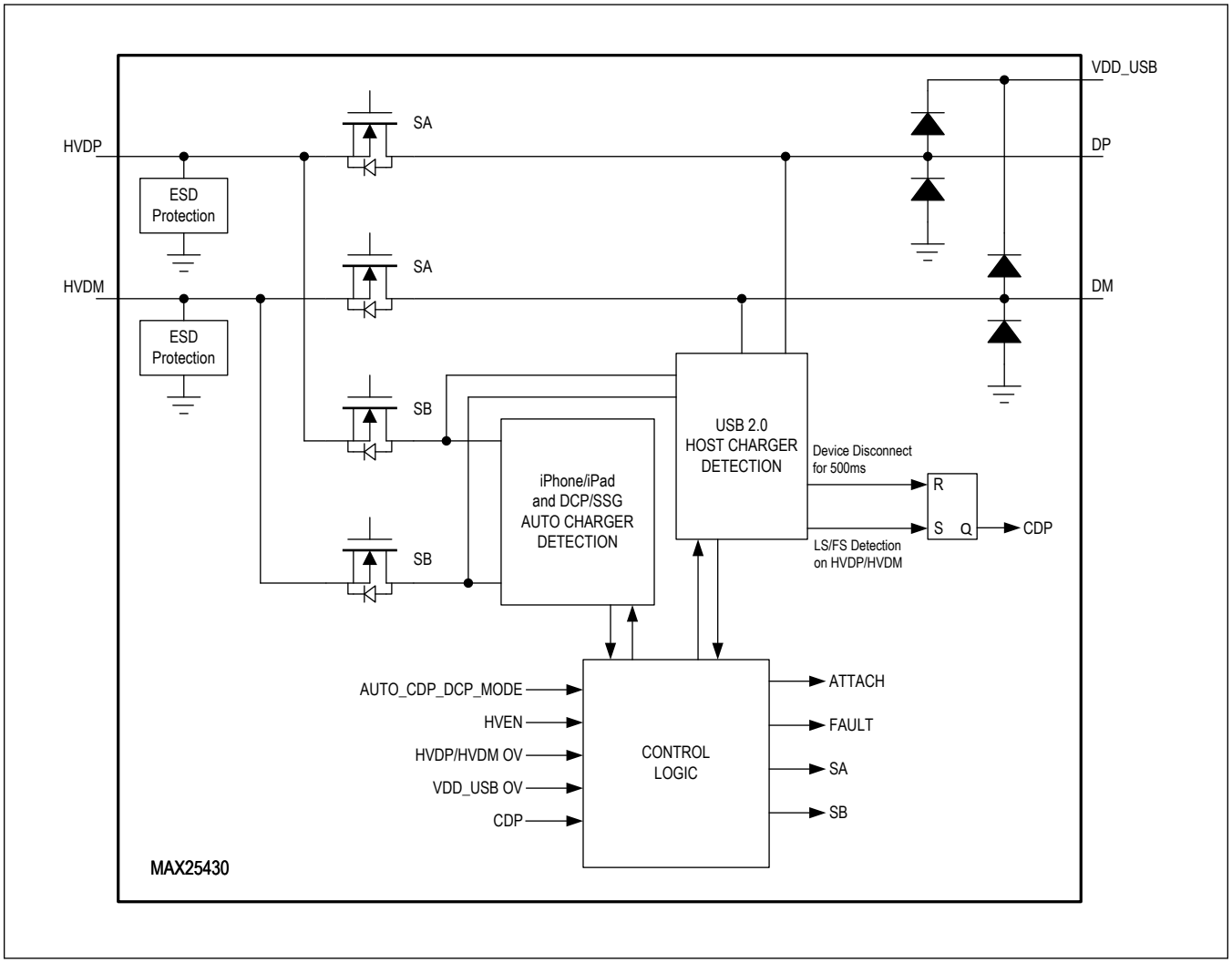


Figure 10. Data Switch and Charge-Detection Block Diagram

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USB Host Adapter Emulator

The MAX25430 integrates the latest USB-IF Battery Charging Specification Revision 1.2 CDP and DCP circuitry, as well as 1.0A and 2.4A resistor bias options for Apple-compliant devices. Legacy Samsung Galaxy 1.2V divider and China YD/T1591-2009 compatibility is also provided by the Auto-DCP modes.

Table 6. Data Switch Mode Truth Table

DEVICE INPUTS		SA	SB	Data Switch Mode
HVEN	AUTO_CDP_DCP_MODE[1:0]			
0	X	0	0	Off
1	00	1	0	Hi-Speed Pass-Through (SDP)
	01	On if CDP = 0	On if CDP=1	Auto-CDP
	10	0	1	Auto-DCP/Apple 2.4A
	11	0	1	Auto-DCP/Apple 1.0A

USB On-The-Go and Dual-Role Applications

The MAX25430 is fully compatible with USB On-The-Go (OTG) and dual-role applications. A negotiated role swap (HNP or Apple CarPlay) requires no software interaction with the IC. When there is no negotiation before the SoC enters peripheral mode, the MAX25430 must be in Hi-Speed pass-through (SDP mode) before and during the role swap. The MAX25430 devices default to SDP mode on startup. This configuration allows a role swap immediately on startup without microcontroller interaction. The I^2C Master can change the Data Switch mode anytime by writing to the AUTO_CDP_DCP_MODE[1:0] register.

Protection

In an Automotive USB Type-C with Power Delivery application, several threats to the module can be encountered.

In case of a Short-to-V_{BUS} event on CC connector pins, the integrated VCONN switch must protect the upstream supply against overvoltage. The CC switches must also clamp and dissipate the energy to protect the upstream PD Controller from pin damage.

In case of a short-to-ground condition, the shared 3.3V or 5.0V supply used for VCONN shall not brownout or be damaged.

For applications with a USB 2.0 data path, the upstream USB host D+/D+ pins have a typical 6V absolute maximum rating and therefore will not survive to any Short-to-Battery, Short-to-VBUS or Automotive ESD event.

Short-to-Battery (18V) can happen during module assembly, repair, end-user (dropping the end of cable in the cigarette lighter).

Short-to-V_{BUS} (20V Power Delivery, up to 24V) is very common for USB Type-C ports and can happen upon device removal due to mechanical twisting, debris or insertion of a non-PD compliant source into the port.

MAX25430 will protect the module against all these threats.

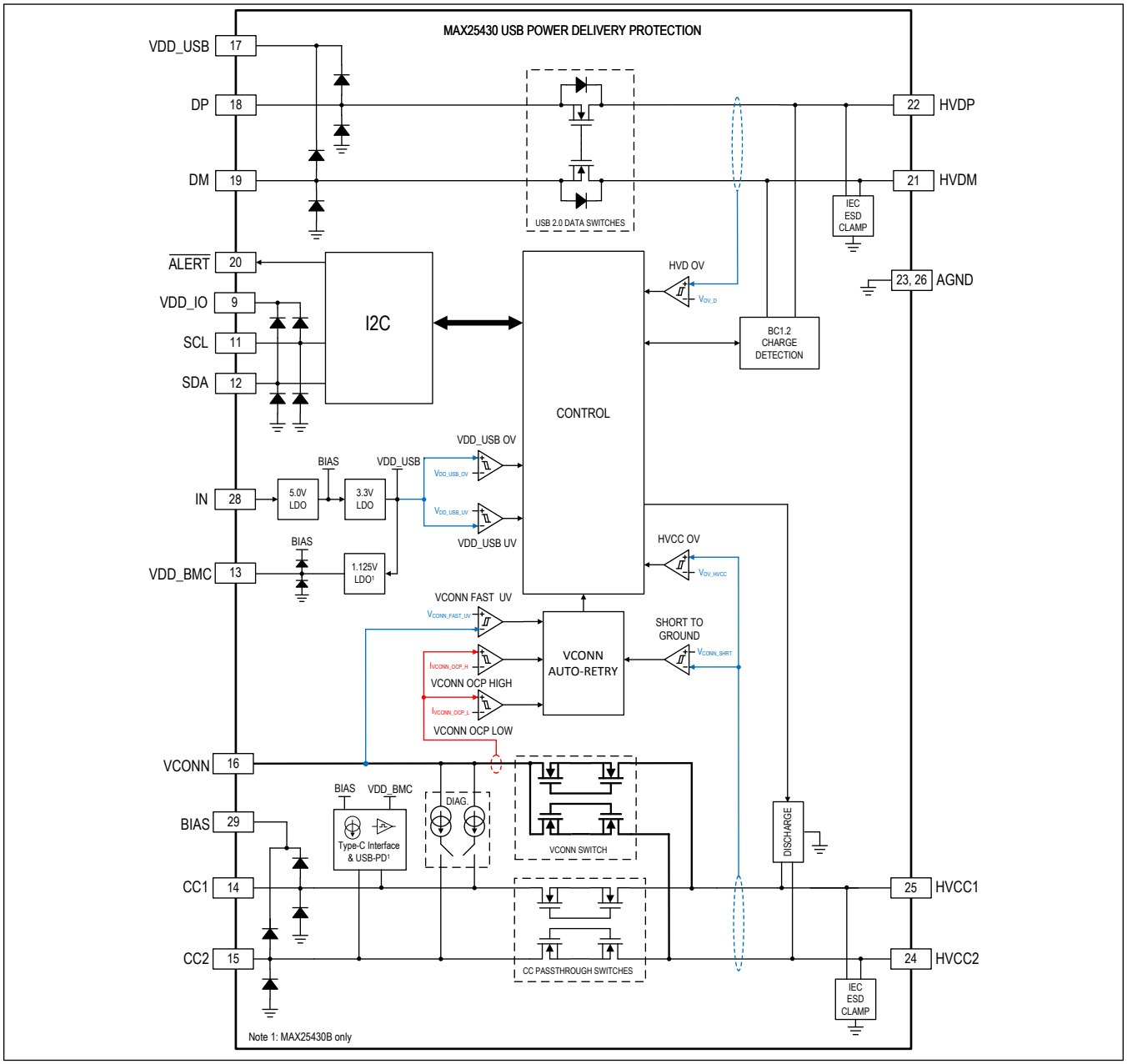


Figure 11. USB Power Delivery Protection Block Diagram

USB 2.0 Data Switches

The D+ and D- pins are the protected side of the USB data switches and connect directly to the low-voltage upstream USB PHY or captive cable. No external circuitry is used on either data pin.

The HVD+ and HVD- pins should be routed to the downstream Type-C connector or captive cable. No external circuitry is required on either pin. HVD+ pin and HVD- pin are tolerant to automotive high-ESD and up to 24V voltage transients.

CC Passthrough Switches

The CC1 and CC2 pins are the protected side of the CC switches and either connect directly to the upstream USB-PD controller for MAX25430A devices or internally to the TCPC block for MAX25430B devices. No external circuitry is needed on either CC pin. The HVCC1 and HVCC2 pins connect directly to the downstream USB Type-C port connector or captive cable. No external circuitry is needed on either HVCC pin. HVCC1 and HVCC2 are tolerant to automotive high-ESD and up to 24V voltage transients.

Shield Short-to-Battery

MAX25430 devices with a G-Suffix integrate USB Shield Short-to-Battery protection. USB Shield Short-to-Battery can occur when a customer's portable device cable is connected to the downstream receptacle, and the far end of this cable falls into the cigarette lighter receptacle and contacts the 12V center terminal. This condition results in a damaging amount of current flow, with insufficient response time by the cigarette lighter fuse. The MAX25430 is designed to sense this Shield Short-to-Battery condition with the SENSE pin and control an external NFET with the GDRV output pin.

Patent "Systems and methods to cable shield fault detection and protection" Appl. No.: 63/017,630.

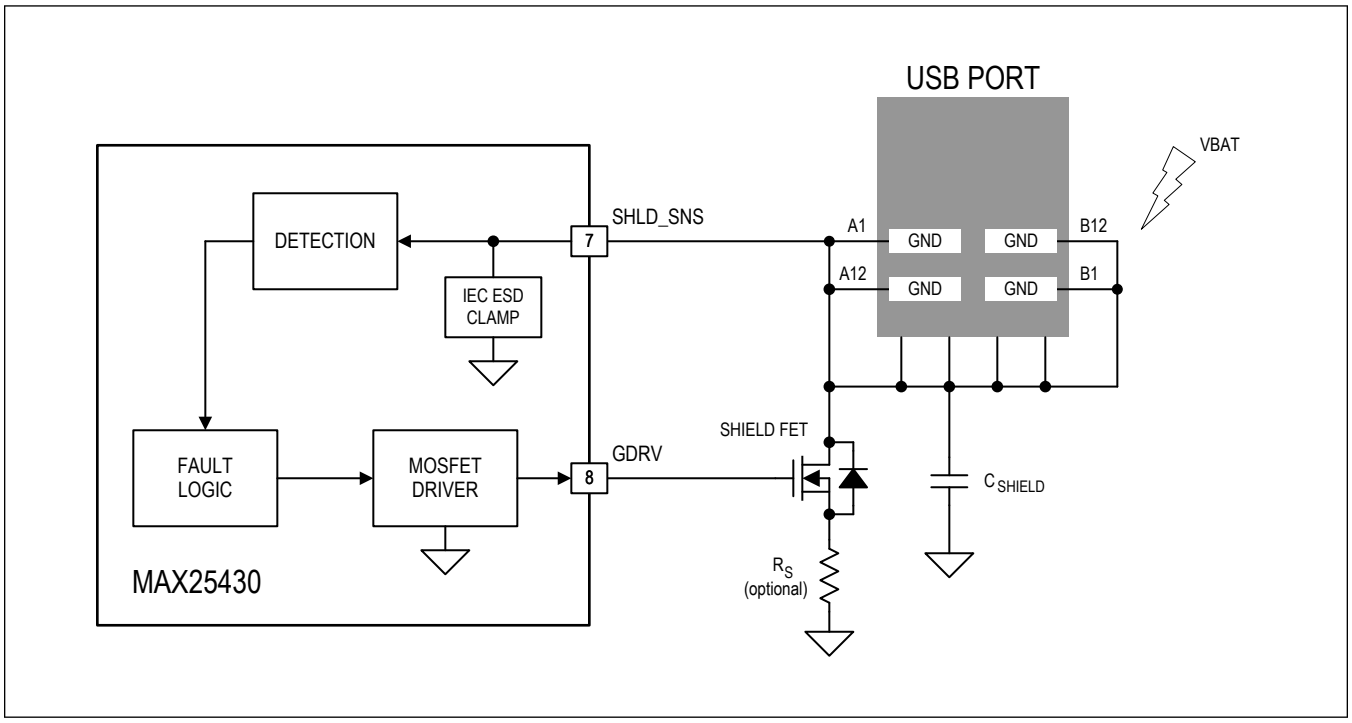


Figure 12. Shield Short-to-Battery Functional Diagram

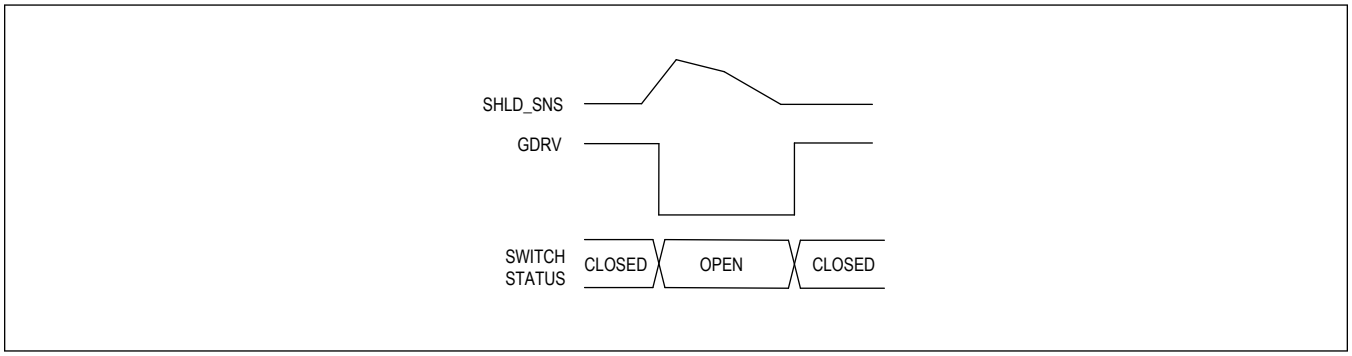


Figure 13. Simplified Shield Short-To-Battery Event Diagram

The diagram above illustrates the protection circuit for the shield short-to-battery protection with a legacy USB cable attachment in place. When the cable shield contacts with V_{BAT}, a large surge current flows through the FET's $R_{DS(ON)}$ and R_S to ground. This surge current develops a voltage across it and is sensed through the SHLD_SNS pin. When the sense voltage satisfies one of the criteria for a fault condition, shield short-to-battery fault handling is engaged to protect the system. Once the fault condition is removed, the GDRV pin will go high to turn the FET on.

Principle of Operation

The MAX25430 continuously monitors for a Type-C device attach and will control GDRV based on attach/detach events and timer circuitry.

When a type-C connection is not present, MAX25430 protects against shield short-to-battery by leaving GDRV = 0. In this state, the USB Shield and all other USB Type-C grounds are floating, however a weak pulldown from SHLD_SNS is always active. This pulldown enables an Rd attachment to be detected, while not providing a low-resistance path to ground.

When a valid Type-C attach is present, GDRV remains high for as long as the connection is present. A valid type-C connection may be to a native USB Type-C device, a Type-C to legacy adapter/cable, or an Apple lightning device. MAX25430 protects against damaging surge currents by using four unique detection methods:

1. Threshold Detection: Surge current exceeds a fixed threshold for several microseconds.
2. Slope Detection: Surge current exceeds a fixed, upper slew-rate limit.
3. Inrush Detection: Surge current is detected that is from an external source, not from V_{BUS}.
4. Panic Threshold Detection: Surge current exceeds a fixed threshold (higher than threshold-detection level) with no debounce time.

Any of these protection mechanisms can trigger the shield short-to-battery fault handling described in the *Fault Table (Maxim Auto-Shield)*. Threshold and panic detection are always available, but slope and inrush protection require the use of the 20mΩ cable compensation sense resistor (R_{CS3}). Threshold, slope and inrush protection are automatically disabled when any of the following are true:

- An attached USB device draws more than 500mA
- An attached USB device initiates a BC1.2 handshake
- USB-PD communication is present

When a shield short-to-battery event is detected, GDRV is driven low until 1ms after the fault condition has cleared.

GDRV Truth Table

Table 7 below shows the state of the GDRV pin with respect to the level detected on HVCC1 and HVCC2. This table applies to all MAX25430 devices. For MAX25430A, it is assumed a PD Controller is present upstream.

Table 7. GDRV Truth Table

V_{IN} > UVLO	HVEN	HVCC1 State	HVCC2 State	GDRV State
No	-	-	-	Low
Yes	Low	-	-	
	High	Open	Open	
		Open	Ra	
		Ra	Open	
		Open	Rd	High*
		Rd	Open	
		Rd	Ra	
		Ra	Rd	
		Ra	Ra	
		Rd	Rd	

*If no Shield Short-To-Battery fault has been detected

Fault Detection and Diagnostics

The MAX25430 features advanced fault reporting and management mechanisms to protect the system from various events that are not within normal operating conditions. The MAX25430 is designed to eliminate false fault reporting by using internal deglitch and fault blanking timers. This ensures the SHIELDING bit is not incorrectly asserted during normal operation, such as starting into heavy capacitive loads. To report the fault to the $\overline{ALERT}$ pin, set the corresponding mask bit. The table below describes the different faults, reporting mechanisms, debounce values, action and recovery type. Each action and recovery type is defined in the *Fault Type* table.

Table 8. Fault Table (Maxim Auto-Shield)

NAME	EVENT	REPORTING	DEBOUNCE PRIOR TO ACTION	FAULT ACTION	FAULT RECOVERY
Thermal Shutdown	IC temperature exceeds the thermal shutdown threshold	SHIELDING VNDR_ALRT[a]	100µs	A	A
HVCC Overvoltage	HVCC1 or HVCC2 exceeds the V_{OV_HVCC} threshold	SHIELDING VNDR_ALRT[a]	Immediate	A	A
HVD Overvoltage	HVDP or HVDM exceeds the V_{OV_D} threshold	SHIELDING VNDR_ALRT[a]	Immediate	A	A
V_{DD_USB} Overvoltage	V_{DD_USB} exceeds the $V_{DD\_USB\_OV}$ threshold	SHIELDING VNDR_ALRT[a]	2.5µs	A	A
V_{DD_USB} Undervoltage	V_{DD_USB} falls below the $V_{DD\_USB\_UV}$ threshold	VDD_USB_UV VNDR_ALRT[b]	Immediate	C	C
V_{BUS} I_{LIM}	V_{BUS} current exceeds the threshold set in the VOUT_ILIM[1:0] register	SHIELDING VNDR_ALRT[a]	16ms	A	A
V_{BUS} OCP	V_{BUS} current exceeds the I_{OUT_OCP} threshold	SHIELDING VNDR_ALRT[a] VBUS_OCP_FAULT[g]	Immediate	A	A
V_{BUS} Overvoltage	V_{BUS} exceeds the threshold set in the VBUS_OV_THRESH[2:0] register, except during V_{BUS} transitions	SHIELDING VNDR_ALRT[a] VBUS_OVP_FAULT[h]	Immediate	A	A
V_{BUS} Undervoltage	V_{BUS} falls below the threshold set in the VBUS_UV_THRESH[2:0] register, except during V_{BUS} transitions	VBUS_UV VNDR_ALRT[c]	16ms	C	C
V_{BUS} Short-to-Ground	V_{BUS} falls below 2V (typical)	SHIELDING VNDR_ALRT[a]	Immediate	A	A
V_{BUS} Pre-Bias Overvoltage	COMMAND.SourceVbusDefaultVoltage is received but V_{BUS} is above the vSafe0V threshold	I2C_ERR	10µs	C	C
VCONN OCP Low	VCONN current exceeds the $I_{VCONN\_OCP\_L}$ threshold	SHIELDING[d] VNDR_ALRT[a,d] VCONN_OCP_FAULT[d,i]	400µs	B	B
VCONN OCP High	VCONN current exceeds the $I_{VCONN\_OCP\_H}$ threshold	SHIELDING[d] VNDR_ALRT[a,d] VCONN_OCP_FAULT[d,i]	5µs	B	B
VCONN Undervoltage	VCONN pin falls below the $V_{CONN\_FAST\_UV}$ threshold	VCONN_IN_UV VNDR_ALRT[e]	2.5µs	B	B
VCONN Reverse OV	HVCC to VCONN pin voltage exceeds the reverse overvoltage threshold (100mV typ.)	SHIELDING VNDR_ALRT[a]	2.5µs	D	B

Table 8. Fault Table (Maxim Auto-Shield) (continued)

VCONN Short-to-Ground	HVCC is below the short-to-ground threshold (0.5V (typ.) for more than 8ms) prior VCONN switch soft-start	VCONN_PRESENT stays at 0	30µs	Disable VCONN and take Action D except Retry Time is 16ms	B
IN Undervoltage	V_{IN} (main IC supply) falls below the threshold set in the IN_UV_THRESH[3:0] register	SHIELDING VNDR_ALRT[a]	100µs	A	A
Shield Short-to-Battery	A Shield Short-to-Battery fault has been detected. (G-Suffix devices only) Refer to the *Shield Short-to-Battery* section.	SHIELDING VNDR_ALRT[a]	Immediate	A and Turn off SHIELD FET	A
Buck-Boost Input Overcurrent	The differential voltage across the input current sense resistor exceeds the V_{OC1} threshold (16.6A typ. for R_{CS1} = 3mΩ)	IN_OC VNDR_ALRT[f]	16ms	C	C
Buck-Boost Output Runaway	V_{BUS} is below 50% of the target regulation voltage or the differential voltage across the output current sense resistor is above the V_{OC2} threshold (output runaway)	SHIELDING VNDR_ALRT[a]	Immediate	A	A

Note a: if SHIELDING_MASK = '1'

Note b: if VDD_USB_UV_MASK = '1'

Note c: if VBUS_UV_MASK = '1'

Note d: On the third consecutive fault

Note e: if VCONN_IN_UV_MASK = '1'

Note f: if IN_OC_MASK = '1'

Note g: if VBUS_OCP_DET_EN = '0'

Note h: if VBUS_OVP_DET_EN = '0'

Note i: if VCONN_OCP_DET_EN = '0'

Table 9. Fault Types

Fault Type	Action[1]	Recovery
A	-Assert ALERT[2] -Disable DC-DC, Discharge to vSafe0V -Open Data Switches -Open CC Passthrough Switches -Discharge HVCC1 and HVCC2 pins -Open VCONN Switch for RETRY_TMR setting -Reset BC1.2 State Machine	-DC-DC can be re-enabled by the I2C Master via the COMMAND register -Close Data Switches -Close CC Passthrough Switches -Close VCONN Switch based on TCPC POWER_CONTROL[0] and TCPC_CONTROL[0] settings
B	First and second fault: -Open CC Passthrough Switches -Open VCONN Switch -Start VCONN Short to Ground Detect Sequence -Start VCONN Retry Sequence Third Fault: Same as first two faults except: -Open VCONN Switch for the time set in RETRY_TMR bit field -Assert ALERT[2]	-Close CC Passthrough switches -Close VCONN Switch depending on TCPC POWER_CONTROL[0] and TCPC_CONTROL[0] settings
C	-Assert ALERT[2]	None
D	-Open CC Passthrough Switches -Open VCONN Switch for the time set in RETRY_TMR bit field -Assert ALERT[2]	-Close CC Passthrough switches -Close VCONN Switch depending on TCPC POWER_CONTROL[0] and TCPC_CONTROL[0] settings

Note 1: Faults do not reset the TCPC State Machine nor disable Rp current sources.

Note 2: if MSK_VNDR_ALRT=1

I²C, Control, and Diagnostics

I2C Diagnostics and Events Handling

Contact Maxim Integrated for more information on how to program I²C Diagnostics and Events Handling.

Mask Registers and Nested Alerts

- The registers in this section provide the masks that may be set for the ALERT registers. A masked register will still indicate in the ALERT register but will not set the $\overline{\text{ALERT}}$ pin low. POWER_STATUS_MASK, FAULT_STATUS_MASK, EXTENDED_STATUS_MASK and ALERT_EXTENDED_MASK registers are nested alerts.
- A POWER_STATUS change has to be unmasked in both the POWER_STATUS_MASK and the ALERT_MASK_L.MSK_PWR_STAT to assert the $\overline{\text{ALERT}}$ pin.
- A FAULT_STATUS change has to be unmasked in both the FAULT_STATUS_MASK and the ALERT_MASK_H.MSK_FAULT_STAT to assert the $\overline{\text{ALERT}}$ pin.
- An EXTENDED_STATUS change has to be unmasked in both the EXTENDED_STATUS_MASK and the ALERT_MASK_H.MSK_EXTND_STAT to assert the $\overline{\text{ALERT}}$ pin.
- An ALERT_EXTENDED change has to be unmasked in both the ALERT_EXTENDED_MASK and the ALERT_MASK_H.MSK_ALRT_EXTND to assert the $\overline{\text{ALERT}}$ pin.

Figure 14 and Figure 15 describe the Alerts, corresponding masks and links between them. A Level 1 Alert will require to have one mask bit unmasked to assert the $\overline{\text{ALERT}}$ pin. A Level 2 Alert will require to have two mask bits unmasked to assert the $\overline{\text{ALERT}}$ pin.

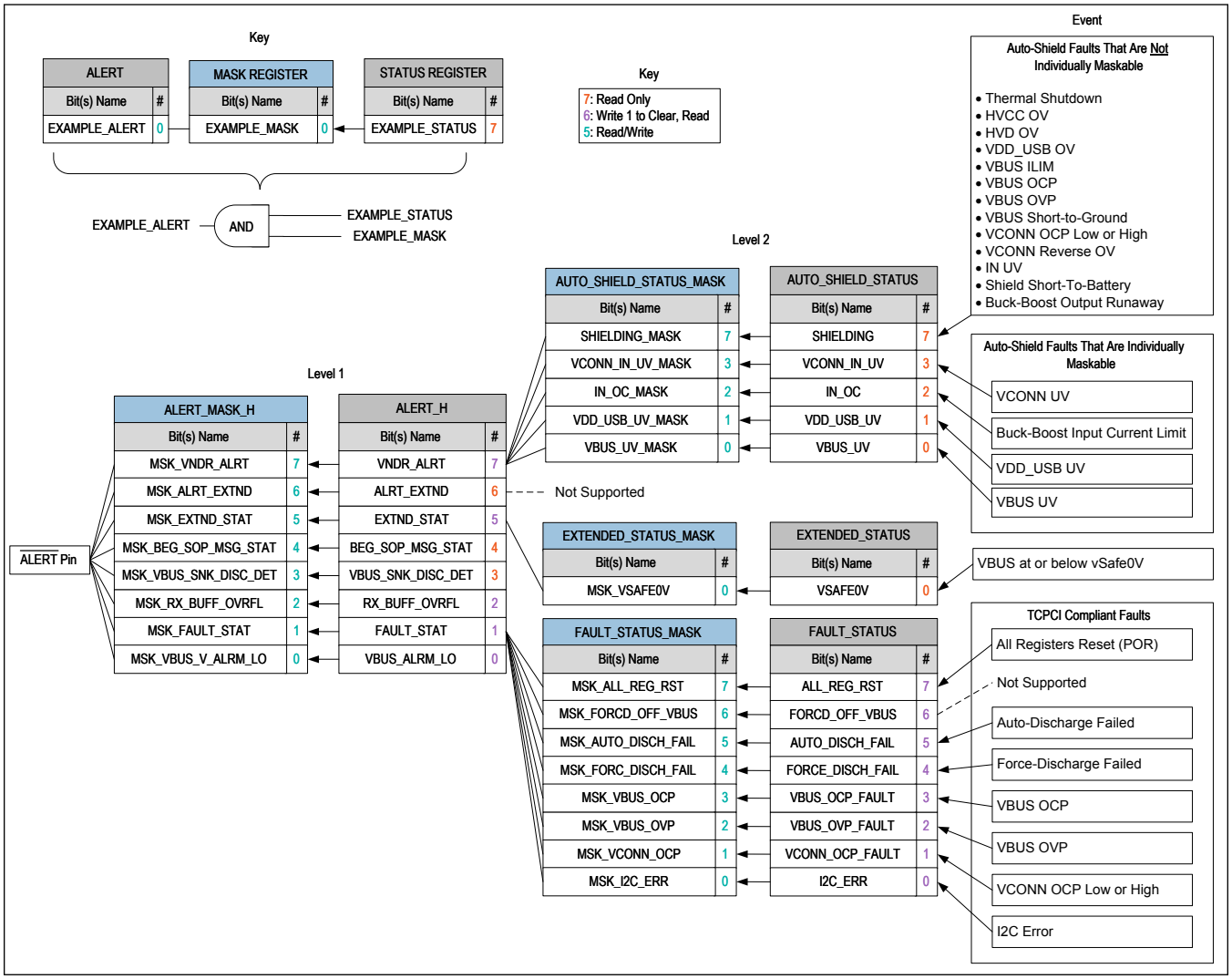


Figure 14. Nested Alerts Diagram - ALERT_H

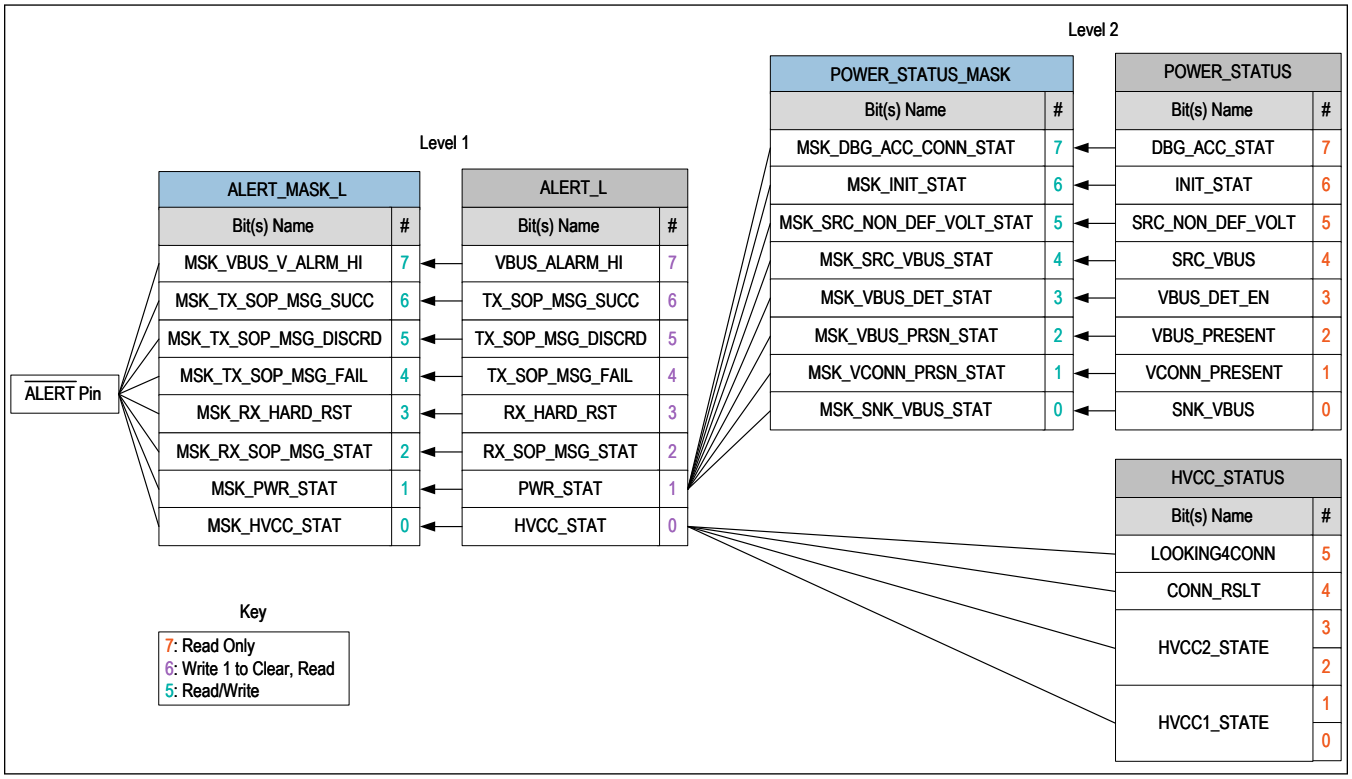


Figure 15. Nested Alerts Diagram - ALERT_L

I²C Interface

The MAX25430 is an I2C Slave device and requires an I²C Master to communicate with its internal registers. It can accept SCL clock rates up to 1MHz, and its 7-bit device address can be set to 0x50, 0x51, 0x52, or 0x53 via the ADDR input pin.

The Master, a PD Controller, SoC or microcontroller, generates SCL and always initiates data transfer on the bus. The MAX25430's SCL line operates as an input only. A pull-up resistor greater than 500 Ω is required on SCL if the Master has an open-drain SCL output.

The MAX25430's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA line.

These resistors should be placed close to the MAX25430 SCL and SDA pins to minimize the effects of I²C bus capacitance. Maxim recommends using a value of 4.7kΩ for both resistors in most cases. Series resistors in line with SCL and SDA are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

The MAX25430 I²C Slave logic is powered by the voltage applied to VDD_IO (1.8V to 5.0V), allowing the MAX25430's logic levels to be matched with those of the I²C Master. Note that I²C communications is possible even if the buck-boost is not switching (ie. when V_{BUS} is off).

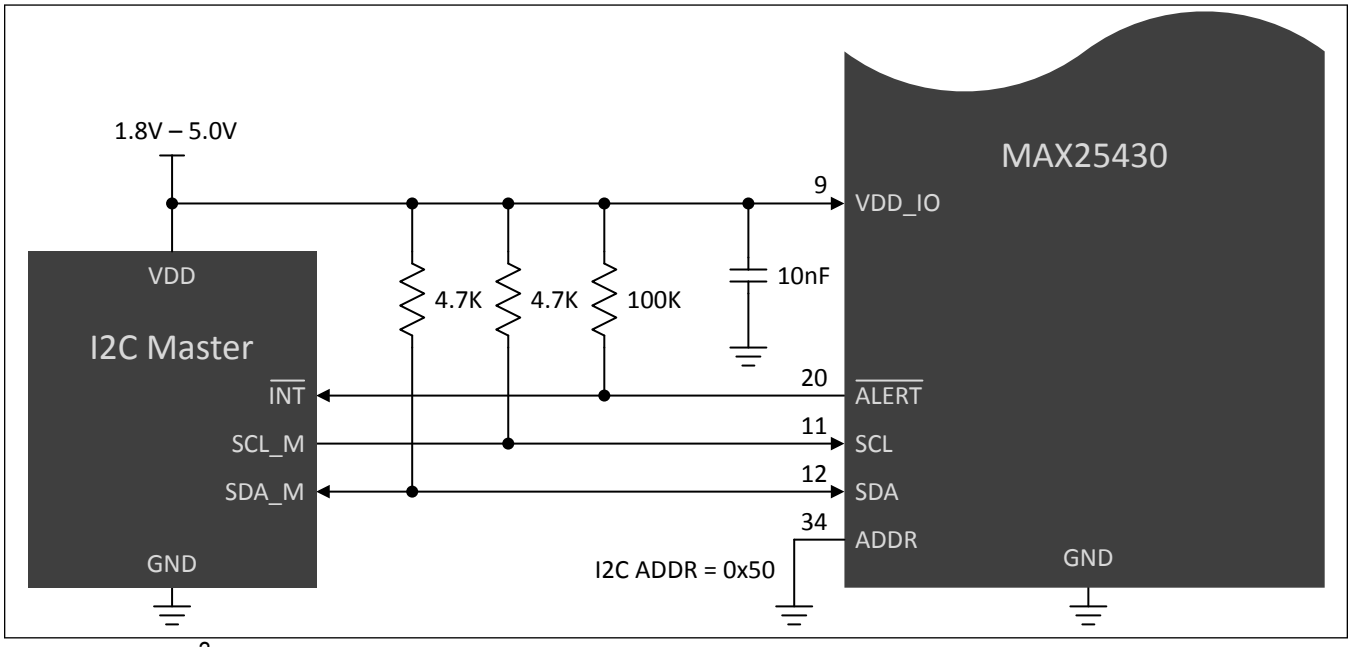


Figure 16. Typical I²C Application Diagram

Interrupt Output ($\overline{\text{ALERT}}$ Pin)

$\overline{\text{ALERT}}$ is an active-low, open-drain output that asserts to notify the I²C Master of an interrupt. A pull-up to V_{DD_IO} is required for proper operation. Note that certain bits require their corresponding mask bit to be set for the $\overline{\text{ALERT}}$ pin to be asserted, as the mask bits act as AND gates.

I²C Slave Addressing (ADDR Pin)

Once the device is enabled, the I²C slave address is set and latched based on the ADDR pin. The address is defined as the 7 most significant bits (MSBs) followed by the R/W bit. Set the R/W bit to 1 to configure the devices to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the devices after the START Condition.

Table 10. I²C Slave Addresses

ADDR Pin	A6	A5	A4	A3	A2	A1	A0	7-BIT ADDRESS	WRITE	READ
GND	1	0	1	0	0	0	0	0x50	0xA0	0xA1
8870Ω to GND	1	0	1	0	0	0	1	0x51	0xA2	0xA3
15800Ω to GND	1	0	1	0	0	1	0	0x52	0xA4	0xA5
BIAS	1	0	1	0	0	1	1	0x53	0xA6	0xA7

I²C Protocol

Data is transferred MSB first with each data bit present on SDA sampled on every SCL clock pulse while the SDA line is stable. A byte of data on SDA contains 8 bits, MSB first, that can represent but is not limited to a register address or data written to the device. Additionally, SDA should never change while the SCL is high. There are two exceptions to this rule, the START Condition, and STOP Condition.

START Condition

Every I²C transaction between a Master device and Slave device begins with the Master sending a START Condition. The I²C master generates a START Condition by first detecting when the I²C bus is idle, and then asserting the SDA signal low while allowing SCL to remain pulled high.

STOP Condition

An I2C STOP Condition is created whenever an I2C Master produces a rising edge on SDA while SCL remains high. This terminates any transaction with a slave device and frees up the I2C bus. SDA and SCL idle high when the I2C bus is not busy. The bus remains active if a REPEATED START (RS) condition is generated instead of a STOP condition.

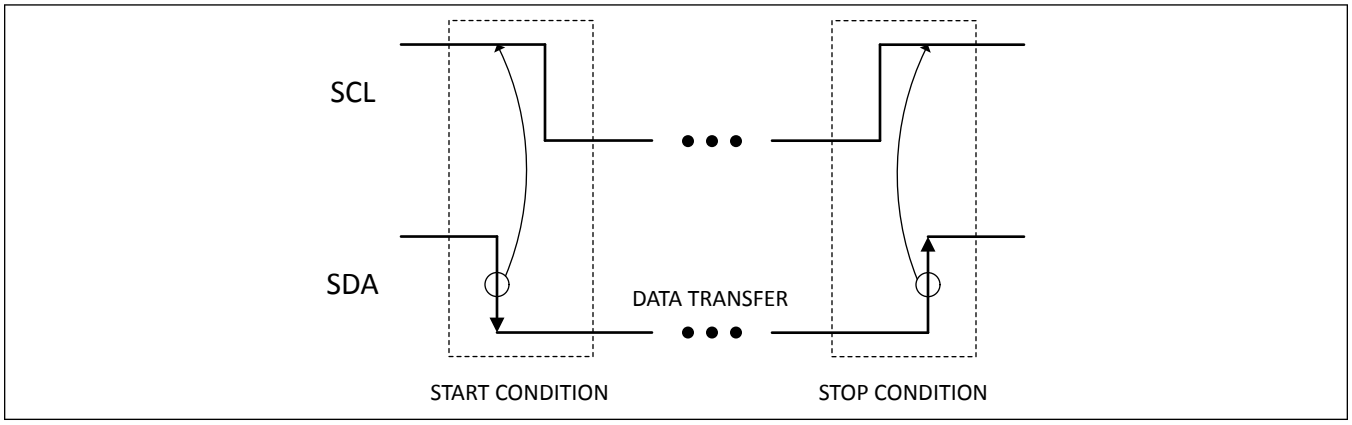


Figure 17. START and STOP Conditions

REPEATED START Condition

An I2C REPEATED START Condition is created when an I2C Master produces a second START during a transaction with a Slave device. Repeated Starts are needed to signal the Slave device that the Master desires a change in data direction during a transaction. The REPEATED START is sent after the Acknowledge bit (ACK).

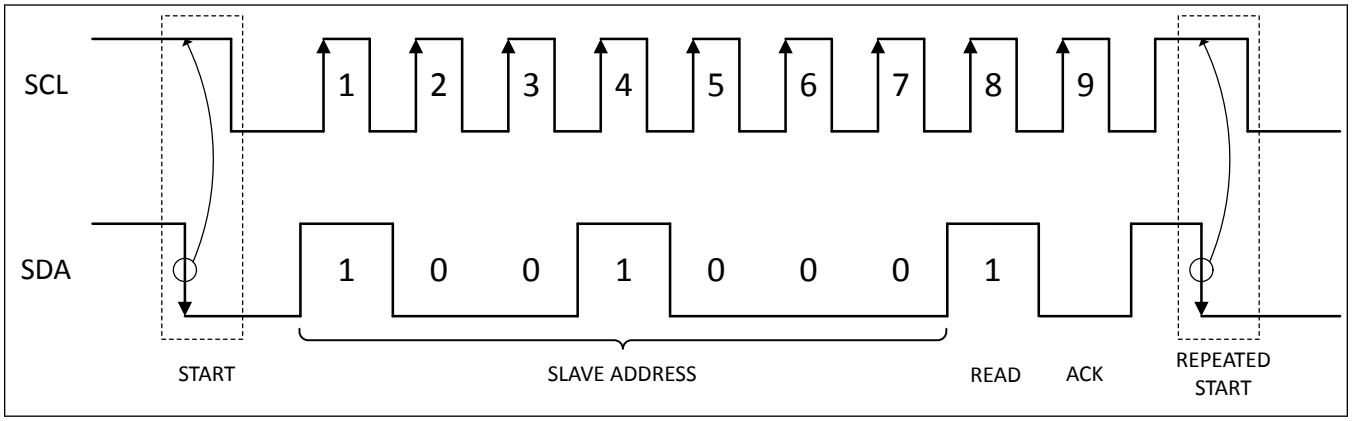


Figure 18. REPEATED START Condition

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data. The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the I2C Master can reattempt communication.

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. The I2C specification

allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX25430 does not use any form of clock stretching to hold down the clock line.

General Call Adresss

The MAX25430 does not implement the I2C specifications “general call address”. If the MAX25430 sees the general call address (0b0000_0000) it will not issue an acknowledge.

I2C Transactions

The MAX25430 can respond to several types of I2C transactions, as described below.

Read Byte

The Master Read Byte transaction begins with the master sending a START Condition. This is followed by a 7-bit address and R/W bit = 0, indicating a master write operation. If this address matches the MAX25430 device address, the device will acknowledge (ACK) by holding the SDA line low for one SCL clock. The master then sends the byte address, which serves as a pointer to the MAX25430 device register where data will be read. The MAX25430 again acknowledges the byte sent. Then, the master sends a REPEATED START condition, alerting the MAX25430 device that the next byte will again be an address. The master device clocks in the MAX25430 address, this time appended with a logic ‘1’. This signals the MAX25430 that the master wants to read the data from the register address previously sent. The MAX25430 again ACKs the byte sent. On the rising of the next SCL clock, the slave begins sending the desired data byte to the master. The master will then signal the MAX25430 that the previous byte was the final byte needed by not acknowledging (NACK), followed by a STOP Condition, indicating the end of the Read Byte transaction.

When the I2C Master desires to read data from two or more MAX25430 registers that are not contiguously located, sequential Read Byte transactions must be used. For instance, two bytes of data can be read from the MAX25430, one at register address 0x1E and the other at register address 0x20, however the I2C bus is released (STOP Condition) between read operations. The MAX25430 will acknowledge its address and data bytes sent by the Master. It expects the Master to NACK the last data byte prior to sending a STOP Condition.

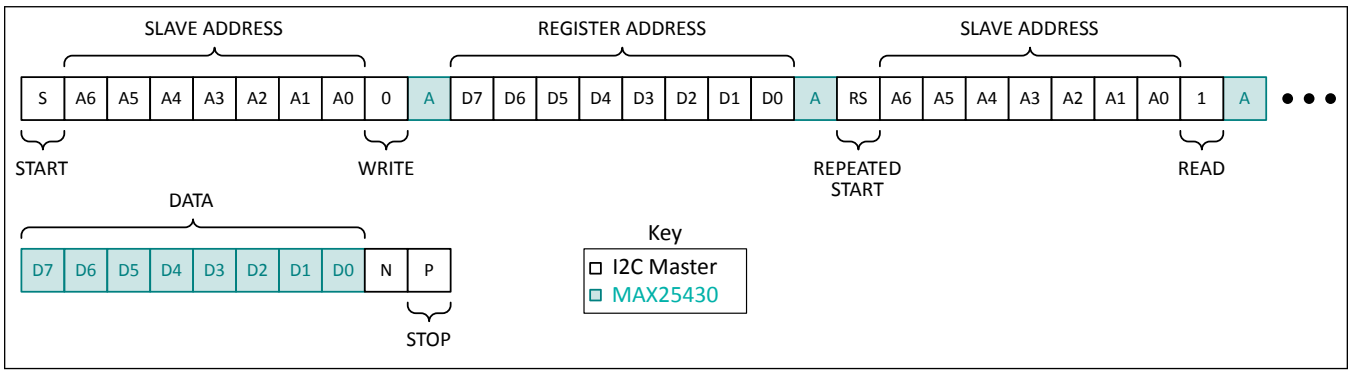


Figure 19. Read Byte

Write Byte

The Master Write Byte transaction begins with the master sending a START Condition. This is followed by a 7-bit address and R/W bit = 0, indicating a master write operation. If this address matches the MAX25430 device address, it will acknowledge (ACK) by holding the SDA line low for one SCL clock. The master then sends the register address, which serves as a pointer to the MAX25430 register where data will be written. The MAX25430 again acknowledges the byte sent. Then the master sends the data byte and waits for the MAX25430 to ACK the data byte. Finally, the I2C Master terminates the transaction by sending a STOP Condition.

When it is desired to write data to two or more non-contiguous MAX25430 registers, sequential Master Write transactions should be used. The MAX25430 will acknowledge its address and data bytes sent by the Master. A Master STOP Condition terminates each write.

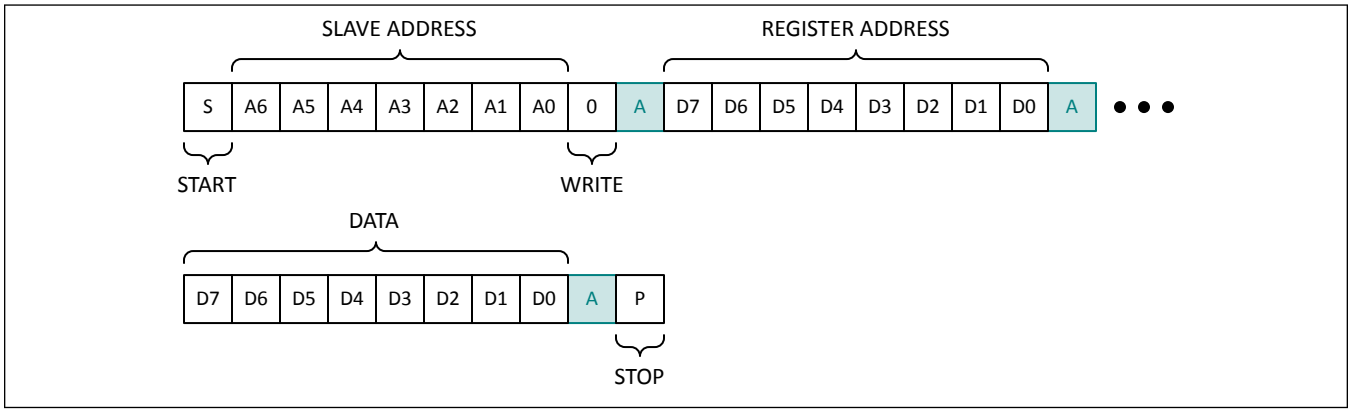


Figure 20. Write Byte

Read Word

The Master Read Word transaction follows the same sequence as the Master Read Byte except that two data bytes are received from the MAX25430, a low-address data byte (DATA n) followed by a high-address data byte (DATA n+1). This is accomplished by ACKing the first data byte received from the Slave device, and then NACKing the second data byte, followed by sending a STOP Condition. Note that the MAX25430 automatically increments the register pointer to the next address. Reading ALERT_L and ALERT_H registers in a single operation is an example of using the Read Word transaction.

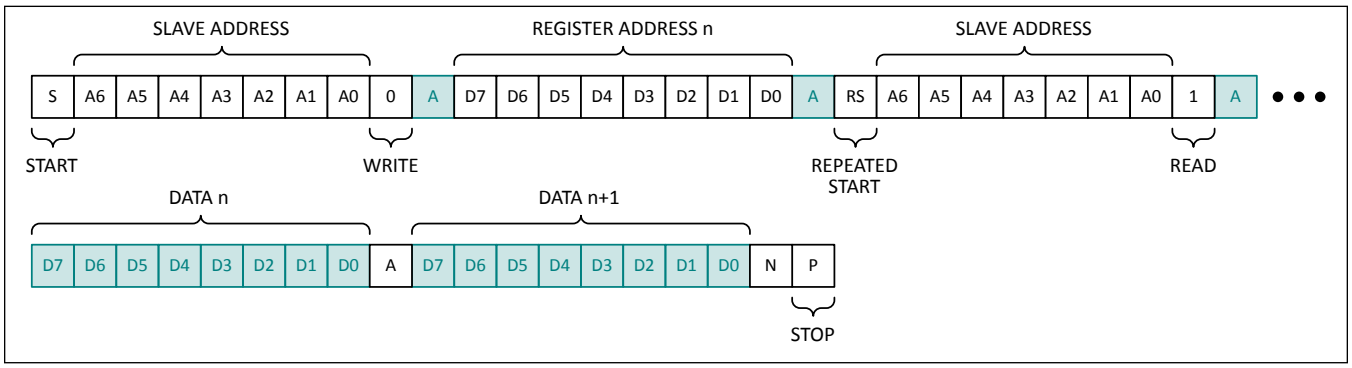


Figure 21. Read Word

Write Word

The Master Write Word transaction is similar to a Master Write Byte except that data is written to two sequential MAX25430 registers in one operation. The transaction begins exactly as a Master Write Byte transaction; namely a START Condition, the Slave Address followed by a write bit then Register Address. However, two data bytes are then sent, a low-address data byte (DATA n) followed by a high-address data byte (DATA n+1). The MAX25430 will acknowledge each byte received, and automatically increment the register address pointer between the low and high data bytes. Finally, the Master sends a STOP Condition to complete the transaction. Note that the low and high data bytes follow the same bit order as the previous bytes (Slave and Register address) which is MSB first (D7 to D0). Once the data is received, the I^2C Master will need to flip the bit order and concatenate to obtain a 16-bit word with LSB first.

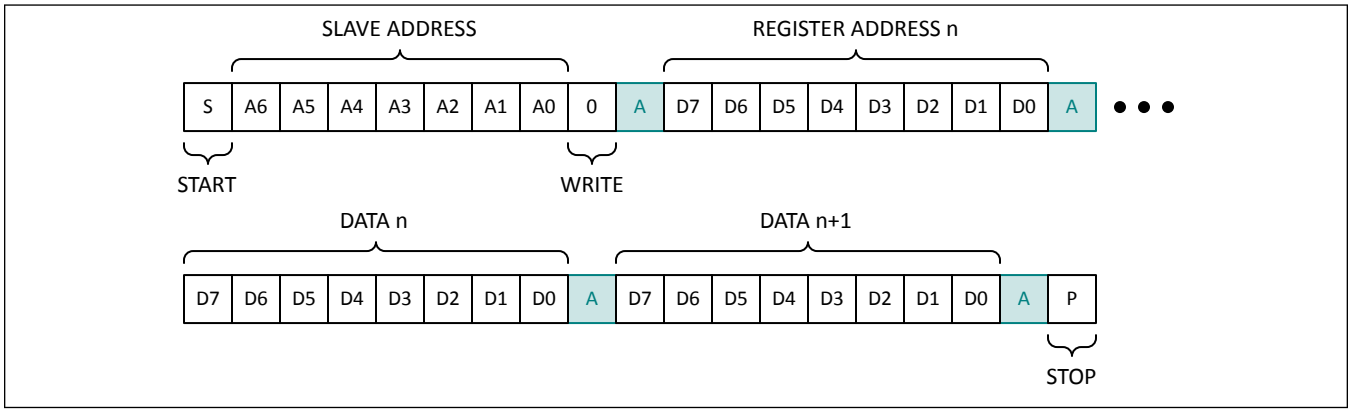


Figure 22. Write Word

Read Block

The Master Read Block transaction is a powerful function, enabling the I2C Master to read from 1 to 255 bytes of data from contiguous MAX25430 registers in one operation. Note that I2C Read operations from the MAX25430B's TCPC Receive Buffer require this type of I2C transaction for proper operation.

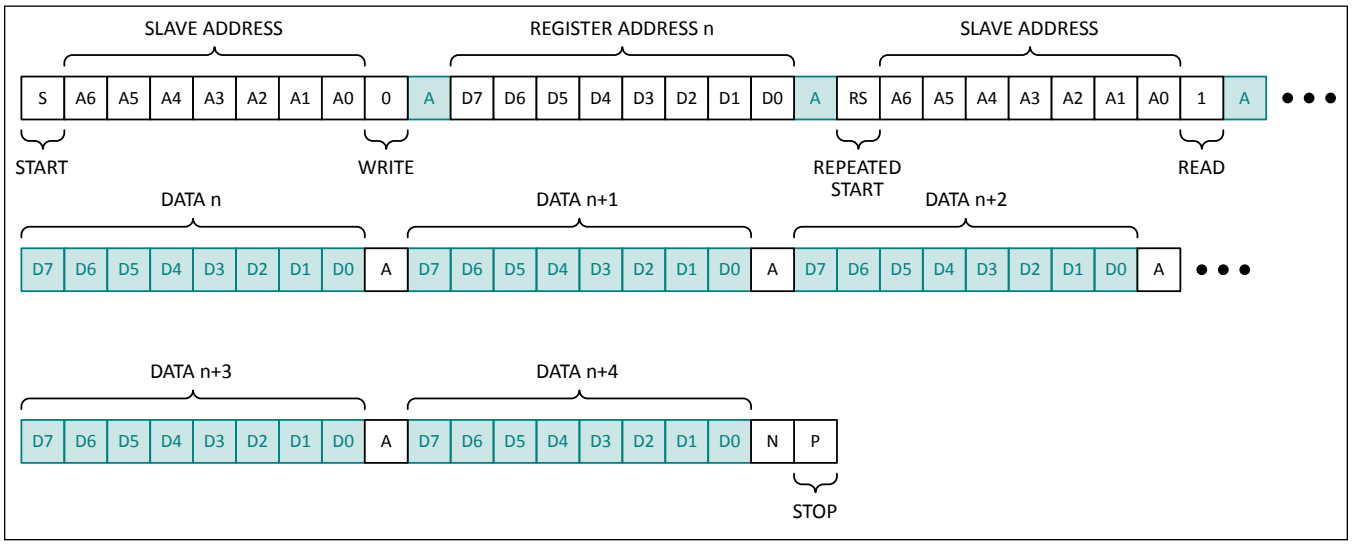


Figure 23. Read Block

The Master Read Block transaction begins as any I2C Read operation, first the Master sends a START Condition, followed by the MAX25430's 7-bit device address plus the R/W bit = 0. The MAX25430 will ACK its address, then the Master sends the register address for the beginning of the contiguous block where data is to be read from. The MAX25430 will again ACK the received data. Next the Master sends a REPEATED START Condition, informing the MAX25430 that the next byte sent will be an address. The I2C Master then sends the MAX25430's 7-bit device address plus the R/W bit = 1, configuring the MAX25430 I2C for Slave read operation. The MAX25430 again acknowledges its address and prepares to deliver data from its registers.

The Master can now read up to 255 bytes of data from the MAX25430 by continuing to clock the SCL signal. The MAX25430 will output data on SDA, one byte for each 8 SCL clocks, and expect that the Master ACK the data sent on the 9th SCL clock. The MAX25430 will automatically increment the register address pointer between successive bytes.

When the desired number of bytes from the MAX25430 has been sent, the Master must send a NACK followed by a STOP Condition to terminate the transaction.

Write Block

The MAX25430 also supports I2C block data writes for up to 255 contiguous registers. The MAX25430B's Transmit Buffer requires this type of I2C transaction for proper operation.

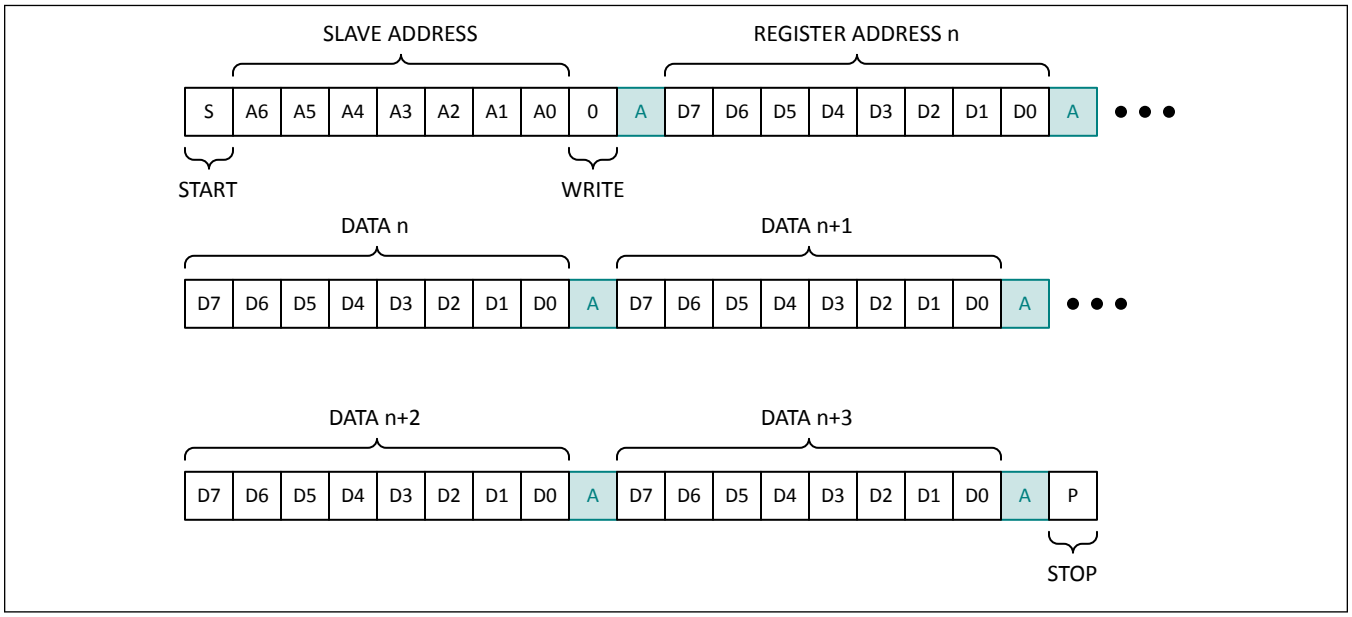


Figure 24. Write Block

The Master Write Block transaction begins by sending a START Condition, followed by the MAX25430's 7-bit device address plus the R/W bit = 0. The MAX25430 will ACK its address, then the Master sends the register address for the beginning of the contiguous block where data will be written. The MAX25430 will again ACK the received data.

The Master can now write up to 255 bytes of data to the MAX25430 by continuing to clock the SCL signal. The MAX25430 will store data from SDA, one byte for each 8 SCL clocks, and will ACK the data sent on the 9th SCL clock. The MAX25430 will automatically increment the register address pointer between successive bytes. When the desired number of bytes from the MAX25430 has been sent, the Master sends a STOP Condition to terminate the transaction.

Watchdog

MAX25430 implements a programmable watchdog timer to give the design engineer the ability to monitor the I^2C interface for lack of communication from the I^2C Master. The watchdog provides a fail-safe mechanism in case the TCPM software stack or PD Controller firmware hangs in a state where, for instance, a voltage is sourced on V_{BUS} when the sink is no longer attached.

The watchdog timer functionality is enabled by setting TCPC_CONTROL.EN_WD_TMR to logic '1'. The watchdog timer starts when any of the unmasked interrupts in the Alert register are set or when the $\overline{ALERT}$ pin is asserted. The watchdog timer is cleared on any I^2C access by the I^2C Master (either Read or Write). If the $\overline{ALERT}$ pin is still asserted after this I2C access, the watchdog timer will reinitialize and start monitoring again until all of the Alerts are cleared or until the $\overline{ALERT}$ pin is de-asserted.

When the Watchdog is enabled and the I^2C Master is unable to clear the interrupt within the programmed time set in WATCHDOG_SETUP.WD_TIMEOUT[1:0], it will cause the watchdog timer to expire. When the Watchdog timer expires, MAX25430 will immediately disconnect the CC terminations by setting ROLE_CONTROL bits 3...0 to 1111b, discharge V_{BUS} to vSafe0V, and then set FAULT_STATUS.I2C_ERR bit. The MAX25430 will remove the V_{BUS} discharge circuit when V_{BUS} is below vSafe0V and it will not re-apply the discharge circuit if V_{BUS} rises above vSafe0V. Stop discharge in this case is an edge-triggered event.

Any further changes on V_{BUS} need to be initiated by the I^2C master when its communication link with the MAX25430 is restored.

Register Map

Summary Table

The following register map summary table displays all the registers for the MAX25430 product family. Bit descriptions that show "MAX25430B only" are only applicable to MAX25430B devices. If using MAX25430A devices, "MAX25430B only" bits should be ignored and left to their reset values. Row "Reset" in Register Details contains MAX25430B reset values while row "Reset A" contains MAX25430A reset values.

Registers starting from address 0x00 to address 0x79 are compliant to the Type-C Port Controller Interface Specification Revision 2.0, Version 1.1. Refer to the specification for additional information on how to use those registers.

Register starting from address 0x80 to address 0x8B are vendor-defined by Maxim Integrated.

For more information on the MAX25430 register set and for instructions on how to program the interface, contact Maxim Integrated.

ADDRESS	NAME	MSB							LSB
USB Type-C and USB-PD Registers									
0x00	VENDOR_ID_L[7:0]	VENDOR_ID[7:0]							
0x01	VENDOR_ID_H[7:0]	VENDOR_ID[15:8]							
0x02	PRODUCT_ID_L[7:0]	PRODUCT_ID[7:0]							
0x03	PRODUCT_ID_H[7:0]	PRODUCT_ID[15:8]							
0x04	DEVICE_ID_L[7:0]	DEVICE_ID[7:0]							
0x05	DEVICE_ID_H[7:0]	DEVICE_ID[15:8]							
0x06	USBTYPEC_REV_L[7:0]	TYPEC_REV[7:0]							
0x08	USBPD_REV_VER_L[7:0]	PD_VER[7:0]							
0x09	USBPD_REV_VER_H[7:0]	PD_REV[7:0]							
0x0A	PD_INTERFACE_REV_L[7:0]	IBS_VER[7:0]							
0x0B	PD_INTERFACE_REV_H[7:0]	IBS_REV[7:0]							
0x10	ALERT_L[7:0]	VBUS_ALARM_HI	TX_SOP_MSG_SUCC	TX_SOP_MSG_DISCRD	TX_SOP_MSG_FAIL	RX_HARD_RST	RX_SOP_MSG_STAT	PWR_STAT	HVCC_STAT
0x11	ALERT_H[7:0]	VNDR_ALRT	ALRT_EXTND	EXTND_STAT	BEG_SOP_MSG_STAT	VBUS_SNK_DISC_DET	RX_BUFF_OVRFL	FAULT_STAT	VBUS_ALARM_LO
0x12	ALERT_MASK_L[7:0]	MSK_VBUS_V_ALRM_HI	MSK_TX_SOP_MSG_SUCC	MSK_TX_SOP_MSG_DISCRD	MSK_TX_SOP_MSG_FAIL	MSK_RX_HARD_RST	MSK_RX_SOP_MSG_STAT	MSK_PWR_STAT	MSK_HVCC_STAT
0x13	ALERT_MASK_H[7:0]	MSK_VNDR_ALRT	MSK_ALRT_EXTND	MSK_EXTND_STAT	MSK_BEG_SOP_MSG_STAT	MSK_VBUS_SNK_DISC_DET	MSK_RX_BUFF_OVRFL	MSK_FAULT_STAT	MSK_VBUS_V_ALRM_LO

ADDRESS	NAME	MSB							LSB
0x14	POWER_STATUS_MASK[7:0]	MSK_DEBG_ACC_CONN_STAT	MSK_INIT_STAT	MSK_SRC_NON_DEF_VOLT_STAT	MSK_SRC_VBUS_STAT	MSK_VBUS_DET_STAT	MSK_VBUS_PRSN_STAT	MSK_VCONN_PRSN_STAT	MSK_SNK_VBUS_STAT
0x15	FAULT_STATUS_MASK[7:0]	MSK_All_REG_RST	MSK_FORCD_OFF_VBUS	MSK_AUTO_DISCH_FAIL	MSK_FORC_DISCH_FAIL	MSK_VBUS_OCP	MSK_VBUS_OVP	MSK_VCONN_OCP	MSK_I2C_ERR
0x16	EXTENDED_STATUS_MASK[7:0]	–	–	–	–	–	–	–	MSK_VSAFE0V
0x17	ALERT_EXTENDED_MASK[7:0]	–	–	–	–	–	MSK_TMR_EXP	MSK_SRC_FST_RSWP	MSK_SNK_FST_RSWP
0x18	CONFIG_STANDARD_OUTPUT[7:0]	HI_IMPD_OUT	DBG_ACC_CONN	AUDIO_ACC_CONN	ACTV_CABL_CONN	MUX_CNTRL[1:0]		CONN_PRSNT	CONN_ORIENT
0x19	TCPC_CONTROL[7:0]	EN_SMB_PEC	EN_LK4CONN_ALRT	EN_WD_TMR	DBG_ACC_CNTRL	I2C_CLK_STRCH[1:0]		BIST_TM	PLUG_ORNT
0x1A	ROLE_CONTROL[7:0]	–	DRP	RP_VAL[1:0]		HVCC2[1:0]		HVCC1[1:0]	
0x1B	FAULT_CONTROL[7:0]	–	–	–	FRC_OFF_VBUS_DIS	VBUS_DISCH_FLT_DET_TMR_EN	VBUS_OCP_DET_EN	VBUS_OVP_DET_EN	VCONN_OCP_DET_EN
0x1C	POWER_CONTROL[7:0]	FAST_RSWP_EN	VBUS_VOLT_MON_EN	VOLT_ALRMS_EN	AUTO_DISCH_DISC_EN	BLED_DISCH_EN	FORC_DISCH_EN	VCONN_PWR_SUPP	EN_VCONN
0x1D	HVCC_STATUS[7:0]	–	–	LOOKING4CONN	CONN_RSLT	HVCC2_STATE[1:0]		HVCC1_STATE[1:0]	
0x1E	POWER_STATUS[7:0]	DBG_ACC_STAT	INIT_STAT	SRC_NON_DEF_VOLT	SRC_VBUS	VBUS_DET_EN	VBUS_PRESENT	VCONN_PRESENT	*SNK_VBUS
0x1F	FAULT_STATUS[7:0]	ALL_REG_RST	FORCD_OFF_VBUS	*AUTO_DISCH_FAIL	FORCE_DISCH_FAIL	VBUS_OCP_FAULT	VBUS_OVP_FAULT	VCONN_OCP_FAULT	I2C_ERR
0x20	EXTENDED_STATUS[7:0]	–	–	–	–	–	–	–	VSAFE0V
0x21	ALERT_EXTENDED[7:0]	–	–	–	–	–	TMR_EXP	SRC_FST_RSWP	SNK_FST_RSWP
0x23	COMMAND[7:0]	COMMAND[7:0]							
0x24	DEVICE_CAPABILITIES_1_L[7:0]	PWR_ROLE_CAP[2:0]			SOP_DBG_CAP	SRC_VCONN_CAP	SNK_VBUS_CAP	SRC_HI_VBUS_CAP	SRC_VBUS_CAP
0x25	DEVICE_CAPABILITIES_1_H[7:0]	VBUS_HI_VOLT_TRGT_CAP	VBUS_OCP_RPT_CAP	VBUS_OVP_RPT_CAP	BLEED_DISCH_CAP	FORCE_DISCH_CAP	VBUS_MEAS_ALRM_CAP	SRC_RES_SUP_CAP[1:0]	

ADDRESS	NAME	MSB							LSB
0x26	DEVICE_CAPABILITIES_2_L[7:0]	SNK_DISC_DET_CAP	STP_DISCH_THR_CAP	VBUS_VOLT_ALRM_LSB_CAP[1:0]		VCONN_PWR_CAP[2:0]			VCONN_OCP_CAP
0x27	DEVICE_CAPABILITIES_2_H[7:0]	–	–	GENERIC_TMR_CAP	LONG_MSG_CAP	SMB_PEC_CAP	SRC_FRS_CAP	SNK_FRS_CAP	WDOG_TMR_CAP
0x28	STANDARD_INPUT_CAPABILITIES[7:0]	–	–	–	SRC_FRS_INP_CAP[1:0]		VBUS_EXT_OVP_CAP	VBUS_EXT_OCP_CAP	FRC_OFF_VBUS_CAP
0x29	STANDARD_OUTPUT_CAPABILITIES[7:0]	VBUS_SNK_DIS_DET_CAP	DBG_ACC_CAP	VBUS_PRESENT_CAP	AUD_ACC_CAP	ACT_CBL_CAP	MUX_CONFG_CAP	CONN_PRESENT_CAP	CONN_ORIENT_CAP
0x2A	CONFIG_EXTENDED1[7:0]	–	–	–	–	–	–	FRS_BIDIR	SRC_FRS_IN
0x2E	MESSAGE_HEADER_INFO[7:0]	–	–	–	CBL_PLG	DATA_ROLE	USB_PD[1:0]		PWR_ROLE
0x2F	RECEIVE_DETECT[7:0]	–	EN_CBL_RST	EN_HRD_RST	EN_SOP_DBG2	EN_SOP_DBG1	EN_SOP2	EN_SOP1	EN_SOP
0x30	RECEIVE_BUFFER[7:0]	RECEIVE_BUFFER[7:0]							
0x50	TRANSMIT[7:0]	–	–	*RETRY_COUNTER[1:0]		–	*TX_SOP_MESSAGE[2:0]		
0x51	TRANSMIT_BUFFER[7:0]	TRANSMIT_BUFFER[7:0]							
0x70	VBUS_VOLTAGE_L[7:0]	VBUS_VOLTAGE[7:0]							
0x71	VBUS_VOLTAGE_H[7:0]	–	–	–	–	SCALE_FACTOR[1:0]		VBUS_VOLTAGE[9:8]	
0x74	VBUS_STOP_DISCHARGE_THRESHOLD_L[7:0]	VBUS_STOP_DISCH_THRESHOLD[7:0]							
0x75	VBUS_STOP_DISCHARGE_THRESHOLD_H[7:0]	–	–	–	–	–	–	VBUS_STOP_DISCH_THRESHOLD[9:8]	
0x76	VBUS_VOLTAGE_ALARM_HI_CFG_L[7:0]	VBUS_ALARM_HI_CFG[7:0]							
0x77	VBUS_VOLTAGE_ALARM_HI_CFG_H[7:0]	–	–	–	–	–	–	VBUS_ALARM_HI_CFG[9:8]	
0x78	VBUS_VOLTAGE_ALARM_LO_CFG_L[7:0]	*VBUS_ALARM_LO_CFG[7:0]							
0x79	VBUS_VOLTAGE_ALARM_LO_CFG_H[7:0]	–	–	–	–	–	–	VBUS_ALARM_LO_CFG[9:8]	
Power, Protection and Legacy USB Registers									
0x80	PWR_OUT_CONTROL[7:0]	–	–	VOUT_ILIM[1:0]		–	–	VOUT_SEL[1:0]	
0x81	CABLE_COMP_CONTROL[7:0]	–	–	GAIN[5:0]					

ADDRESS	NAME	MSB							LSB
0x82	RESERVED[7:0]	–	–	–	–	–	–	–	RESERVED
0x83	BUCK_BOOST_SETUP[7:0]	SLP[2:0]			FSW[1:0]		SYNC_DIR	SS_SEL[1:0]	
0x84	WATCHDOG_SETUP[7:0]	–	–	–	–	–	–	WD_TIMEOUT[1:0]	
0x85	AUTO_SHIELD_SETUP[7:0]	–	–	–	–	–	–	RETRY_TMR[1:0]	
0x86	AUTO_CDP_DCP_SETUP[7:0]	–	–	–	–	–	–	AUTO_CDP_DCP_MODE[1:0]	
0x87	IN_THRESH[7:0]	–	–	–	–	IN_UV_THRESH[3:0]			
0x88	VCONN_THRESH[7:0]	–	–	–	VCONN_OCP_SEL	–	VCONN_IN_UV_THRESH[2:0]		
0x89	VBUS_THRESH[7:0]	–	VBUS_OV_THRESH[2:0]			–	VBUS_UV_THRESH[2:0]		
0x8A	AUTO_SHIELD_STATUS_MASK[7:0]	SHIELDING_MASK	–	–	–	VCONN_IN_UV_MASK	IN_OC_MASK	VDD_USB_UV_MASK	VBUS_UV_MASK
0x8B	AUTO_SHIELD_STATUS[7:0]	SHIELDING	–	–	–	VCONN_IN_UV	IN_OC	VDD_USB_UV	VBUS_UV

Register Details

VENDOR_ID_L (0x0)

Lower 8-bits of VID

BIT	7	6	5	4	3	2	1	0
Field	VENDOR_ID[7:0]							
Reset	0x6A							
Access Type	Read Only							
Reset A	0x6A							

BITFIELD	BITS	DESCRIPTION	DECODE
VENDOR_ID	7:0	Lower 8-bits of Maxim VID	Always reads 0x6A in MAX25430

VENDOR_ID_H (0x1)

A Vendor ID, or VID, is used to identify the TCPC vendor. The VID is a unique 16-bit unsigned integer assigned by USB-IF.

BIT	7	6	5	4	3	2	1	0
Field	VENDOR_ID[15:8]							
Reset	0x0B							
Access Type	Read Only							
Reset A	0x0B							

BITFIELD	BITS	DESCRIPTION	DECODE
VENDOR_ID	7:0	Upper 8-bits of Maxim VID	Always reads 0x0B in MAX25430

PRODUCT_ID_L (0x2)

Lower 8-bits of PID

BIT	7	6	5	4	3	2	1	0
Field	PRODUCT_ID[7:0]							
Reset	0x00							
Access Type	Read Only							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
PRODUCT_ID	7:0	Lower 8-bits of MAX25430 PID	Always reads 0x00 in MAX25430

PRODUCT_ID_H (0x3)

The Product ID, or PID, is used to identify the product.

BIT	7	6	5	4	3	2	1	0
Field	PRODUCT_ID[15:8]							
Reset	0x00							
Access Type	Read Only							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
PRODUCT_ID	7:0	Upper 8-bits of MAX25430 PID	Always reads 0x00 in MAX25430

DEVICE_ID_L (0x4)

Lower 8-bits of the DEVICE_ID register.

BIT	7	6	5	4	3	2	1	0
Field	DEVICE_ID[7:0]							
Reset								
Access Type	Read Only							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
DEVICE_ID	7:0	Lower 8-bits of MAX25430's Device ID	See Ordering Table

DEVICE_ID_H (0x5)

Upper 8-bits of the DEVICE_ID register. The Device ID is used to identify the MAX25430 variant. See ordering table at the end of the datasheet.

BIT	7	6	5	4	3	2	1	0
Field	DEVICE_ID[15:8]							
Reset								
Access Type	Read Only							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
DEVICE_ID	7:0	Upper 8-bits of MAX25430's Device ID	See Ordering Table

USBTYPEC_REV_L (0x6)

This register refers to USB Type-C Cable and Connector Specification Revision, USB Type-C represented by a unique 16-bit unsigned register. The format is packed binary coded decimal.

BIT	7	6	5	4	3	2	1	0
Field	TYPEC_REV[7:0]							
Reset	0x13							
Access Type	Read Only							
Reset A	0x13							

BITFIELD	BITS	DESCRIPTION	DECODE
TYPEC_REV	7:0	USB TYPE-C Revision = Release 1.3	Always reads 0x13 in MAX25430

USBPD_REV_VER_L (0x8)

USBPD_REV_VER[15:8]: Lower 8-bits

BIT	7	6	5	4	3	2	1	0
Field	PD_VER[7:0]							
Reset	0x12							
Access Type	Read Only							
Reset A	0x12							

BITFIELD	BITS	DESCRIPTION	DECODE
PD_VER	7:0	USB-PD Version = 1.2	Always reads 0x12 in MAX25430

USBPD_REV_VER_H (0x9)

This register refers to USB PD Specification Revision and Version, USB PD represented by a unique 16-bit unsigned integer. The format is packed binary coded decimal.

BIT	7	6	5	4	3	2	1	0
Field	PD_REV[7:0]							
Reset	0x30							
Access Type	Read Only							
Reset A	0x30							

BITFIELD	BITS	DESCRIPTION	DECODE
PD_REV	7:0	USB-PD Revision = 3.0	Always reads 0x30 in MAX25430

PD_INTERFACE_REV_L (0xA)

PD_INTERFACE_REV[7:0]: Lower 8-bits

BIT	7	6	5	4	3	2	1	0
Field	IBS_VER[7:0]							
Reset	0x11							
Access Type	Read Only							
Reset A	0x11							

BITFIELD	BITS	DESCRIPTION	DECODE
IBS_VER	7:0	USB-PD Inter-Block Specification Version = Version 1.1	Always reads 0x11 in MAX25430

PD_INTERFACE_REV_H (0xB)

The USB-Port Controller Specification Revision register refers to this Specification Revision and Version represented by a unique 16-bit unsigned integer. The format is packed binary coded decimal.

BIT	7	6	5	4	3	2	1	0
Field	IBS_REV[7:0]							
Reset	0x20							
Access Type	Read Only							
Reset A	0x20							

BITFIELD	BITS	DESCRIPTION	DECODE
IBS_REV	7:0	USB-PD Inter-Block Specification = Revision 2.0	Always reads 0x20 in MAX25430

ALERT_L (0x10)

Lower 8-bits of ALERT Register. The following description applies to both ALERT_L and ALERT_H registers:

This register is set by MAX25430 and cleared by TCPM. This register is used to communicate a status change from the MAX25430 to the TCPM. After an event or condition occurs, MAX25430 sets the corresponding bit in the ALERT register. MAX25430 will keep the bit associated with the ALERT asserted until the TCPM writes a 1 to clear it. MAX25430 indicates an alert status change has occurred by presenting a logical 1 in the corresponding alert bit position in this register and asserting the $\overline{\text{ALERT}}$ pin. The TCPM clears the ALERT bit by writing a logical 1 to the respective ALERT bit position. The TCPM can clear any number of ALERT bits in a single write by setting multiple bits to logical 1 and the rest of the bits in the register to logical 0. The TCPM writing a logical 0 to any ALERT bit has no effect, and therefore does not cause those ALERT bits to be set or cleared. The $\overline{\text{ALERT}}$ pin remains asserted until all ALERT bits are cleared by the TCPM. If the TCPM writes a logical 1 to a bit that is already logical 0, MAX25430 will not change the value of that bit.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_ALARM_HI	TX_SOP_MSG_SUCC	TX_SOP_MSG_DISCRD	TX_SOP_MSG_FAIL	RX_HARD_RST	RX_SOP_MSG_STAT	PWR_STAT	HVCC_STAT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read
Reset A	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_HI	7	VBUS Voltage Alarm Hi (MAX25430B only)	0: Cleared 1: A high-voltage alarm has occurred

BITFIELD	BITS	DESCRIPTION	DECODE
TX_SOP_MSG_SUCC	6	Transmit SOP* Message Successful (MAX25430B only)	0: Cleared 1: Reset or SOP* message transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
TX_SOP_MSG_DISCRD	5	Transmit SOP* Message Discarded (MAX25430B only)	0: Cleared 1: Reset or SOP* message transmission not sent due to an incoming receive message. Transmit SOP* message buffer registers are empty.
TX_SOP_MSG_FAIL	4	Transmit SOP* Message Failed (MAX25430B only)	0: Cleared 1: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.
RX_HARD_RST	3	Received Hard Reset (MAX25430B only)	0: Cleared 1: Received Hard Reset message
RX_SOP_MSG_STAT	2	Received SOP* Message Status (MAX25430B only)	0: Cleared 1: RECEIVE_BUFFER register changed. READABLE_BYTE_COUNT being set to 0 does not set this bit.
PWR_STAT	1	Power Status	0: Cleared 1: Power Status changed
HVCC_STAT	0	HVCC Status (MAX25430B only)	0: Cleared 1: HVCC Status changed Set when ROLE_CONTROL.HVCC1[1..0] or ROLE_CONTROL.HVCC2[1..0] has changed. MAX25430B does not assert this bit when HVCC_STATUS.LOOKING4CONN changes state if TCPC_CONTROL.EN_LK4CONN_ALRT is set to 0.

ALERT_H (0x11)

Upper 8-bits of ALERT Register.

Writing a 1 to ALERT.RX_BUFF_OVRFL does not clear it unless the TCPM also writes a 1 to ALERT.RX_SOP_MSG_STAT. The ALERT.RX_BUFF_OVRFL is always asserted if the SOP* buffer registers are full, and those registers can only be cleared by writing a 1 to ALERT.RX_SOP_MSG_STAT.

BIT	7	6	5	4	3	2	1	0
Field	VNDR_ALRT	ALRT_EXTND	EXTND_STAT	BEG_SOP_MSG_STAT	VBUS_SNK_DISC_DET	RX_BUFF_OVRFL	FAULT_STAT	VBUS_ALARM_LO
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Read Only	Write 1 to Clear, Read	Read Only	Read Only	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read
Reset A	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
VNDR_ALRT	7	Vendor Defined Alert	0: Cleared 1: A vendor defined alert has been detected. Defined in the VENDOR_DEFINED registers starting at address 0x80. This bit can be cleared, regardless of the current status of the alert source.
ALRT_EXTND	6	Alert Extended (Reserved)	Always reads 0 in MAX25430 (Extended Alerts not supported)
EXTND_STAT	5	Extended Status	0: Cleared 1: Extended Status changed
BEG_SOP_MSG_STAT	4	Beginning SOP* Message Status (MAX25430B only)	Always reads 0 in MAX25430 (Extended messaging not supported)
VBUS_SNK_DISC_DET	3	VBUS Sink Disconnect Detected (MAX25430B only)	Always reads 0 in MAX25430 (Source-only)
RX_BUFF_OVRFL	2	Rx Buffer Overflow (MAX25430B only)	0: TCPC Rx buffer is functioning properly 1: TCPC Rx buffer has overflowed. Future GoodCRC shall not be sent. This bit is cleared when the TCPM writes a 1 to it and a 1 to ALERT.RX_SOP_MSG_STAT.
FAULT_STAT	1	Fault Status	0: No fault 1: A fault has occurred. Read the FAULT_STATUS register
VBUS_ALARM_LO	0	VBUS Voltage Alarm Lo (MAX25430B only)	0: Cleared 1: A low-voltage alarm has occurred

ALERT_MASK_L (0x12)

Lower 8-bits of the 16-bit ALERT_MASK register.

This is an event interrupt mask register. It is masked and unmasked by the TCPM. The ALERT_MASK_L register is cleared by the TCPM. This register shall be initialized by the TCPM upon power on or Hard Reset. The assertion of the $\overline{ALERT}$ pin is prevented when the corresponding bit in this register is set to zero by the TCPM. Setting any bits in this register has no effect on the ALERT_L register.

BIT	7	6	5	4	3	2	1	0
Field	MSK_VBUS_V_ALRM_HI	MSK_TX_SOP_MSG_SUCC	MSK_TX_SOP_MSG_DISCRD	MSK_TX_SOP_MSG_FAIL	MSK_RX_HARD_RST	MSK_RX_SOP_MSG_STAT	MSK_PWR_STAT	MSK_HVCC_STAT
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext
Reset A	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_VBUS_V_ALRM_HI	7	VBUS Voltage Alarm Hi Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_TX_SOP_MSG_SUCC	6	Transmit SOP* Message Successful Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_TX_SOP_MSG_DISCRD	5	Transmit SOP* Message Discarded Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_TX_SOP_MSG_FAIL	4	Transmit SOP* Message Failed Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_RX_HARD_RST	3	Received Hard Reset Message Status Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_RX_SOP_MSG_STAT	2	Receive SOP* Message Status Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_PWR_STAT	1	Power Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_HVCC_STAT	0	CC Status Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked

ALERT_MASK_H (0x13)

Upper 8-bits of the 16-bit ALERT_MASK register.

This is an event interrupt mask register. It is masked and unmasked by the TCPM. The ALERT_MASK_H register is cleared by the TCPM. This register shall be initialized by the TCPM upon power on or Hard Reset. The assertion of the $\overline{\text{ALERT}}$ pin is prevented when the corresponding bit in this register is set to zero by the TCPM. Setting any bits in this register has no effect on ALERT_H register.

BIT	7	6	5	4	3	2	1	0
Field	MSK_VNDR_ALRT	MSK_ALRT_EXTND	MSK_EXTND_STAT	MSK_BEG_SOP_MSG_STAT	MSK_VBUS_SNK_DISC_DET	MSK_RX_BUFF_OVRFL	MSK_FAULT_STAT	MSK_VBUS_V_ALRM_LO
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext	Write, Read, Ext
Reset A	0b1	0b0	0b0	0b0	0b0	0b0	0b1	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_VNDR_ALRT	7	Vendor Defined Alert Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_ALRT_EXTND	6	Alert Extended Interrupt Mask (Reserved)	Writes are not applicable in MAX25430 (Alert Extended not supported)
MSK_EXTND_STAT	5	Extended Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_BEG_SOP_MSG_STAT	4	Beginning SOP* Message Status Interrupt Mask (Reserved)	Writes are not applicable in MAX25430 (Extended messaging not supported)
MSK_VBUS_SNK_DISC_DET	3	VBUS Sink Disconnect Detected Interrupt Mask (Reserved)	Writes are not applicable in MAX25430 (Source-only)
MSK_RX_BUFF_OVRFL	2	Rx Buffer Overflow Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_FAULT_STAT	1	Fault Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_VBUS_V_ALRM_LO	0	VBUS Voltage Alarm Lo Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked

POWER_STATUS_MASK (0x14)

This is an event interrupt mask. It is masked and unmasked by the TCPM. This register allows individual masking of power events. The POWER_STATUS_MASK register is cleared by the TCPM. This register shall be initialized by the TCPM upon power on or Hard Reset. The assertion of the $\overline{\text{ALERT}}$ pin is prevented when the corresponding bit is set to zero by the TCPM. Setting any bits in this register has no effect on the POWER_STATUS register.

BIT	7	6	5	4	3	2	1	0
Field	MSK_DEBG_ACC_CONN_STAT	MSK_INIT_STAT	MSK_SRC_NON_DEF_VOLT_STAT	MSK_SRC_VBUS_STAT	MSK_VBUS_DET_STAT	MSK_VBUS_PRSN_STAT	MSK_VCONN_PRSN_STAT	MSK_SNK_VBUS_STAT
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Reset A	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_DEBG_ACC_CONN_STAT	7	Debug Accessory Connected Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_INIT_STAT	6	MAX25430 Initialization Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_SRC_NON_DEF_VOLT_STAT	5	Sourcing High Voltage Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_SRC_VBUS_STAT	4	Sourcing VBUS Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_DET_STAT	3	VBUS Detection Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_PRSN_STAT	2	VBUS Present Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_VCONN_PRSN_STAT	1	VCONN Present Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_SNK_VBUS_STAT	0	Sinking VBUS Status Interrupt Mask (Reserved)	Writes are not applicable in MAX25430 (Force Off VBUS not supported)

FAULT_STATUS_MASK (0x15)

This is an event interrupt mask. It is masked and unmasked by the TCPM. This register allows individual masking of fault events. The FAULT_STATUS_MASK Register is cleared by the TCPM. The FAULT_STATUS_MASK Register shall be initialized upon power on or Hard Reset.

The assertion of the $\overline{\text{ALERT}}$ pin is prevented when the corresponding bit is set to zero by the TCPM. Setting any bits in this register has no effect on the FAULT_STATUS register.

BIT	7	6	5	4	3	2	1	0
Field	MSK_All_REG_RST	MSK_FORCD_OFF_VBUS	MSK_AUTO_DISCH_FAIL	MSK_FORC_DISCH_FAIL	MSK_VBUS_OCP	MSK_VBUS_OVP	MSK_VCONN_OCP	MSK_I2C_ERR
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Reset A	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_All_REG_RST	7	All Registers Reset To Default Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_FORCD_OFF_VBUS	6	Force Off VBUS Interrupt Status Mask (Reserved)	Writes are not applicable in MAX25430 (Force Off VBUS not supported)
MSK_AUTO_DISCH_FAIL	5	Auto Discharge Failed Interrupt Mask (MAX25430B only)	0: Interrupt masked 1: Interrupt unmasked
MSK_FORC_DISCH_FAIL	4	Force Discharge Failed Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_OCP	3	VBUS Over Current Protection Fault Interrupt Status Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_VBUS_OVP	2	VBUS Over Voltage Protection Fault Interrupt Status Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_VCONN_OCP	1	Vconn Over Current Fault Interrupt Status Mask	0: Interrupt masked 1: Interrupt unmasked
MSK_I2C_ERR	0	I2C Interface Error Interrupt Status Mask	0: Interrupt masked 1: Interrupt unmasked

EXTENDED_STATUS_MASK (0x16)

This is an event interrupt mask. It is masked and unmasked by the TCPM. The EXTENDED_STATUS_MASK register is cleared by the TCPM. This register shall be initialized upon power on or Hard Reset. The assertion of the $\overline{\text{ALERT}}$ pin is prevented when the corresponding bit is set to zero by the TCPM. Setting any bits in this register has no effect on the EXTENDED_STATUS register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MSK_VSAFE0V
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read
Reset A	–	–	–	–	–	–	–	0b1

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_VSAFE0V	0	vSafe0V Status Interrupt Mask	0: Interrupt masked 1: Interrupt unmasked

ALERT_EXTENDED_MASK (0x17)

This register is not applicable to MAX25430.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MSK_TMR_EXP	MSK_SRC_FST_RSWP	MSK_SNK_FST_RSWP
Reset	–	–	–	–	–	0b1	0b1	0b1
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read
Reset A	–	–	–	–	–	0b1	0b1	0b1

BITFIELD	BITS	DESCRIPTION	DECODE
MSK_TMR_EXP	2	Timer Expired Interrupt Mask (Reserved)	Writes are not applicable in MAX25430 (Generic Timer not supported)
MSK_SRC_FST_RSWP	1	Source Fast Role Swap Interrupt Mask (Reserved)	Writes are not applicable in MAX25430 (Fast Role Swap not supported)
MSK_SNK_FST_RSWP	0	Sink Fast Role Swap Interrupt Mask (Reserved)	Writes are not applicable in MAX25430 (Source-only)

CONFIG_STANDARD_OUTPUT (0x18)

CONFIGURE STANDARD OUTPUT[7:0]:

This read/write register is used to configure the Standard Outputs or read the status of the Standard Outputs and is optional normative per the TCPCI specification. Since the MAX25430 does not support any Standard Outputs, this register is only used by the TCPM to read reset values, if needed.

BIT	7	6	5	4	3	2	1	0
Field	HI_IMPD_OUT	DBG_ACC_CONN	AUDIO_ACC_CONN	ACTV_CABL_CONN	MUX_CNTRL[1:0]		CONN_PRSNT	CONN_ORIENT
Reset	0b0	0b1	0b1	0b0	0b00		0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read
Reset A	0b0	0b1	0b1	0b0	0b00		0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
HI_IMPD_OUT	7	"High Impedance Output" Output Pin Control (Reserved)	Writes are not applicable in MAX25430 ("High Impedance Output" Pin not implemented)
DBG_ACC_CONN	6	"Debug Accessory Connected#" Output Pin Control (Reserved)	0: A Debug Accessory is connected 1: No Debug Accessory is connected (default)
AUDIO_ACC_CONN	5	"Audio Accessory Connected#" Output Pin Control (Reserved)	Writes are not applicable in MAX25430 ("Audio Accessory Connected#" Output Pin not implemented)
ACTV_CABL_CONN	4	"Active Cable Connected" Output Pin Control (Reserved)	Writes are not applicable in MAX25430 ("Active Cable Connected" Output Pin not implemented)
MUX_CNTRL	3:2	"MUX Control" Output Pin Control (Reserved)	Writes are not applicable in MAX25430 ("MUX Control" Output Pin not implemented)
CONN_PRSNT	1	"Connection Present" Output Pin Control (Reserved)	Writes are not applicable in MAX25430 ("Connection Present" Output Pin not implemented)
CONN_ORIENT	0	"Connector Orientation" Output Pin Control (Reserved)	Writes are not applicable in MAX25430 ("Connector Orientation" Output Pin not implemented)

TCPC_CONTROL (0x19)

After the TCPC has set the power on reset default values, this register is set and cleared only by the TCPM. The TCPM writes to this register to set the Plug Orientation.

BIT	7	6	5	4	3	2	1	0
Field	EN_SMB_PEC	EN_LK4CONN_ALRT	EN_WD_TMR	DBG_ACC_CNTRL	I2C_CLK_STRCH[1:0]		BIST_TM	PLUG_ORNT
Reset	0b0	0b0	0b0	0b0	0b00		0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Read Only		Write, Read	Write, Read
Reset A	0b0	0b0	0b0	0b0	0b00		0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
EN_SMB_PEC	7	Enable SMBus PEC (Reserved)	Writes are ignored and always reads 0 in MAX25430 (SMBus PEC not supported)
EN_LK4CONN_ALRT	6	Enable Looking4Connection Alert (MAX25430B only)	0: Disable ALERT_L.HVCC_STAT assertion when HVCC_STATUS.LOOKING4CONN changes (default) 1: Enable ALERT_L.HVCC_STAT assertion when HVCC_STATUS.LOOKING4CONN changes
EN_WD_TMR	5	Enable Watchdog Timer	0: Watchdog Timer is disabled (default) 1: Watchdog Timer is enabled See Watchdog Timer section for more information
DBG_ACC_CNTRL	4	Debug Accessory Control (MAX25430B only)	0: Disabled (power on default) 1: Controlled by TCPM
I2C_CLK_STRCH	3:2	I2C Clock Stretching Control (Reserved)	Writes are ignored and always reads 0 in MAX25430 (I2C Clock Stretching not supported)
BIST_TM	1	BIST Test Mode (MAX25430B) Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the TCPC. The TCPM should clear this bit when a disconnect is detected.	0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert. 1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert. The TCPM can mask or ignore received message alerts when this bit is set to 1 since the TCPC may or may not assert the alert. The TCPM may also treat received messages in this mode in the same way as received messages during normal operation.

BITFIELD	BITS	DESCRIPTION	DECODE
PLUG_ORNT	0	Plug Orientation	0: When VCONN is enabled, apply it to the CC2 pin. MAX25430B only: MAX25430B monitors the CC1 pin for BMC communications if PD message delivery is enabled. 1: When VCONN is enabled, apply it to the CC1 pin. MAX25430B only: MAX25430B monitors the CC2 pin for BMC communications if PD message delivery is enabled.

ROLE_CONTROL (0x1A)

After the TCPC has set the power on reset default values, this register is set and cleared only by the TCPM. The TCPM writes to this register to configure the CC pull up (Rp) current sources.

BIT	7	6	5	4	3	2	1	0
Field	–	DRP	RP_VAL[1:0]		HVCC2[1:0]		HVCC1[1:0]	
Reset	–	0b0	0b00		0b01		0b01	
Access Type	–	Read Only	Write, Read		Write, Read		Write, Read	
Reset A	–	0b0	0b11		0b11		0b11	

BITFIELD	BITS	DESCRIPTION	DECODE
DRP	6	DRP (Reserved)	Writes are ignored and always reads 0 in MAX25430 (DRP not supported)
RP_VAL	5:4	Rp Value Setting (MAX25430B only)	00: Rp default 01: Rp 1.5A 10: Rp 3.0A 11: Reserved
HVCC2	3:2	HVCC2 Control (MAX25430B only)	00: Reserved 01: Rp 10: Reserved 11: Open (Disconnect or don't care)
HVCC1	1:0	HVCC1 Control (MAX25430B only)	00: Reserved 01: Rp 10: Reserved 11: Open (Disconnect or don't care)

FAULT_CONTROL (0x1B)

After the TCPC has set the power on reset default values, this register is set and cleared only by the TCPM. The TCPM writes to FAULT_CONTROL to enable/disable the reporting of certain faults.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FRC_OFF_VBUS_DIS	VBUS_DISCH_FLT_DET_TMR_EN	VBUS_OCP_DET_EN	VBUS_OVP_DET_EN	VCONN_OCP_DET_EN
Reset	–	–	–	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	–	Read Only	Write, Read	Write, Read	Write, Read	Write, Read
Reset A	–	–	–	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
FRC_OFF_VBUS_DIS	4	Force Off VBUS (Reserved)	Writes are ignored and always reads 0b in MAX25430 (Force Off Vbus control not supported)
VBUS_DISCH_FLT_DET_TMR_EN	3	VBUS Discharge Fault Detection Timer	0: VBUS Discharge Fault Detection Timer enabled 1: VBUS Discharge Fault Detection Timer disabled This enables the timers for both FAULT_STATUS.AUTO_DISCH_FAIL and FAULT_STATUS.FORCE_DISCH_FAIL
VBUS_OCP_DET_EN	2	Internal OCP VBUS Over Current Protection Fault	0: Fault detection circuit enabled 1: Fault detection circuit disabled
VBUS_OVP_DET_EN	1	Internal OVP VBUS Over Voltage Protection Fault	0: Internal OVP circuit enabled 1: Internal OVP circuit disabled
VCONN_OCP_DET_EN	0	VCONN Over Current Fault	0: Fault detection circuit enabled 1: Fault detection circuit disabled

POWER_CONTROL (0x1C)

After the TCPC has set the power on reset default values, this register is set and cleared by the TCPM.

BIT	7	6	5	4	3	2	1	0
Field	FAST_RSWP_EN	VBUS_VOLT_MON_EN	VOLT_ALRMS_EN	AUTO_DISCH_DISC_EN	BLED_DISCH_EN	FORC_DISCH_EN	VCONN_PWR_SUPP	EN_VCONN
Reset	0b0	0b1	0b1	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Write, Read	Write, Read	Write, Read	Read Only	Write, Read	Write, Read	Write, Read, Dual
Reset A	0b0	0b1	0b1	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
FAST_RSWP_EN	7	Fast Role Swap Enable (Reserved)	Writes are ignored and always reads 0 in MAX25430 (Fast Role Swap not supported)
VBUS_VOLT_MON_EN	6	VBUS_VOLTAGE Monitor: (MAX25430B only)	0: Enables VBUS Voltage Monitoring (ADC) 1: Disables VBUS Voltage Monitoring (default)
VOLT_ALRMS_EN	5	Disable Voltage Alarms (MAX25430B only)	0: Enables Voltage Alarms Power status reporting 1: Disables Voltage Alarms Power status reporting (default)
AUTO_DISCH_DISC_EN	4	Auto Discharge Disconnect (MAX25430B only)	0: MAX25430B does not automatically discharge VBUS based on VBUS voltage (default) 1: MAX25430B automatically discharges VBUS
BLED_DISCH_EN	3	Enable Bleed Discharge (Reserved)	Writes are ignored and always reads 0 in MAX25430 (Bleed Discharge not supported)
FORC_DISCH_EN	2	Force Discharge	0: Disable VBUS Force Discharge (default) 1: Enable VBUS Force Discharge
VCONN_PWR_SUPP	1	VCONN Power Supported	0: Deliver at least 1W on VCONN 1: Deliver at least the power indicated in DEVICE_CAPABILITIES.VCONNPowerSupported Writing to this register has no affect in MAX25430 (always 1W).

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VCONN	0	Enable VCONN	0: Disable VCONN Source (default) 1: Enable VCONN Source to CC The MAX25430 autonomously disables VCONN by clearing EN_VCONN when SHIELDING is active.

HVCC_STATUS (0x1D)

This register is set and cleared by the TCPC. The TCPC will update this register within 50µs (max.) of a change on the HVCC1 or HVCC2 wires, after debounce.

BIT	7	6	5	4	3	2	1	0
Field	–	–	LOOKING4CONN	CONN_RSLT	HVCC2_STATE[1:0]		HVCC1_STATE[1:0]	
Reset	–	–	0b0	0b0	0b00		0b00	
Access Type	–	–	Read Only	Read Only	Read Only		Read Only	
Reset A	–	–	0b0	0b0	0b11		0b11	

BITFIELD	BITS	DESCRIPTION	DECODE
LOOKING4CONN	5	Looking4Connection (MAX25430B only)	0: MAX25430B is not actively looking for a connection 1: MAX25430B is looking for a connection A transition from 1 to 0 indicates a potential connection has been found.
CONN_RSLT	4	ConnectResult (Reserved)	Always reads 0 in MAX25430 (Source Only)
HVCC2_STATE	3:2	HVCC2 State (MAX25430B only)	00: SRC.Open (Open, Rp) 01: SRC.Ra (below maximum vRa) 10: SRC.Rd (within the vRd range) 11: Reserved
HVCC1_STATE	1:0	HVCC1 State (MAX25430B only)	00: SRC.Open (Open, Rp) 01: SRC.Ra (below maximum vRa) 10: SRC.Rd (within the vRd range) 11: Reserved

POWER_STATUS (0x1E)

This register is set and cleared by the TCPC. The TCPM reads this register upon detecting an ALERT and reading the ALERT.PowerStatus bit set to 1. The TCPC indicates the current Power Status in this register.

BIT	7	6	5	4	3	2	1	0
Field	DBG_ACC_STAT	INIT_STAT	SRC_NON_DEF_VOLT	SRC_VBUS	VBUS_DET_EN	VBUS_PRESENT	VCONN_PRESENT	*SNK_VBUS
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Reset A	0b0	0b0	0b0	0b0	0b1	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
DBG_ACC_STAT	7	Debug Accessory Status	0: No Debug Accessory connected (default) 1: Debug Accessory connected

BITFIELD	BITS	DESCRIPTION	DECODE
INIT_STAT	6	MAX25430 Initialization Status	0: The MAX25430 has completed initialization and all registers are valid 1: The MAX25430 is still performing internal initialization and the only registers that are guaranteed to return the correct values are 0x00...0x0B
SRC_NON_DEF_VOLT	5	Sourcing Nondefault VBUS Voltage	0: Sourcing vSafe5V Voltage on VBUS 1: Sourcing Nondefault Voltage on VBUS This bit is asserted as long as MAX25430 is sourcing nondefault voltage over VBUS (i.e. not vSafe5V) as a response to TCPM sending the SourceVbusNondefaultVoltage command. This bit is not valid if POWER_STATUS.SRC_VBUS = 0.
SRC_VBUS	4	Sourcing VBUS	0: MAX25430 is not sourcing VBUS 1: MAX25430 is sourcing VBUS
VBUS_DET_EN	3	VBUS Detection Enabled	0: VBUS Detection Disabled 1: VBUS Detection Enabled (default)
VBUS_PRESENT	2	VBUS Present Status	0: VBUS is not present (below 4V) 1: VBUS is present (4V or above)
VCONN_PRESENT	1	VCONN Present Status	0: VCONN is not present 1: This bit is asserted whenever VCONN is present on HVCC1 or HVCC2
*SNK_VBUS	0	Sinking VBUS Status (Reserved)	Always reads 0 in MAX25430 (Source Only)

FAULT_STATUS (0x1F)

This register is set by TCPC and cleared by TCPM. The TCPM reads this register upon detecting an ALERT and reading the ALERT.Fault bit set to 1. The TCPC indicates the current fault status in this register.

BIT	7	6	5	4	3	2	1	0
Field	ALL_REG_RST	FORCD_OFF_VBUS	*AUTO_DISCH_FAIL	FORCE_DISCH_FAIL	VBUS_OCP_FAULT	VBUS_OVP_FAULT	VCONN_OCP_FAULT	I2C_ERR
Reset	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read	Write 1 to Clear, Read
Reset A	0b1	0b0	0b0	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
ALL_REG_RST	7	All Registers Reset To Default	0: Registers have not been reset to their default values 1: All Registers have been initialized to their default values This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs.
FORCD_OFF_VBUS	6	Force Off VBUS (Reserved)	Writes are ignored and always reads 0 in MAX25430 (Force Off VBUS not supported)

BITFIELD	BITS	DESCRIPTION	DECODE
*AUTO_DISCH_FAIL	5	VBUS Auto Discharge Failed (MAX25430B only)	0: No Fault 1: VBUS Auto Discharge commanded by the TCPM failed
FORCE_DISCH_FAIL	4	VBUS Force Discharge Failed	0: No Fault 1: VBUS Force Discharge commanded by the TCPM failed
VBUS_OCP_FAULT	3	VBUS Overcurrent Protection Fault	0: No Fault 1: VBUS Overcurrent Fault latched
VBUS_OVP_FAULT	2	VBUS Overvoltage Protection Fault	0: No Fault 1: VBUS Overvoltage Fault latched
VCONN_OCP_FAULT	1	VCONN Over Current Protection Fault	0: No Fault detected 1: Over current VCONN protection fault latched
I2C_ERR	0	I2C Interface Error	0: No Error 1: An I2C error has occurred The following conditions will cause MAX25430 to assert this bit: ● The TCPM writes to the TRANSMIT register when the TRANSMIT_BUFFER is empty. (MAX25430B only) ● The watchdog timer has expired ● The TCPM writes an invalid COMMAND ● The TCPM tells the MAX25430B to turn on VBUS and a Pre-bias exists on VBUS that cannot be discharged.

EXTENDED_STATUS (0x20)

This register is set and cleared by the TCPC. The TCPM reads this register upon detecting an ALERT and reading the ALERT.ExtendedStatus bit set to 1.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	VSAFE0V
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only
Reset A	–	–	–	–	–	–	–	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
VSAFE0V	0	vSafe0V Status	0: VBUS is above vSafe0V 1: VBUS is at or below vSafe0V MAX25430 will report Vbus is at or below vSafe0V when the OUT pin is below 0.8V (typ.). This bit is not valid when POWER_STATUS.VBUS_DET_EN = 0

ALERT_EXTENDED (0x21)

This register is not applicable to MAX25430.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	TMR_EXP	SRC_FST_RSWP	SNK_FST_RSWP
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only
Reset A	–	–	–	–	–	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
TMR_EXP	2	Generic Timer Expired (Reserved)	Writes are ignored and always reads 0 (Generic timer not supported)
SRC_FST_RSWP	1	Source Fast Role Swap (Reserved)	Writes are ignored and always reads 0 (Fast Role Swap not supported)
SNK_FST_RSWP	0	Sink Fast Role Swap (Reserved)	Writes are ignored and always reads 0 (Source-only)

COMMAND (0x23)

The COMMAND register is issued and written by the TCPM. The COMMAND register is cleared by the MAX25430 after being acted upon.The TCPM shall issue COMMAND.Look4Connection to enable the MAX25430B to restart Connection Detection. An example of this is when a potential connection as a Source occurred but was further debounced by the TCPM to find the Sink disconnected. In this case the TCPM state machine will go back to its Unattached.Src state. This would result in ROLE_CONTROL staying the same.

The TCPM shall issue COMMAND.SourceVbusNondefaultVoltage to enable the MAX25430 to transition the VBUS source to a Non-Default voltage level. The target voltage for COMMAND.SourceVbusNondefaultVoltage is set in the PWR_OUT_CONTROL.VOUT_SEL[2..0]. The steps of transitioning to source a nondefault voltage over VBUS shall be as follow:

1. MAX25430 supplies vSafe5V over VBUS
2. TCPM writes to PWR_OUT_CONTROL.VOUT_SEL[2..0] to set the voltage target level
3. TCPM issues COMMAND.SourceVbusNondefaultVoltage (only for Default to Non-Default transitions)
4. MAX25430 starts the operation of transitioning to the target voltage level.

If the TCPM has a new target voltage level for COMMAND.SourceVbusNondefaultVoltage, it shall repeat Step 2, only. The TCPM is not required to go back to vSafe5V and then to a different voltage. It may go directly to the new voltage by writing new values to PWR_OUT_CONTROL.VOUT_SEL[2..0]. The TCPM shall not perform Step 3 for Non-Default to Non-Default voltage transitions. Doing so will trigger an I2C error flag by the MAX25430.

BIT	7	6	5	4	3	2	1	0
Field	COMMAND[7:0]							
Reset	0x00							
Access Type	Write, Read, Ext							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
COMMAND	7:0	Supported Commands	0x11: Reserved 0x22: DisableVbusDetect 0x33: EnableVbusDetect 0x66: DisableSourceVbus 0x77: SourceVbusDefaultVoltage 0x88: SourceVbusNondefaultVoltage 0x99: Look4Connection (MAX25430B only) 0xAA: RxOneMore (MAX25430B only) 0xCC: Reserved 0xDD: ResetTransmitBuffer (MAX25430B only) 0xEE: ResetReceiveBuffer (MAX25430B only) 0xFF: Reserved When COMMAND 0x77 is written to enable sourcing default voltage over VBUS, MAX25430 will automatically enable VBUS detection by setting POWER_STATUS.VBUS_DET_EN = 1

DEVICE_CAPABILITIES_1_L (0x24)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	PWR_ROLE_CAP[2:0]			SOP_DBG_CAP	SRC_VCONN_CAP	SNK_VBUS_CAP	SRC_HI_VBUS_CAP	SRC_VBUS_CAP
Reset	0b001			0b1	0b1	0b0	0b1	0b1
Access Type	Read Only			Read Only	Read Only	Read Only	Read Only	Read Only
Reset A	0b111			0b0	0b1	0b0	0b1	0b1

BITFIELD	BITS	DESCRIPTION	DECODE
PWR_ROLE_CAP	7:5	Power Roles Supported (MAX25430B only)	001: Source only. Rp 3.0A, 1.5A, and default indicated in DEVICE_CAPABILITIES_1_H.SRC_RES_SUP_CAP
SOP_DBG_CAP	4	SOP'_DBG/SOP"_DBG Support (MAX25430B only)	1: All SOP* messages are supported
SRC_VCONN_CAP	3	Source VCONN Capability	1: MAX25430 is capable of sourcing VCONN through its switch
SNK_VBUS_CAP	2	Sink VBUS Capability	0: MAX25430 is not capable of controlling the sink path to the system load (Source only).
SRC_HI_VBUS_CAP	1	Source Nondefault VBUS Capability	1: MAX25430 is capable of sourcing Nondefault voltages on VBUS.
SRC_VBUS_CAP	0	Source VBUS Capability	1: MAX25430 is capable of controlling the source path to VBUS

DEVICE_CAPABILITIES_1_H (0x25)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_HI_VOLT_TRGT_CAP	VBUS_OCP_RPT_CAP	VBUS_OVP_RPT_CAP	BLEED_DISCH_CAP	FORCE_DISCH_CAP	VBUS_MEAS_ALRM_CAP	SRC_RES_SUP_CAP[1:0]	
Reset	0b0	0b1	0b1	0b0	0b1	0b1	0b10	
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	
Reset A	0b0	0b1	0b1	0b0	0b1	0b0	0b11	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_HI_VOLT_TRGT_CAP	7	VBUS High Voltage Target Capability	0: VBUS_HV_TARGET register not supported The VBUS_HV_TARGET register can also be refered as VBUS_NONDEFAULT_TARGET.
VBUS_OCP_RPT_CAP	6	VBUS OCP Reporting Capability	1: Supported
VBUS_OVP_RPT_CAP	5	VBUS OVP Reporting Capability	1: Supported
BLEED_DISCH_CAP	4	Bleed Discharge Capability	0: Not supported
FORCE_DISCH_CAP	3	Force Discharge Capability	1: Supported
VBUS_MEAS_ALRM_CAP	2	VBUS Measurement and Alarm Capabilities	1: Supported
SRC_RES_SUP_CAP	1:0	Source Resistor Supported (MAX25430B only)	10: Rp 3.0A, 1.5A, and default

DEVICE_CAPABILITIES_2_L (0x26)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	SNK_DISC_DET_CAP	STP_DISCH_THR_CAP	VBUS_VOLT_ALRM_LSB_CAP[1:0]		VCONN_PWR_CAP[2:0]			VCONN_OCP_CAP
Reset	0b0	0b1	0b00		0b000			0b1
Access Type	Read Only	Read Only	Read Only		Read Only			Read Only
Reset A	0b0	0b1	0b11		0b000			0b1

BITFIELD	BITS	DESCRIPTION	DECODE
SNK_DISC_DET_CAP	7	Sink Disconnect Detection Capability	0: VBUS_SINK_DISCONNECT_THRESHOLD not supported (Source only)
STP_DISCH_THR_CAP	6	VBUS Stop Discharge Threshold Capability	1: VBUS_STOP_DISCHARGE_THRESHOLD supported
VBUS_VOLT_ALRM_LSB_CAP	5:4	VBUS Voltage Alarm LSB Capability	00: MAX25430B has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 11: Not supported on MAX25430A
VCONN_PWR_CAP	3:1	VCONN Power Supported	000: 1W

BITFIELD	BITS	DESCRIPTION	DECODE
VCONN_OCP_CAP	0	VCONN Overcurrent Fault Capability	1: Supported

DEVICE_CAPABILITIES_2_H (0x27)

This register is in the nonvolatile memory of the TCPC. This register describes features supported by the TCPC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	GENERIC_TMR_CAP	LONG_MSG_CAP	SMB_PEC_CAP	SRC_FRS_CAP	SNK_FRS_CAP	WDOG_TMR_CAP
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Reset A	–	–	0b0	0b0	0b0	0b0	0b0	0b1

BITFIELD	BITS	DESCRIPTION	DECODE
GENERIC_TMR_CAP	5	Generic Timer Capability	0: Not supported
LONG_MSG_CAP	4	Long Message Capability	0: Long Messages (264 bytes) not supported. MAX25430 supports up to 30 bytes content of the SOP* message.
SMB_PEC_CAP	3	SMBus PEC Capability	0: Not supported
SRC_FRS_CAP	2	Source FR Swap Capability	0: Not supported
SNK_FRS_CAP	1	Sink FR Swap Capability	0: Not supported
WDOG_TMR_CAP	0	Watchdog Timer Capability	1: Supported

STANDARD_INPUT_CAPABILITIES (0x28)

Standard Inputs are not supported on MAX25430.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	SRC_FRS_INP_CAP[1:0]		VBUS_EXT_OVP_CAP	VBUS_EXT_OCP_CAP	FRC_OFF_VBUS_CAP
Reset	–	–	–	0b00		0b0	0b0	0b0
Access Type	–	–	–	Read Only		Read Only	Read Only	Read Only
Reset A	–	–	–	0b00		0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
SRC_FRS_INP_CAP	4:3	Source Fast Role Swap Standard Input Capability	00: Not supported
VBUS_EXT_OVP_CAP	2	VBUS External Overvoltage Fault Standard Input Capability	0: Not supported
VBUS_EXT_OCP_CAP	1	VBUS External Overcurrent Fault Standard Input Capability	0: Not supported
FRC_OFF_VBUS_CAP	0	Force Off VBUS Standard Input Capability	0: Not supported

STANDARD_OUTPUT_CAPABILITIES (0x29)

Standard Outputs are not supported on MAX25430

BIT	7	6	5	4	3	2	1	0
Field	VBUS_SNK_DIS_DET_CAP	DBG_ACC_CAP	VBUS_PRESENT_CAP	AUD_ACC_CAP	ACT_CBL_CAP	MUX_CONFG_CAP	CONN_PRESENT_CAP	CONN_ORIENT_CAP
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Reset A	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_SNK_DIS_DET_CAP	7	VBUS Sink Disconnect Detect Standard Output Capability	0: Not supported
DBG_ACC_CAP	6	Debug Accessory Standard Output Capability	0: Not supported
VBUS_PRESENT_CAP	5	VBUS Present Monitor Standard Output Capability	0: Not supported
AUD_ACC_CAP	4	Audio Adapter Accessory Standard Output Capability	0: Not supported
ACT_CBL_CAP	3	Active Cable Indicator Standard Output Capability	0: Not supported
MUX_CONFG_CAP	2	MUX Configuration Control Standard Output Capability	0: Not supported
CONN_PRESENT_CAP	1	Connection Present Standard Output Capability	0: Not supported
CONN_ORIENT_CAP	0	Connector Orientation Standard Output Capability	0: Not supported

CONFIG_EXTENDED1 (0x2A)

This register is not applicable to MAX25430.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	FRS_BIDIR	SRC_FRS_IN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read, Ext	Read Only
Reset A	–	–	–	–	–	–	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
FRS_BIDIR	1	Fast Role Swap Bidirectional Pin (Reserved)	Writes to this bit are ignored and will assert FAULT_STATUS.I2C_ERR. Always reads 0.
SRC_FRS_IN	0	Standard Input Source FR Swap (Reserved)	Writes are ignored and always reads 0 (Standard Input Source FR Swap not supported)

MESSAGE_HEADER_INFO (0x2E)

The TCPC sets this register at power on. The TCPM may overwrite this register after TCPC initialization is complete.

On attach and after implementing the tCCDebounce delay (defined in the USB Type-C Specification), the TCPM shall

update this register first before writing to the RECEIVE_DETECT register.

The TCPC reads from this register to generate the Message header for the GoodCRC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CBL_PLG	DATA_ROLE	USB_PD[1:0]		PWR_ROLE
Reset	–	–	–	0b0	0b1	0b10		0b1
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		Write, Read
Reset A	–	–	–	0b0	0b1	0b10		0b1

BITFIELD	BITS	DESCRIPTION	DECODE
CBL_PLG	4	Cable Plug (MAX25430B only)	0: Message originated from Source, Sink, or DRP 1: Message originated from a Cable Plug
DATA_ROLE	3	Data Role (MAX25430B only)	0: UFP 1: DFP
USB_PD	2:1	USB PD Specification Revision (MAX25430B only)	00: Revision 1.0 01: Revision 2.0 10: Revision 3.0 11: Reserved
PWR_ROLE	0	Power Role (MAX25430B only)	0: Sink 1: Source

RECEIVE_DETECT (0x2F)

Set by TCPM, cleared by TCPM (and/or TCPC in some instances).

The TCPM notifies the TCPC of the message type and/or signaling types to be detected. The TCPM should not set any bits in this register until it is able to respond. The TCPC responds to the enabled message type with a GoodCRC if it is a SOP* message, except in the case of a GoodCRC message.

BIT	7	6	5	4	3	2	1	0
Field	–	EN_CBL_RST	EN_HRD_RST	EN_SOP_DBG2	EN_SOP_DBG1	EN_SOP2	EN_SOP1	EN_SOP
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Reset A	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
EN_CBL_RST	6	Enable Cable Reset detection (MAX25430B only)	0: Cable Reset detection disabled (default) 1: Cable Reset detection enabled
EN_HRD_RST	5	Enable Hard Reset detection (MAX25430B only)	0: Hard Reset detection disabled (default) 1: Hard Reset detection enabled
EN_SOP_DBG2	4	Enable SOP_DBG'' message (MAX25430 only)	0: SOP_DBG'' message detection disabled (default) 1: SOP_DBG'' message detection enabled
EN_SOP_DBG1	3	Enable SOP_DBG' message (MAX25430B only)	0: SOP_DBG' message detection disabled (default) 1: SOP_DBG' message detection enabled
EN_SOP2	2	Enable SOP'' message (MAX25430B only)	0: SOP'' message detection disabled (default) 1: SOP'' message detection enabled

BITFIELD	BITS	DESCRIPTION	DECODE
EN_SOP1	1	Enable SOP' message (MAX25430B only)	0: SOP' message detection disabled (default) 1: SOP' message detection enabled
EN_SOP	0	Enable SOP message (MAX25430B only)	0: SOP message detection disabled (default) 1: SOP message detection enabled

RECEIVE_BUFFER (0x30)

The RECEIVE_BUFFER combines three registers into one:

-READABLE_BYTE_COUNT

-RX_BUF_FRAME_TYPE

-RX_BUF_BYTE_x.

These registers are accessed one after the other by reading successively the RECEIVE_BUFFER. These registers indicate the status of the received SOP* message buffer. These registers shall be read by the TCPM when MAX25430B indicates a SOP* message was received in the Alert Status registers.

The TCPM first reads the RECEIVE_BUFFER which indicates the READABLE_BYTE_COUNT to determine the number of bytes in the RX_BUFFER_BYTE_x. The TCPM then reads again RECEIVE_BUFFER which indicates the RX_BUF_FRAME_TYPE to determine the type of message. The TCPM will then read RECEIVE_BUFFER which indicates the content of the USB PD message in RX_BUF_BYTE_x.

BIT	7	6	5	4	3	2	1	0
Field	RECEIVE_BUFFER[7:0]							
Reset	0x00							
Access Type	Read, Ext							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
RECEIVE_BUFFER	7:0	Receive Buffer (MAX25430B only)	READABLE_BYTE_COUNT[7:0]: Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). RX_BUF_FRAME_TYPE[2:0]: Received SOP* Message 0x00: Received SOP 0x01: Received SOP' 0x02: Received SOP'' 0x03: Received SOP_DBG' 0x04: Received SOP_DBG'' 0x05: Received Cable Reset All others are reserved. RX_BUF_BYTE_x[7:0]: Content of the USB PD message.

TRANSMIT (0x50)

The TCPM writes to this register to transmit a SOP* message where the SOP* message payload (i.e. the header bytes and the data bytes) was written into the TCPC's internal transmit buffer using the TRANSMIT_BUFFER register. The TCPC transmits the aggregate of data written to the TRANSMIT_BUFFER since the pointer was last reset either due to the TCPM writing to the TRANSMIT register or the TCPM writing to COMMAND.ResetTransmitBuffer (0xDD). The entire register shall be written at once and then sent. The TCPC clears the TRANSMIT register

I2C_WRITE_BYTE_COUNT and its internal transmit buffer after executing the transmission regardless of the outcome (either successful, failed or discarded).

BIT	7	6	5	4	3	2	1	0
Field	–	–	*RETRY_COUNTER[1:0]		–	*TX_SOP_MESSAGE[2:0]		
Reset	–	–	0x0		–	0x0		
Access Type	–	–	Write, Read		–	Write, Read		
Reset A	–	–	0x00		–	0x0		

BITFIELD	BITS	DESCRIPTION	DECODE
*RETRY_COUNTER	5:4	Retry Counter (MAX25430B only)	0x0: No message retry is required 0x1: Automatically retry message transmission once 0x2: Automatically retry message transmission twice 0x3: Automatically retry message transmission three times
*TX_SOP_MESSAGE	2:0	Transmit SOP* Message (MAX25430B only)	0x0: Transmit SOP 0x1: Transmit SOP' 0x2: Transmit SOP'' 0x3: Transmit SOP_DBG' 0x4: Transmit SOP_DBG'' 0x5: Transmit Hard Reset 0x6: Transmit Cable Reset 0x7: Transmit BIST Carrier Mode 2

TRANSMIT_BUFFER (0x51)

The TRANSMIT_BUFFER holds the I2C_WRITE_BYTE_COUNT and the portion of the SOP* USB PD message payload (including the header and/or the data bytes) most recently written by the TCPM in TX_BUF_BYTE_x. TX_BUF_BYTE_x is "hidden" and can only be accessed by writing to register address 51h.

The TRANSMIT_BUFFER is capable of holding 30 byte SOP* message. The TCPM can write up to 30 bytes to the TX_BUF_BYTE_x in one burst.

The TCPC automatically increments the TX_BUF_BYTE_x offset as TCPM writes to TX_BUF_BYTE_x. The TCPM can re-write to TX_BUF_BYTE_x beginning at offset 1 by writing to COMMAND.ResetTransmitBuffer.

The TCPM shall write as many bytes in the buffer as defined in the I2C_WRITE_BYTE_COUNT in one I2C write transaction. If the I2C_WRITE_BYTE_COUNT is different than the number of bytes written in the buffer, the TCPC asserts FAULT_STATUS.I2C_ERR and ignores the write (i.e. no change in the TX_BUF_BYTE_x content and the offset).

BIT	7	6	5	4	3	2	1	0
Field	TRANSMIT_BUFFER[7:0]							
Reset	0x00							
Access Type	Write Only							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
TRANSMIT_BUFFER	7:0	Transmit Buffer (MAX25430B only)	I2C_WRITE_BYTE_COUNT[7:0] The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I2C transaction. TX_BUF_BYTE_x[7:0]: Transmit Buffer Bytes.

VBUS_VOLTAGE_L (0x70)

VBUS_VOLTAGE[7:0] - Lower 8-bits

BIT	7	6	5	4	3	2	1	0
Field	VBUS_VOLTAGE[7:0]							
Reset	0x00							
Access Type	Read Only							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_VOLTAGE	7:0	VBUS voltage measurement from 10-bit ADC (Lower 8 bits) (MAX25430B only)	Bits [7:0] of the 10-bit VBUS ADC measurement result with 25mV LSB. Valid when POWER_CONTROL.VBUS_VOLT_MON_EN = 1

VBUS_VOLTAGE_H (0x71)

The TCPM may read this register to determine the measured VBUS voltage. The TCPC maintains synchronization between the upper and lower 8 bits of the register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SCALE_FACTOR[1:0]		VBUS_VOLTAGE[9:8]	
Reset	–	–	–	–	0b00		0b00	
Access Type	–	–	–	–	Read Only		Read Only	
Reset A	–	–	–	–	0b00		0b00	

BITFIELD	BITS	DESCRIPTION	DECODE
SCALE_FACTOR	3:2	Scale Factor (MAX25430B only)	00: VBUS measurement not scaled
VBUS_VOLTAGE	1:0	VBUS voltage measurement from 10-bit ADC (Upper 2 bits) (MAX25430B only)	Bits [9:8] of the 10-bit VBUS ADC measurement result with 25mV LSB. Valid when POWER_CONTROL.VBUS_VOLT_MON_EN = 1.

VBUS_STOP_DISCHARGE_THRESHOLD_L (0x74)

Lower 8 bits of the 10-bit VBUS_STOP_DISCHARGE_THRESHOLD register.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_STOP_DISCH_THRESHOLD[7:0]							
Reset	0x20							
Access Type	Write, Read							
Reset A	0x20							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_STOP_DISCH_THRESHOLD	7:0	VBUS Stop Discharge Threshold (Lower 8 bits)	Bits [7:0] of the 10-bit VBUS Stop Discharge Threshold. 0x000 to 0x020: 0.8V (Default) 0x021 to 0x3FF: (Value * 0.1V)/4 Bit 1 and Bit 0 are always ignored. Bit 2 is the LSB and equals to 100mV. Examples: 0x000 = 0.8V 0x021 = 0.9V 0x022 = 1.0V

VBUS_STOP_DISCHARGE_THRESHOLD_H (0x75)

Upper 2 bits of the 10-bit VBUS_STOP_DISCHARGE_THRESHOLD register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VBUS_STOP_DISCH_THRESHOLD[9:8]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	
Reset A	–	–	–	–	–	–	0b00	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_STOP_DISCH_THRESHOLD	1:0	VBUS Stop Discharge Threshold (Upper 2 bits)	Bits [9:8] of the 10-bit VBUS Stop Discharge Threshold

VBUS_VOLTAGE_ALARM_HI_CFG_L (0x76)

Lower 8 bits of the 10-bit VBUS_ALARM_HI_CFG register.

BIT	7	6	5	4	3	2	1	0
Field	VBUS_ALARM_HI_CFG[7:0]							
Reset	0x00							
Access Type	Write, Read							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_HI_CFG	7:0	VBUS Alarm High Voltage trip point (Lower 8 bits)	Bits [7:0] of the 10-bit VBUS Alarm High Voltage threshold with 25mV LSB

VBUS_VOLTAGE_ALARM_HI_CFG_H (0x77)

Upper 2 bits of the 10-bit VBUS_ALARM_HI_CFG register. This registers define the level triggered alarm thresholds.

The TCPM writes to VBUS_VOLTAGE_ALARM_HI_CFG to set the high voltage alarm level. The TCPC sets ALERT_L.VBUS_ALARM_HI to logic '1' when VBUS drops below the high voltage alarm level.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VBUS_ALARM_HI_CFG[9:8]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	
Reset A	–	–	–	–	–	–	0b00	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_HI_CFG	1:0	VBUS Alarm High Voltage trip point (Upper 2 bits)	Bits [9:8] of the 10-bit VBUS Alarm High Voltage threshold with 25mV LSB

VBUS_VOLTAGE_ALARM_LO_CFG_L (0x78)

Lower 8 bits of the 10-bit VBUS_ALARM_LO_CFG register.

BIT	7	6	5	4	3	2	1	0
Field	*VBUS_ALARM_LO_CFG[7:0]							
Reset	0x00							
Access Type	Write, Read							
Reset A	0x00							

BITFIELD	BITS	DESCRIPTION	DECODE
*VBUS_ALARM_LO_CFG	7:0	VBUS Low Voltage trip point (Lower 8 bits)	Bits [7:0] of the 10-bit VBUS Alarm Low Voltage threshold with 25mV LSB

VBUS_VOLTAGE_ALARM_LO_CFG_H (0x79)

Upper 2 bits of the 10-bit VBUS_ALARM_LO_CFG register. This registers define the level triggered alarm thresholds.

The TCPM writes to VBUS_VOLTAGE_ALARM_LO_CFG to set the low voltage alarm level. The TCPC sets ALERT_H.VBUS_ALARM_LO to logic '1' when VBUS drops below the low voltage alarm level.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	VBUS_ALARM_LO_CFG[9:8]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	
Reset A	–	–	–	–	–	–	0b00	

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ALARM_LO_CFG	1:0	VBUS Alarm Low Voltage trip point (Upper 2 bits)	Bits [9:8] of the 10-bit VBUS Alarm Low Voltage threshold with 25mV LSB

PWR_OUT_CONTROL (0x80)

BIT	7	6	5	4	3	2	1	0
Field	–	–	VOUT_ILIM[1:0]		–	–	VOUT_SEL[1:0]	
Reset	–	–	0x0		–	–	0x0	
Access Type	–	–	Write, Read		–	–	Write, Read	
Reset A	–	–	0x0		–	–	0x0	

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT_ILIM	5:4	VBUS Overcurrent Threshold (VBUS ILIM)	0x0: 3A (default) 0x1: 4A 0x2 and 0x3: 6A
VOUT_SEL	1:0	VBUS Output Voltage Selection	0x0: 5V (default) 0x1: 9V 0x2: 15V 0x3: 20V

CABLE_COMP_CONTROL (0x81)

BIT	7	6	5	4	3	2	1	0
Field	–	–	GAIN[5:0]					
Reset	–	–	0x00					
Access Type	–	–	Write, Read					
Reset A	–	–	0x00					

BITFIELD	BITS	DESCRIPTION	DECODE
GAIN	5:0	Cable Compensation Gain	Multiply the decimal value by 8 to get the gain in mΩ. Maximum Gain = 0x3F = 0d63.

RESERVED (0x82)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RESERVED
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Reset A	–	–	–	–	–	–	–	0b0

BITFIELD	BITS	DESCRIPTION
RESERVED	0	Reserved

BUCK_BOOST_SETUP (0x83)

BIT	7	6	5	4	3	2	1	0
Field	SLP[2:0]			FSW[1:0]		SYNC_DIR	SS_SEL[1:0]	
Reset	0b011			0b10		0b1	0b00	
Access Type	Write, Read			Write, Read		Write, Read	Write, Read	
Reset A	0b011			0b10		0b1	0b00	

BITFIELD	BITS	DESCRIPTION	DECODE
SLP	7:5	Slope Compensation Peak Ramp Voltage	000: 100 mV 001: 200 mV 010: 300 mV 011: 400 mV (Default) 100: 500 mV 101: 600 mV 110: 700 mV 111: 800 mV
FSW	4:3	DC/DC Convertor Switching Frequency	00: 220 kHz 01: 300 kHz 10: 400 kHz (default) 11: Reserved
SYNC_DIR	2	SYNC Pin Direction	0: Output 1: Input (default)
SS_SEL	1:0	Spread Spectrum Selection	00: Disabled (default) 01: +/- 3% Spread Spectrum 10: +/- 6% Spread Spectrum 11: +/- 9% Spread Spectrum

WATCHDOG_SETUP (0x84)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	WD_TIMEOUT[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	
Reset A	–	–	–	–	–	–	0b00	

BITFIELD	BITS	DESCRIPTION	DECODE
WD_TIMEOUT	1:0	Watchdog Timer Timeout Value	00: 1 second (default) 01: 2 seconds 10: 4 seconds 11: 5 seconds

AUTO_SHIELD_SETUP (0x85)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	RETRY_TMR[1:0]	
Reset	–	–	–	–	–	–	0b11	
Access Type	–	–	–	–	–	–	Write, Read	
Reset A	–	–	–	–	–	–	0b11	

BITFIELD	BITS	DESCRIPTION	DECODE
RETRY_TMR	1:0	Retry Timer Value	00 = 2.0s 01 = 1.0s 10 = 0.5s 11 = 16ms (default) Determines the length of the RETRY timer after a fault condition

AUTO_CDP_DCP_SETUP (0x86)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AUTO_CDP_DCP_MODE[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	
Reset A	–	–	–	–	–	–	0b00	

BITFIELD	BITS	DESCRIPTION	DECODE
AUTO_CDP_DCP_MODE	1:0	BC1.2 Charge Detection Mode Selection	00: High Speed Pass Through (default) 01: Auto-CDP 10: Auto-DCP / Apple 2.4A 11: Auto-DCP / Apple 1.0A

IN_THRESH (0x87)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	IN_UV_THRESH[3:0]			
Reset	–	–	–	–	0x7			
Access Type	–	–	–	–	Write, Read			
Reset A	–	–	–	–	0x7			

BITFIELD	BITS	DESCRIPTION	DECODE
IN_UV_THRESH	3:0	Input Supply (V_{IN}) Undervoltage Threshold	0x0 : 4.5 V 0x1 : 4.9 V 0x2 : 5.3 V 0x3 : 5.7 V 0x4 : 6.1 V 0x5: 6.5 V 0x6: 6.9 V 0x7: 7.3 V (Default) 0x8: 7.7 V 0x9: 8.1 V 0xA: 8.5 V 0xB : Reserved 0xC : Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

VCONN_THRESH (0x88)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	VCONN_OCP_SEL	–	VCONN_IN_UV_THRESH[2:0]		
Reset	–	–	–	0x0	–	0x7		
Access Type	–	–	–	Write, Read	–	Write, Read		
Reset A	–	–	–	0x0	–	0x7		

BITFIELD	BITS	DESCRIPTION	DECODE
VCONN_OCP_SEL	4	VCONN Overcurrent Threshold Low	0: $I_{VCONN\_OCP\_L1}$ = 250 mA typ. (default) 1: $I_{VCONN\_OCP\_L2}$ = 360 mA typ.
VCONN_IN_UV_THRESH	2:0	VCONN Undervoltage Threshold	0x0: 2.75V 0x1: 2.85V 0x2: 2.95V 0x3: 3.05V 0x4: 4.35V 0x5: 4.45V 0x6: 4.55V 0x7: 4.65V (default)

VBUS_THRESH (0x89)

BIT	7	6	5	4	3	2	1	0
Field	–	VBUS_OV_THRESH[2:0]			–	VBUS_UV_THRESH[2:0]		
Reset	–	0x3			–	0x3		
Access Type	–	Write, Read			–	Write, Read		
Reset A	–	0x3			–	0x3		

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_OV_THRESH	6:4	VBUS Overvoltage Fault Threshold	0x0: +8.75% 0x1: +10.00% 0x2: +11.25% 0x3: +12.50% (default) 0x4: +13.75% 0x5: +15.00% 0x6: +16.25% 0x7: +17.50%
VBUS_UV_THRESH	2:0	VBUS Undervoltage Fault Threshold	0x0: -8.75% 0x1: -10.00% 0x2: -11.25% 0x3: -12.50% (default) 0x4: -13.75% 0x5: -15.00% 0x6: -16.25% 0x7: -17.50%

AUTO_SHIELD_STATUS_MASK (0x8A)

A Read-Write register that configures which of the conditions in the AUTO_SHIELD_STATUS register will assert VNDR_ALRT.

BIT	7	6	5	4	3	2	1	0
Field	SHIELDING_MASK	–	–	–	VCONN_IN_UV_MASK	IN_OC_MASK	VDD_USB_UV_MASK	VBUS_UV_MASK
Reset	0b1	–	–	–	0b0	0b0	0b0	0b0
Access Type	Write, Read	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read
Reset A	0b1	–	–	–	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
SHIELDING_MASK	7	Shielding Mask	0: Not included in VNDR_ALRT 1: Included in VNDR_ALRT (default)

BITFIELD	BITS	DESCRIPTION	DECODE
VCONN_IN_UV_MASK	3	VCONN Undervoltage Mask	0: Not included in VNDR_ALRT (default) 1: Included in VNDR_ALRT
IN_OC_MASK	2	Input Supply Overcurrent Mask	0: Not included in VNDR_ALRT (default) 1: Included in VNDR_ALRT
VDD_USB_UV_MASK	1	VDD_USB Undervoltage Mask	0: Not included in VNDR_ALRT (default) 1: Included in VNDR_ALRT
VBUS_UV_MASK	0	VBUS Undervoltage Mask	0: Not included in VNDR_ALRT (default) 1: Included in VNDR_ALRT

AUTO_SHIELD_STATUS (0x8B)

A read only register that indicates a number of status conditions. Each individual status bit can assert an interrupt via VNDR_ALRT by setting the corresponding bit in the AUTO_SHIELD_STATUS_MASK register. The VNDR_ALRT is asserted on the rising-edge of the SHIELDING status (when included), and on any change for any other status (VCONN_IN_UV, IN_OC, VDD_USB_UV, and VBUS_UV).

BIT	7	6	5	4	3	2	1	0
Field	SHIELDING	–	–	–	VCONN_IN_UV	IN_OC	VDD_USB_UV	VBUS_UV
Reset	0b0	–	–	–	0b0	0b0	0b0	0b0
Access Type	Read Only	–	–	–	Read Only	Read Only	Read Only	Read Only
Reset A	0b0	–	–	–	0b0	0b0	0b0	0b0

BITFIELD	BITS	DESCRIPTION	DECODE
SHIELDING	7	Shielding Status	0: No Fault 1: Fault detected Refer to Fault Table.
VCONN_IN_UV	3	VCONN Undervoltage Fault	0: No Fault 1: Undervoltage detected
IN_OC	2	Buck-Boost Input Overcurrent Fault	0: No Fault 1: Overcurrent detected
VDD_USB_UV	1	VDD_USB Undervoltage Fault	0: No Fault 1: Undervoltage detected
VBUS_UV	0	VBUS Undervoltage Fault	0: No Fault 1: Undervoltage detected

Applications Information

TCPC Functionality (MAX25430B only)

The MAX25430B devices incorporate a USB-IF compliant CC PHY capable of encoding/decoding Bi-phase Mark Coded (BMC) messages. Cyclic Redundancy Checking (CRC) is automatically appended to all outgoing messages and checked on all incoming messages.

The MAX25430B's TCPC hardware permits the simple integration with an external MCU, running a TCPM stack, to create a complete USB Type-C Power Delivery Source.

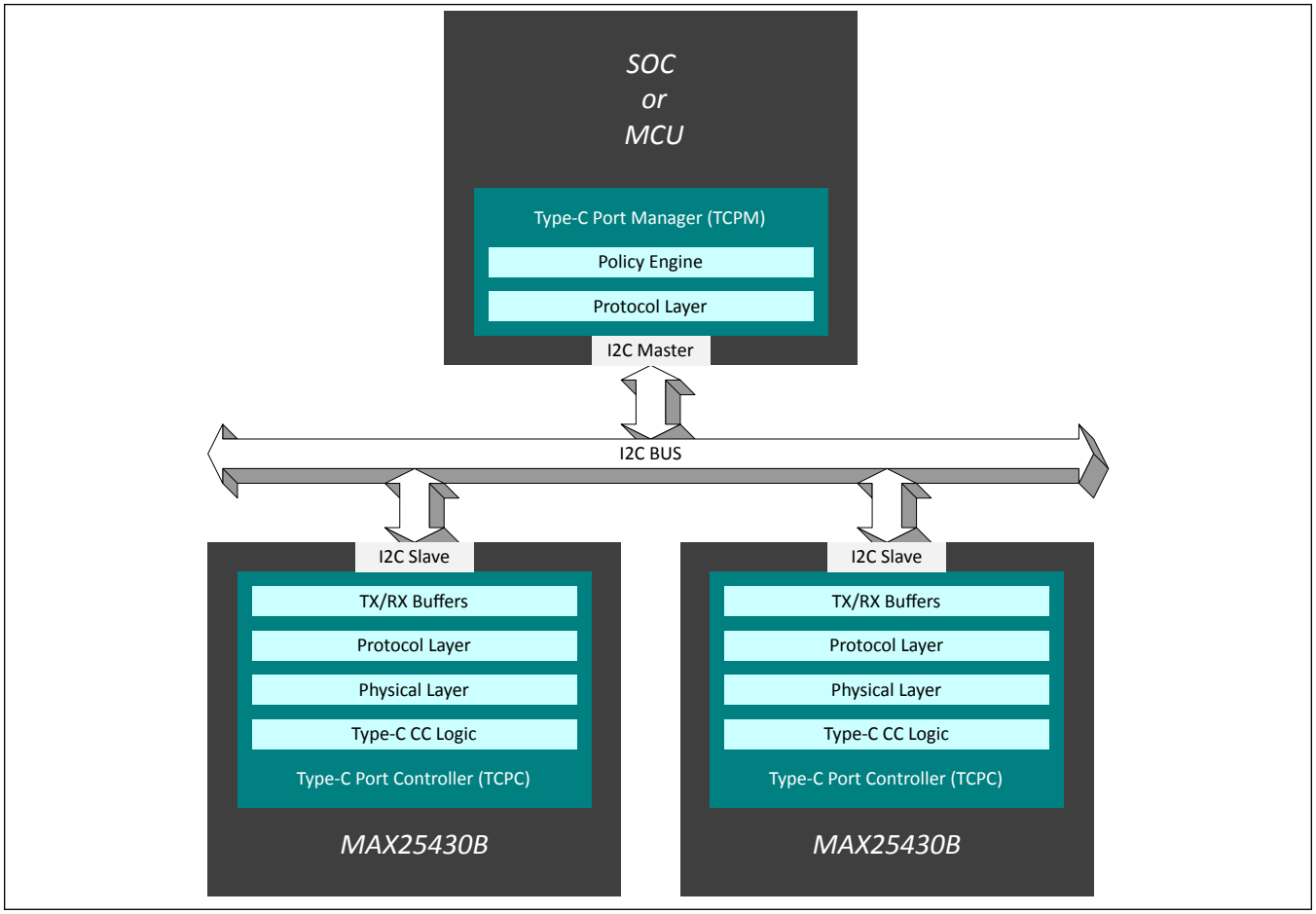


Figure 25. TCPM to TCPC Interface through I2C

Receiving USB-PD messages

The MAX25430B TCPC logic facilitates the reception and decoding of USB-PD messages, by incorporating a Type-C Physical Interface (PHY), and I2C accessible registers. The TCPM need only respond to interrupts, due to changes in status, and then reading from or writing to the appropriate register. The generation and decoding of PD Cyclic-Redundancy-Checking bits is automatically handled by the TCPC logic. Upon receiving a valid USB-PD message, the MAX25430 TCPC logic will assert the $\overline{\text{ALERT}}$ pin low to indicate a change in status. Changes in status are latched in the ALERT_L and ALERT_H registers located at addresses 0x10 and 0x11 respectively. The TCPM must read the ALERT_L

and ALERT_H registers to determine the type of status change.

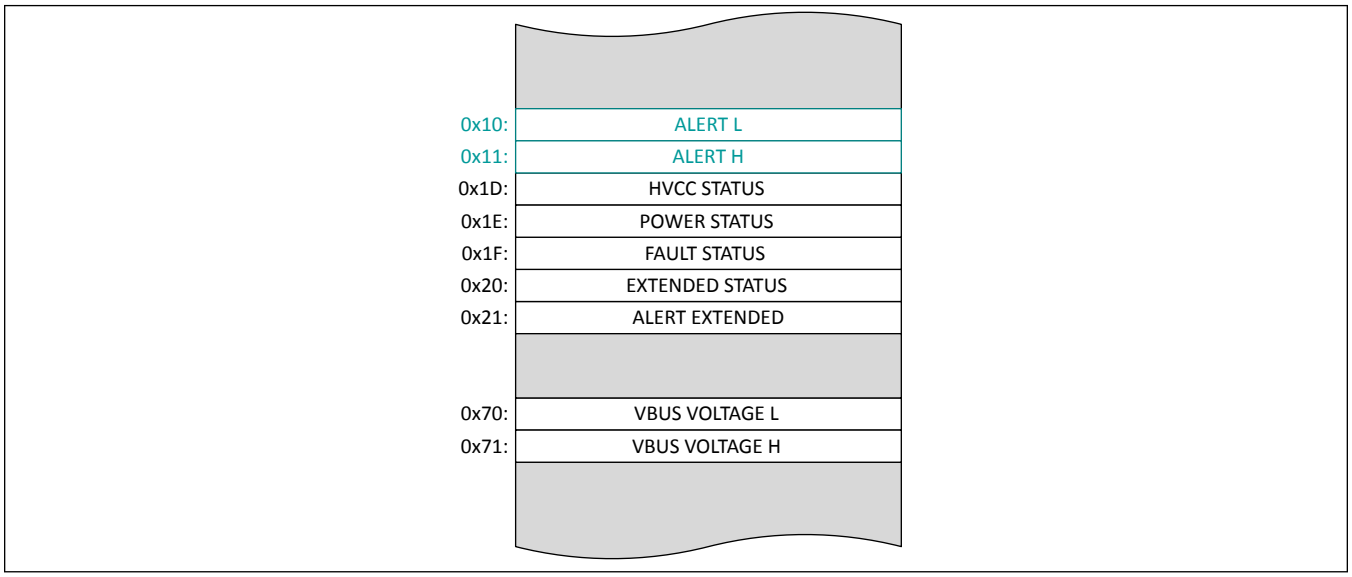


Figure 26. Status Registers

For example, the TCPM detects that the MAX25430 $\overline{ALERT}$ pin has been asserted low. The TCPM would then perform an I²C Read Word transaction on the ALERT_L and ALERT_H registers.

I²C Read Word from Register 0x10:

0x04, 0x00

Table 11. Reading the RX SOP MESSAGE

REGISTER	ADDRESS	D7	D6	D5	D4	D3	**D2**	D1	D0
ALERT_L	0x10	VBUS V ALARM HIGH	TX SOP MESSAGE SUCCESS	TX SOP MESSAGE DISCARD	TX SOP MESSAGE FAIL	RX HARD RESET	**RX SOP MESSAGE**	POWER STATUS	HVCC STATUS
		0	0	0	0	0	**1**	0	0
ALERT_H	0x11	VENDOR ALERT	ALERT EXTENDED	EXTEND STATUS	BEGIN SOP MESSAGE STATUS	VBUS SINK DISCHAR DETECT	RX BUFFER OVRFL	FAULT STATUS	VBUS VOLT ALARM LOW
		0	0	0	0	0	0	0	0

Bit D2 in ALERT_L is set, indicating that a message has been received in the RX BUFFER.

Next, the message must be extracted from the MAX25430 RX_BUFFER and decoded.

The message content is stored in the RX_BUFFER, 32 contiguous bytes starting at address 0x30. The RX_BUFFER must be read with an I²C Read Block transaction (Refer to *I2C Interface*), or the TCPC logic will generate an I²C error.

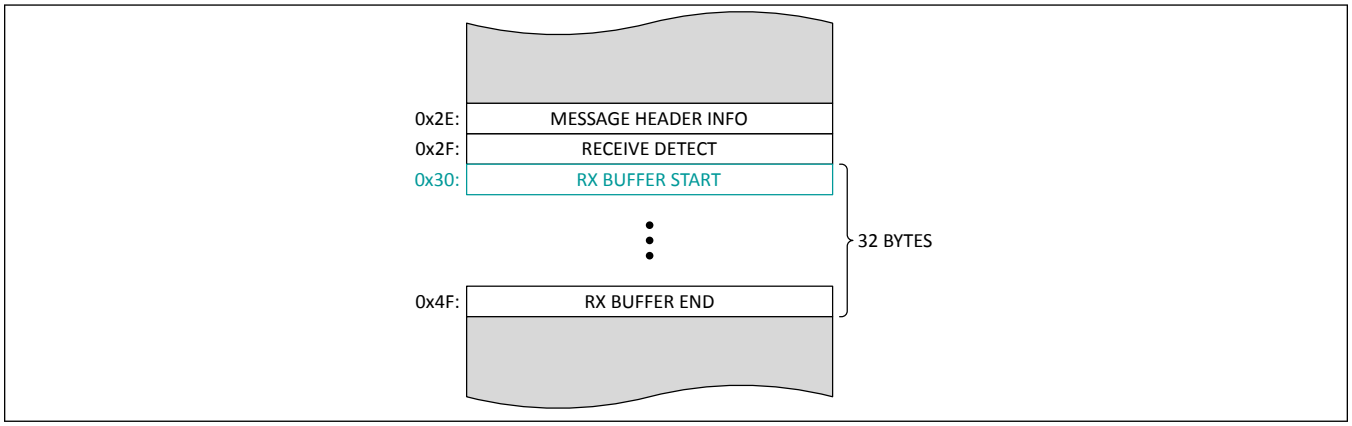


Figure 27. Receive Buffer

Continuing with the example, the message data is extracted from the RX_BUFFER, as seen below.

I²C Read Block from Registers 0x30 – 0x4F:

0x03, 0x00, 0x47, 0x0C, 0x16, 0x87, 0x57, 0xF7, 0xEF, 0xD6,

0x2C, 0x40, 0x26, 0x28, 0x03, 0x9B, 0x00, 0x00, 0x00, 0x00,

0x44, 0xD3, 0x15, 0xEA, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,

0x00, 0x00

Since we cannot know how many relevant bytes are in the message before the I²C transaction, all the bytes in the RX BUFFER are read. The first byte indicates that there are three bytes significant to this message. The second byte is the SOP message type, the third and fourth bytes form the message header 0x0C47.

Note: the TCPC does not erase previous information from the buffer and therefore the TCPM must parse the relevant bytes to decode the message.

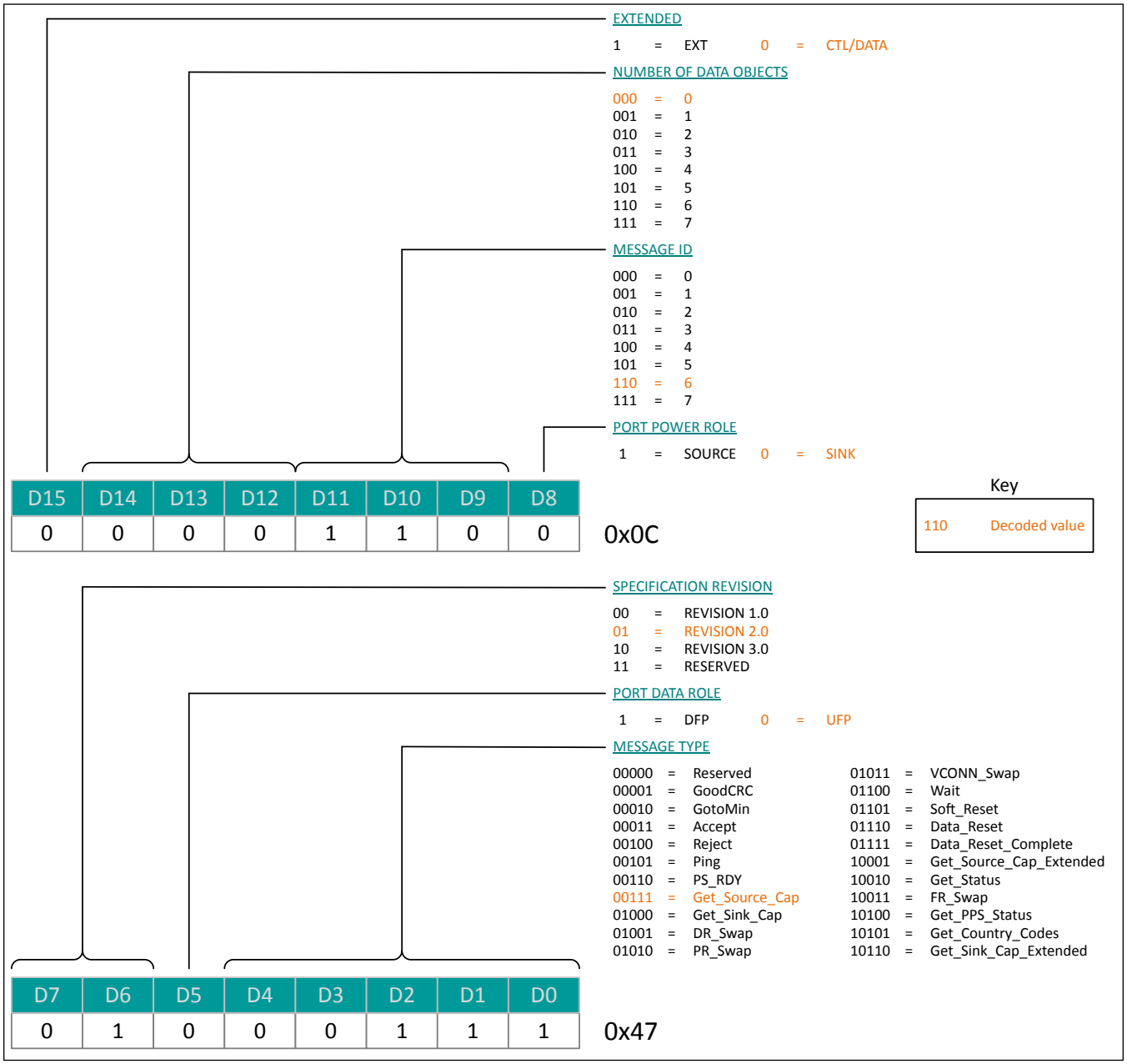


Figure 28. Message Header - "Get_Source_cap"

Decoding the header word indicates the PD Sink is requesting that the Source Capabilities be sent.

Now that the message has been decoded, the $\overline{\text{ALERT}}$ pin interrupt can be cleared, so that MAX25430B TCPC State Machine can continue to service PD messages.

Table 12. Writing 1 to Clear the RX SOP MESSAGE

REGISTER	ADDRESS	D7	D6	D5	D4	D3	**D2**	D1	D0

Table 12. Writing 1 to Clear the RX SOP MESSAGE (continued)

ALERT_L	0x10	V_{BUS} V ALARM HIGH	TX SOP MESSAGE SUCCESS	TX SOP MESSAGE DISCARD	TX SOP MESSAGE FAIL	RX HARD RESET	**RX SOP MESSAGE**	POWER STATUS	HVCC STATUS
		0	0	0	0	0	**1**	0	0
ALERT_H	0x11	VENDOR ALERT	ALERT EXTENDED	EXTEND STATUS	BEGIN SOP MESSAGE STATUS	V_{BUS} SINK DISCHAR DETECT	RX BUFFER OVRFL	FAULT STATUS	V_{BUS} VOLT ALARM LOW
		0	0	0	0	0	0	0	0

I2C Write Word to Register 0x10:

0x04, 0x00

The TCPM clears the ALERT_L register by writing a logic '1' to bit D2. $\overline{ALERT}$ returns high.

Sending USB-PD messages

The MAX25430B TCPC logic simplifies the TCPM code required to transmit USB-PD messages. Sending PD messages is a two-stage process, employing the TX_BUFFER (31 contiguous byte-wide registers), and the TRANSMIT Register.

First, the TX_BUFFER is loaded with an encoded PD message (Control or Data), and then a command byte is written the TRANSMIT Register (0x50) to trigger the MAX25430 TCPC transmit process.

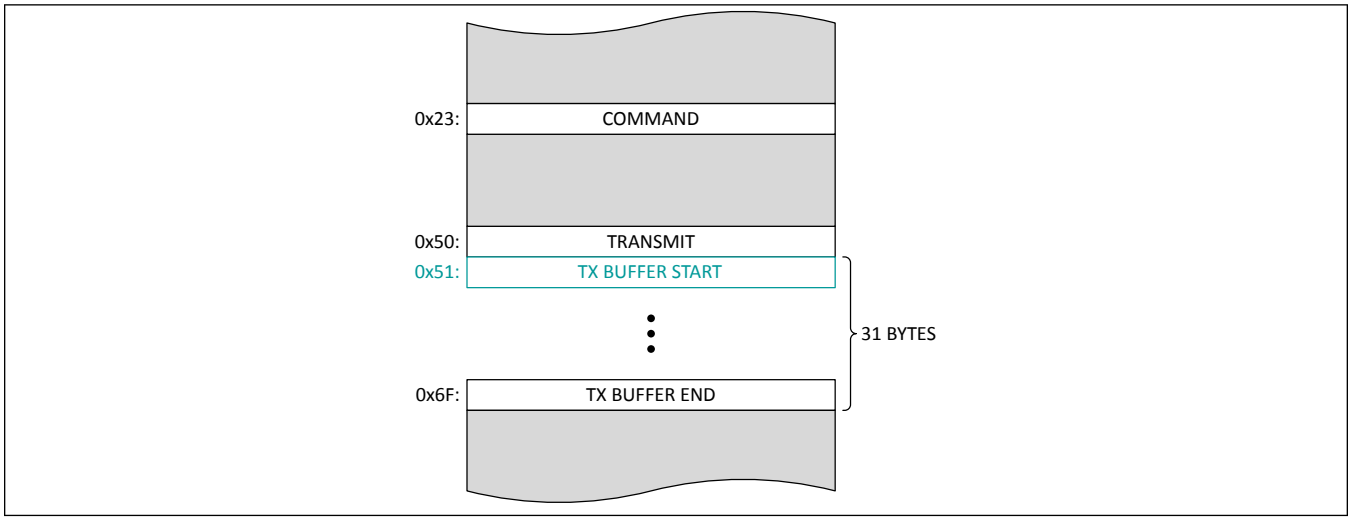


Figure 29. Transmit Buffer

The PD message contents must be written to TX_BUFFER in a single I2C transaction, therefore an I2C Write Block transaction (Refer to *I2C Interface*) should be used, or the TCPC logic will generate an I2C error and the message will not be sent.

To illustrate the proper TCPM coding approach, let's continue with the MAX25430B's response to the PD Sink's Get Source Capabilities example.

The TCPM needs to encode and load the requested Source Capabilities message, Header plus Data Objects, into the TX BUFFER.

Number of bytes: 0x12 (18 bytes)

Message Header: 0x4361 (Source Capabilities with 4 data objects) = 2 bytes

Data Object 1: 0x000190F0 (5.00V @2.4A) = 4 bytes
Data Object 2: 0x0002D12C (9.00V @3A) = 4 bytes
Data Object 3: 0x0004B12C (15.00V @3A) = 4 bytes
Data Object 4: 0x0006412C (20.00V @3A) = 4 bytes

The figures below show the corresponding Message Header and Data Object 1 decoding.

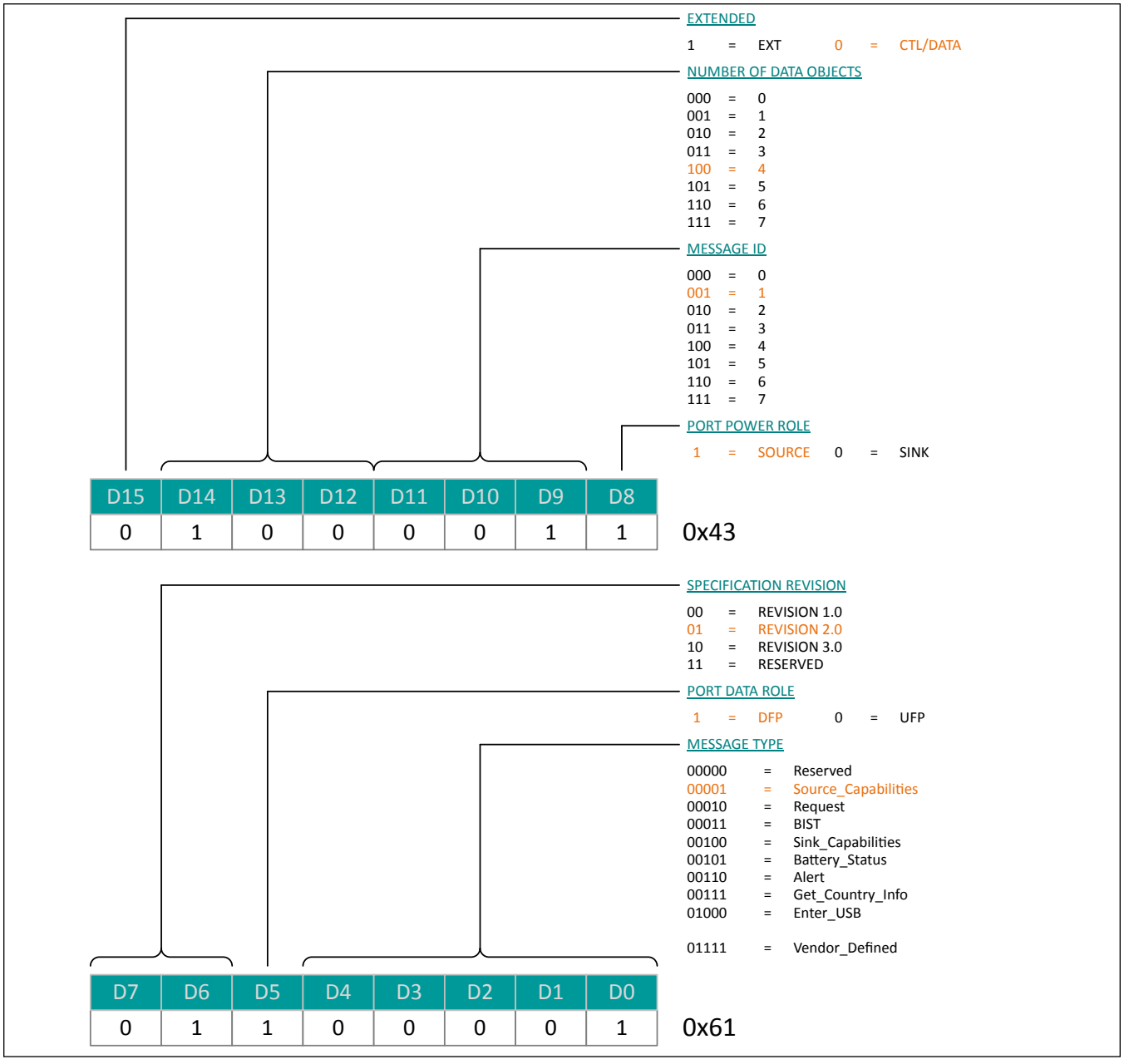


Figure 30. Message Header - "Source_Capabilities"

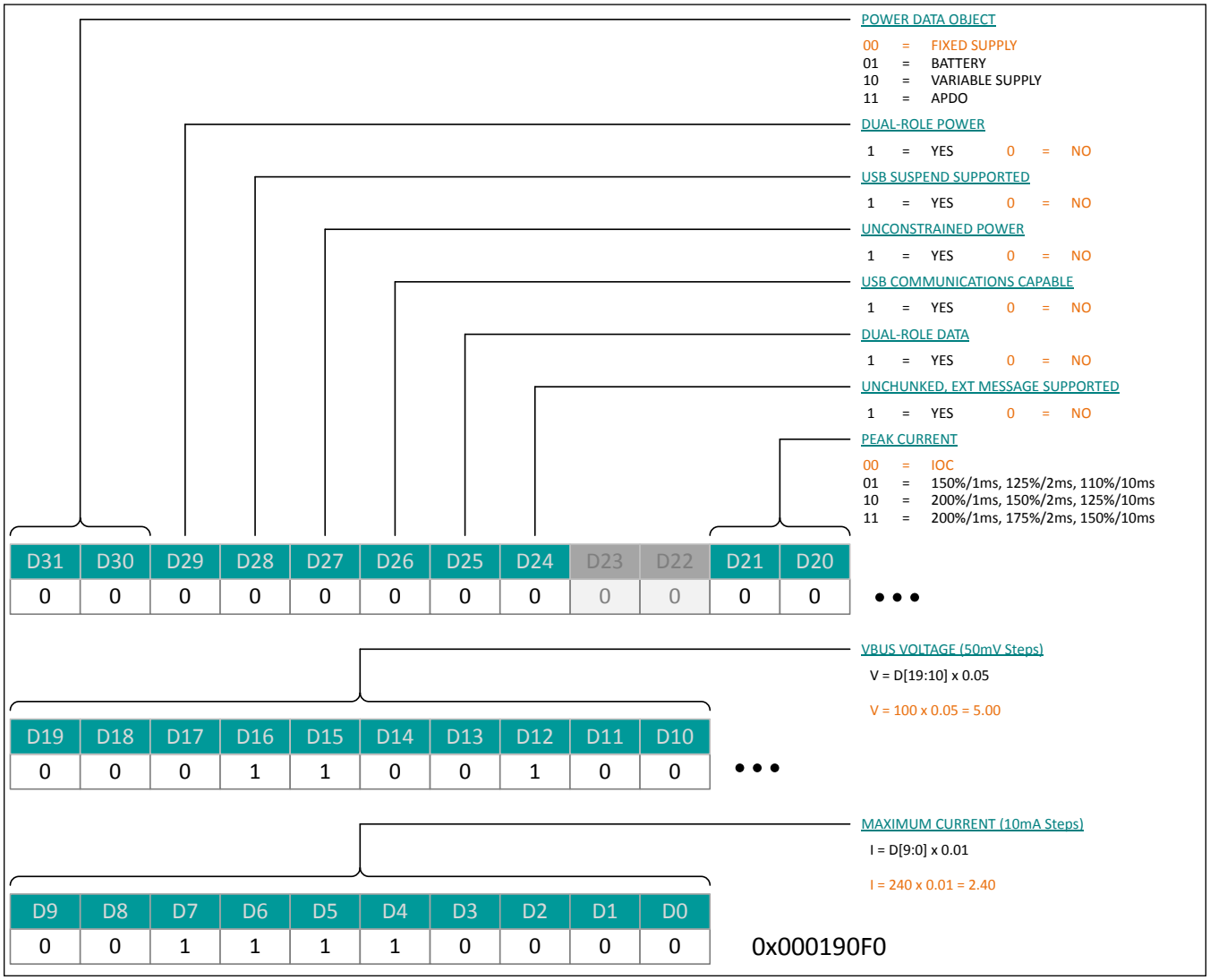


Figure 31. Data Object 1 - 5V/2.4A Fixed PDO

The assembled message packet is then loaded into the TX_BUFFER.

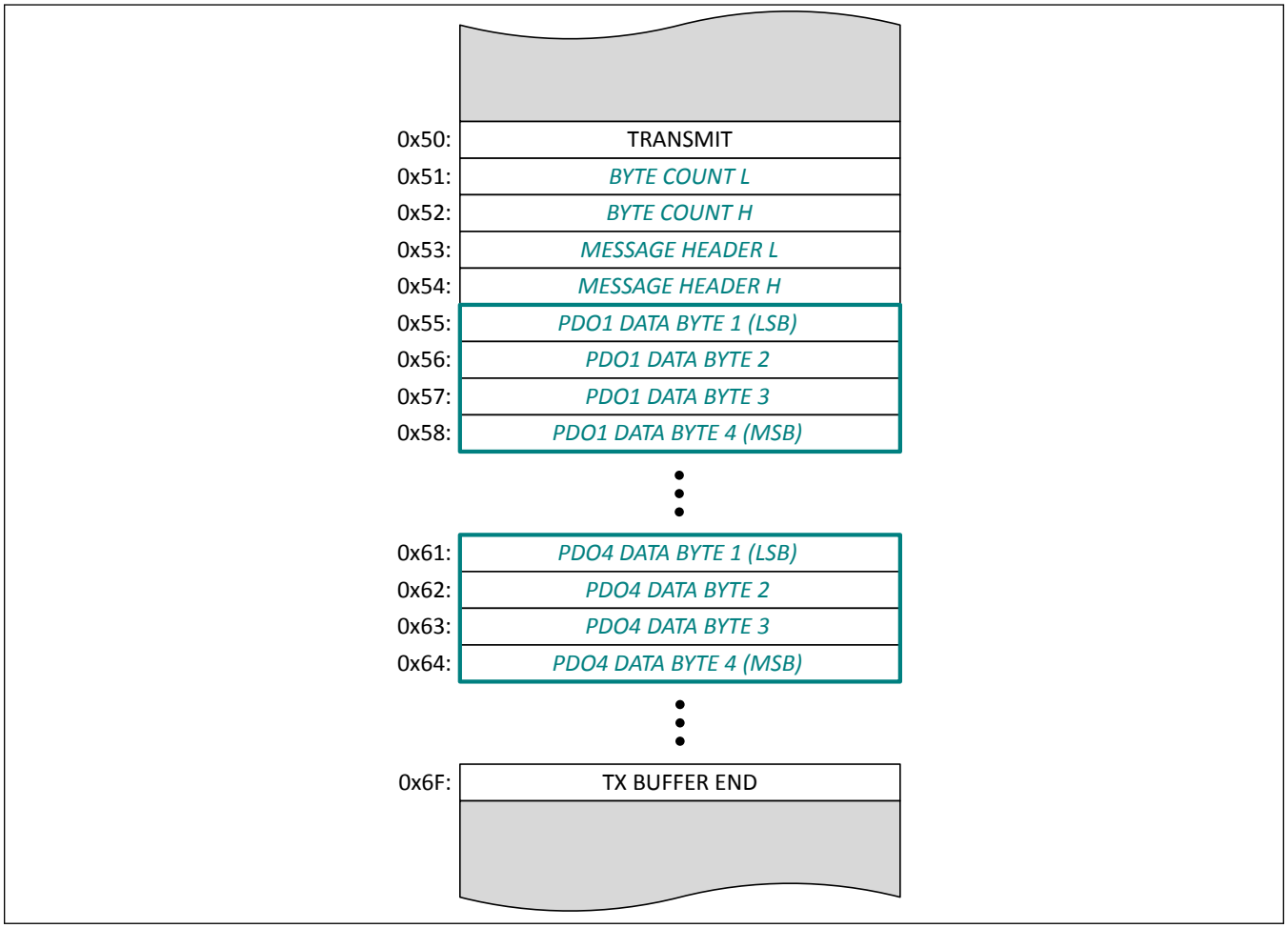


Figure 32. Transmit Buffer - "Source_Capabilities"

I2C Write Block to TX BUFFER 0x51:

0x12, 0x61, 0x43, 0xF0, 0x90, 0x01, 0x00, 0x2C, 0xD1, 0x02,

0x00, 0x2C, 0xB1, 0x04, 0x00, 0x2C, 0x41, 0x06, 0x00

Finally, the message is released to the MAX25430B's TCPC logic by writing 0x30 to the TRANSMIT Register. Then the entire packet will be appended with the proper CRC, BMC encoded, and transmitted via the corresponding HVCC pin.

I2C Write Byte to TRANSMIT 0x50:

0x30

The MAX25430B's TCPC logic will now assert $\overline{\text{ALERT}}$ low and update the ALERT_L register with the message status. The TCPM must service this interrupt to ensure that MAX25430B's TCPC logic can continue to handle USB-PD messages.

I2C Read Word from Register 0x10:

0x40, 0x00

REGISTER	ADDRESS	D7	**D6**	D5	D4	D3	D2	D1	D0

ALERT_L	0x10	V_{BUS} V ALARM HIGH	**TX SOP MESSAGE SUCCESS**	TX SOP MESSAGE DISCARD	TX SOP MESSAGE FAIL	RX HARD RESET	RX SOP MESSAGE	POWER STATUS	HVCC STATUS
		0	**1**	0	0	0	0	0	0
ALERT_H	0x11	VENDOR ALERT	ALERT EXTENDED	EXTEND STATUS	BEGIN SOP MESSAGE STATUS	V_{BUS} SINK DISCHAR DETECT	RX BUFFER OVRFL	FAULT STATUS	V_{BUS} VOLT ALARM LOW
		0	0	0	0	0	0	0	0

The TCPM reads the ALERT_L and ALERT_H registers and sees that bit D6 is set in ALERT_L, indicating that the previously sent message was successful.

Lastly, the TX_SOP_MESSAGE_SUCCESS bit in the ALERT_L register needs to be cleared by the TCPM. This is done by writing logic '1' to bit D6.

I^2C Write Word to Register 0x10:

0x40, 0x00

Additional Resources

Contact Maxim Integrated for more information on how to program the TCPM.

Buck-Boost Component Selection

Inductor Selection

Design of inductor is a compromise between the size, efficiency, control bandwidth, and stability of the converter. For a buck-boost application, selecting the right value of inductor becomes even more critical due to the presence of right-half-plane (RHP) zero in boost and buck-boost mode. A bigger inductance value would reduce RMS current loss in MOSFETs and core/winding losses in the inductor. On the other hand, it slows the control loop and reduces the frequency of the RHP zero that can cause stability concerns.

Start the inductor selection based on the inductor current ripple as a percentage of the maximum inductor current in buck mode using the equations below. Choose the highest inductance between LBUCK and LBOOST. Minimum duty cycle in buck or boost will yield the highest inductor current ripple.

$$L_{BUCK} > \frac{\left(V_{IN\_MAX} - V_{OUT\_MIN}\right) \cdot D_{BUCK\_MIN}}{f_{SW} \cdot \Delta I_L} \text{ (eq. 1)}$$

$$L_{BOOST} > \frac{V_{IN\_MIN} \cdot D_{BOOST\_MAX}}{f_{SW} \cdot \Delta I_L \cdot V_{IN\_MIN}} \text{ (eq. 2)}$$

$$\Delta I_L = I_{OUT\_MAX} \cdot LIR \text{ (eq. 3)}$$

$$D_{BUCK\_MIN} = \frac{V_{OUT\_MIN}}{V_{IN\_MAX} \cdot \eta_{BUCK}} \text{ (eq. 4)}$$

$$D_{BOOST\_MAX} = 1 - \frac{V_{IN\_MIN} \cdot \eta_{BOOST}}{V_{OUT\_MAX}} \text{ (eq. 5)}$$

L_{BUCK}, L_{BOOST} : minimum inductance needed in buck mode and boost mode, respectively, in H.

f_{SW}: switching frequency in Hz.

V_{IN_MIN} , V_{IN_MAX} : minimum and maximum voltage seen at the power stage input, respectively.

I_{OUT_MAX} : maximum DC output current supported in the application.

LIR : desired peak-to-peak inductor current ripple ratio. Ratio of Δ_{IL}/I_{OUT_MAX}.

D_{BUCK_MIN}, D_{BOOST_MAX} : minimum and maximum duty cycle in Buck and Boost mode, respectively.

η_{BUCK}, η_{BOOST} : efficiency at maximum load in buck mode and boost mode, respectively.

V_{OUT_MIN} : lowest output voltage seen in the application. For fixed PDO applications, use 5.15V (Vsafe5V).

V_{OUT_MAX} : highest output voltage seen in the application. 5.15V, 9V, 15V or 20V for fixed PDOs applications.

Select the final value of inductance considering the ripple in both regions of operation, inductor derating and RHP zero. Once the final value of inductance is selected, calculate the peak inductor current and choose an inductor with saturation current approximately 20% more than the peak inductor current. Low DCR helps achieve higher efficiency by reducing inductor conduction loss during high output power with low input voltage.

Example

P_{OUT_MAX} = 100W ; V_{IN_MIN} = 6V ; V_{IN_MAX} = 18V ; V_{OUT_MIN} = 5.15V ; V_{OUT_MAX} = 20V ; f_{SW} = 400kHz ; I_{OUT_MAX} =5A ; η_{BUCK} = η_{BOOST} = 95% ; LIR is chosen to be 55% to keep the inductor small.

For this example, L_{BUCK} > 3.5 uH and L_{BOOST} > 3.9 uH. Therefore, an inductor with a value of 4.7µH will be selected.

Inductor saturation current must be considered when choosing the inductor.

The high input current seen during low V_{IN}/High P_{OUT} conditions has an impact on the current saturation rating of the inductor and therefore its size. MAX25430 advantage is its flexibility with regards to output power thanks to its scalable peak input current limit. When selecting the input current sense resistor value (R_{CS1}), consider the output power, inductor saturation current, minimum input voltage seen at the power stage but also the minimum V_{BUS} voltage to meet at the user port. When the peak input current reaches the I_{OC1} threshold defined by R_{CS1}, the controller will automatically enter

cycle-by-cycle input current limit which may cause V_{BUS} to droop below the minimum specification at the port. Cable compensation will not increase V_{BUS} in this condition as the input current (and therefore the input power) is limited.

Once the input sense resistor value is selected, the inductor saturation current rating (I_{SAT}) value can be chosen. The I_{SAT} value must be higher than the input peak I_{LIM} threshold by some safe margin to avoid saturating the core.

$$I_{SAT} > I_{OC1\_MAX}$$

$$I_{SAT} > \frac{V_{OC1\_MAX}}{R_{CS1}}$$

Example

R_{CS1} = 3mΩ and V_{OC1_MAX} = 60mV yields I_{OC1_MAX} = 20A, therefore:

$$I_{SAT} > 20A$$

Input Capacitor Design

The input capacitor reduces peak currents drawn from the power source and minimizes noise and voltage ripple on the input caused by the circuit switching. In buck mode, input current is discontinuous with maximum ripple. The RMS current is shown in the following equation:

$$I_{RMS} = \frac{I_{OUT\_MAX} \cdot \sqrt{V_{OUT} \cdot \left(V_{IN} - V_{OUT}\right)}}{V_{IN}} \text{ (eq. 6)}$$

The maximum input RMS current occurs at V_{IN} = 2 x V_{OUT}. Substituting V_{IN} previously, the equation then becomes:

$$I_{RMS\_MAX} = \frac{I_{OUT\_MAX}}{2} \text{ (eq. 7)}$$

The input voltage ripple in buck mode is given by:

$$\Delta V_{IN} = \frac{\left(1 - D_{BUCK}\right) \cdot I_{OUT} \cdot D_{BUCK}}{f_{SW} \cdot C_{IN}} \text{ (eq. 8)}$$

It is recommended to keep the input voltage ripple below 1% of the input voltage to limit noise that could be conducted through the battery harness.

Maximum input voltage ripple occurs in buck mode at a duty cycle of 0.5 and at max output current. Select a higher value for the final capacitor or bank of capacitors to account for DC Bias and tolerance derating.

Use the following equation to determine the input capacitance needed to meet the input voltage ripple requirement:

$$C_{IN} > \frac{0.25 \cdot I_{OUT\_MAX}}{f_{SW} \cdot \Delta V_{IN\_MAX} \cdot \left(1 - \left(C_{IN\_TOL} + C_{IN\_DCBIAS}\right)\right)} \text{ (eq. 9)}$$

Example

*f_{SW} = 400kHz ; I_{OUT_MAX} =5A ; D_{BUCK} = 0.5 ; C_{IN_TOL} = 10% ; C_{IN_DCBIAS} = 10% ; ΔV_{IN_MAX} = 12V * 0.01 = 0.12V*

For this example, C_{IN} > 27µF.

Select the input capacitor that can handle the given RMS current at the operating frequency. Ceramic capacitors come with extremely low ESR and help reduce the peak-to-peak ripple voltage at the input voltage. Good quality electrolytic capacitors are also available with low ESR, which give higher capacitance at low cost.

Electrolytic (bulk) input capacitors help reduce input voltage drop during large load transients. ESR in bulk capacitors help dampen line transients. A good combination of electrolytic and ceramic capacitors can help achieve the target specifications and minimize cost.

Place a high-frequency decoupling ceramic capacitor to filter high di/dt and reduce EMI caused by Qt1 turn on. Choose a small package, such as 0402, with low ESL.

Choose a voltage rating of 50V for applications where a 40V load dump can be seen at the input.

Output Capacitor Design

Output capacitance is selected to satisfy the output load-transient requirements. During a load step, the output current changes almost instantaneously whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. Select a capacitor based on the maximum allowable overshoot/undershoot on the output voltage. Typically, the worst-case response from a load transient is in boost mode. Use the following equations to contain the undershoot within the given specifications in boost mode:

$$C_{OUT} \geq \frac{L \cdot \Delta I_{L\_STEP}^{2}}{2 \cdot V_{IN\_MIN} \cdot D_{BOOST\_MAX} \cdot V_{UNDER}} + \frac{\left(\Delta I_{L\_STEP} \cdot t_{DELAY}\right)}{V_{UNDER}} \text{ (eq. 10)}$$

where t_{DELAY} = Time delay for the next control pulse after a load step. For fixed-PWM mode, t_{DELAY} is the turn-off time in buck/boost mode.

Select the output capacitance to handle load transients in deep boost mode. t_{DELAY} is the delay for the PWM modulator to react after a load step. In PWM mode, the worst-case delay would be (1-D) x t_{SW} when the load step occurs right after a turn-on cycle. With the previous example values:

$$C_{OUT} \geq 120\mu F$$

Once the output capacitance is selected, the output voltage undershoot/overshoot can be calculated for buck region of operation using the following equations:

$$V_{UNDER\_BUCK} = \frac{L \cdot \Delta I_{L\_STEP}^{2}}{2 \cdot (V_{IN} - V_{OUT}) \cdot D_{BUCK\_MAX} \cdot C_{OUT}} \text{ (eq. 11)}$$

$$V_{OVER\_BUCK} = \frac{L \cdot \Delta I_{L\_STEP}^{2}}{2 \cdot V_{OUT} \cdot C_{OUT}} \text{ (eq. 12)}$$

Select C_{OUT} to ensure low output voltage undershoot and ripple during a USB-PD load transient at low V_{IN}. VBUS load transients requirements may vary depending on the application. Contact Maxim for assistance with optimizing C_{OUT} for your application.

Output Voltage Setting

V_{OUT} target is selected using VOUT_SEL[1..0] register. Use the COMMAND[7..0] register to enable the buck-boost and request a new target V_{OUT} voltage. Refer to the register map for details.

Current-Sense Resistors Selection

The MAX25430 devices use three external current-sense resistors to provide current information to several functions. The input current-sense resistor R_{CS1} is used for inductor current control and setting the input cycle-by-cycle peak current limit. The output current-sense resistor R_{CS2} is used for output over-current faults, namely V_{BUS} DC I_{LIM}, V_{BUS} OCP, runaway and negative peak current limit. The R_{CS3} current-sense resistor is used for the cable compensation and is optional. Refer to the cable compensation section for more information.

Select an input current-sense resistor based on the maximum input current for the application (typically at maximum output power and minimum input voltage). The differential voltage across R_{CS1} for input current-limit threshold is 50mV. Calculate the peak input current using this equation:

$$I_{IN\_PEAK} = \frac{V_{OUT\_MAX} \cdot I_{OUT\_MAX}}{V_{IN\_MIN}} + \frac{V_{IN\_MIN} \cdot \left(1 - \frac{V_{IN\_MIN}}{V_{OUT\_MAX}}\right)}{2 \cdot L \cdot f_{SW}} \text{ (eq. 13)}$$

Calculate the input current-sense resistor (R_{CS1}) by setting the peak current limit slightly higher than the peak input current (I_{IN_PEAK}) calculated above.

It is highly recommended that designs use an R_{CS2} resistor with an exact value of 2.5mΩ. Since the V_{BUS} DC I_{LIM} is selected digitally (there are a discrete number of levels), changing this value also changes the possible current-limit thresholds. The overcurrent threshold values in the register will need to be scaled accordingly.

Slope Compensation

Slope compensation is required for current-mode control due to its inherent instability. A properly designed current-mode control with slope compensation removes the instability and provides noise immunity from current-sense signals. The MAX25430 offers a simple way to set the slope compensation peak ramp voltage (V_{SLOPE_PK}) by programming the SLP[2:0] register through I^2C from 100mV to 800mV in 100mV increments. Once V_{SLOPE_PK} is calculated, select the next value available in the SLP[2:0] register.

The steps to calculate V_{SLOPE_PK} are the following.

Design the slope compensation to lower the quality factor of the double pole at half the switching frequency of current-mode control. Choose the quality factor to be at or below 0.6 for the entire range of input and output voltages. The quality factor is given by the following equation:

$$Q_P = \frac{1}{\pi \cdot (m_C \cdot D' - 0.5)} \text{ (eq. 14)}$$

where m_C, the compensation ramp factor, is given by:

$$m_C = 1 + \frac{S_e}{S_n} \text{ (eq. 15)}$$

The compensation ramp slope, S_e, is:

$$S_e = \frac{V_{SLOPE\_PK}}{T_{SW}} = V_{SLOPE\_PK} * f_{SW} \text{ (eq. 16)}$$

And the inductor rising slope, S_n, is:

$$S_n = \frac{(V_{IN} - V_{OUT}) \cdot G_{CS}}{L} \text{ (eq. 17)}$$

S_e = Slope of the external ramp, in V/s.

S_n = Rising slope (upslope) of inductor current, in V/s.

V_{SLOPE_PK} = The slope compensation peak ramp voltage for a theoretical 100% duty cycle, in V.

f_{SW} = switching frequency, in Hz

D' = 1 - Duty Cycle

Example

Due to the several possible output voltages, an optimum SLP[2:0] setting needs to be calculated for each fixed output voltages supported. Verify Qp does not exceed the design target across the input voltage range. From the previous example, and with a maximum Qp target of 0.6, we can calculate the optimum SLP[2:0] for Vout = 5.15V.

Using equation 14, Qp = 0.4 yields mc = 1.82. With equation 17, we find $S_n = 1.89.10^5$ V/s. Then, equation 15 gives us $Se = 1.54.10^5$ V/s. Finally, re-arranging equation 16, we find V_{SLOPE_PK} = 385mV.

Set SLP[2:0] to achieve the desired peak-to-peak voltage for the external compensation as calculated above.

Select Set SLP[2:0] = 0b011 for V_{SLOPE_PK} = 400mV.

Repeat the steps above for each output voltage supported.

Error-Amplifier Compensation Design

The MAX25430 uses an internal transconductance amplifier with its output terminal available to the user for external frequency compensation, as shown in Figure 33.

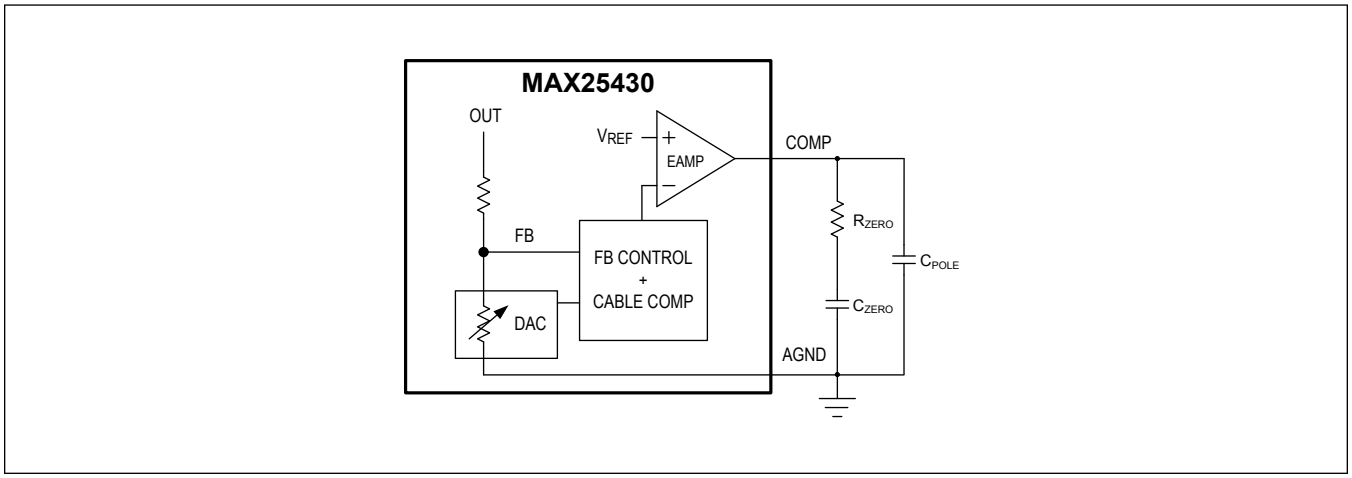


Figure 33. External compensation network

The controller uses a peak current-mode-controlled architecture to regulate the output voltage by forcing the required current through the external inductor. The external current-sense resistor senses the inductor current information. The current-mode control splits the double pole in the feedback loop caused by the inductor and output capacitor into two single poles. One of the poles is moved to a high frequency outside the typical bandwidth of the converter, making it a single-pole system. This makes compensation easy with only Type II required to compensate the loop. In boost mode, an extra right-half plane (RHP) zero is introduced by the power stage to add extra phase delay in the control loop. To avoid any significant effect of the RHP zero on the converter stability, the compensation is designed such that the bandwidth is approximately 1/4 of the worst-case RHP zero frequency.

The design of external compensation requires some iterations to reach an optimized design. Care must be taken while designing the compensation for working in 'deep' boost mode and heavy load (V_{IN_MIN}) as RHP zero frequency reduces.

A convenient way to design compensation for both buck and boost modes is to design the compensation at minimum input voltage and heavy load (deep boost mode). At this operating point, RHP zero is at its lowest frequency. Design the compensation to achieve a bandwidth close to 1/4 of the RHP zero frequency in deep boost mode. Verify the gain and phase margin with the designed compensation in buck mode. The closed-loop gain of the converter is a combination of the power-stage gain of the converter and error-amplifier gain.

The following equation demonstrates the current-mode-controlled boost power-stage transfer function:

$$\frac{\hat{V}_O}{\hat{V}_C} = \frac{R_L \cdot (1 - D)}{2 \cdot G_{CS}} \cdot \frac{\left(1 + \frac{S}{\omega_{ESR}}\right)\left(1 - \frac{S}{\omega_{RHP}}\right)}{\left(1 + \frac{S}{\omega_{P\_BOOST}}\right) \cdot F_H(s)} \quad \text{(eq. 18)}$$

where:

G_{CS} : current-sense gain = 23*R_{CS1}

$$\omega_{P\_BOOST} = \frac{2}{R_L \cdot C_{OUT}} \quad \text{(eq. 19)}$$

$$\omega_{ESR} = \frac{1}{R_C \cdot C_{OUT}} \quad \text{(eq. 20)}$$

$$\omega_{RHP} = \frac{R_L \cdot (1 - D)^2}{L} \quad \text{(eq. 21)}$$

$$F_H(S) = 1 + \frac{S}{\omega_N \cdot Q_P} + \left(\frac{S}{\omega_N}\right)^2 \text{ (eq. 22)}$$

$$Q_P = \frac{1}{\pi \cdot (m_C \cdot D' - 0.5)} \text{ (eq. 23)}$$

$$\omega_N = \frac{\pi}{T_{SW}} \text{ (eq. 24)}$$

Error-amplifier transfer function:

$$H_{EA}(S) = g_M \cdot R_{DC} \cdot \frac{\left(1 + \frac{S}{\omega_{Z\_COMP}}\right)}{\left(1 + \frac{S}{\omega_{P1\_COMP}}\right) \cdot \left(1 + \frac{S}{\omega_{P2\_COMP}}\right)} \text{ (eq. 25)}$$

$$\omega_{Z\_COMP} = \frac{1}{R_{ZERO} \cdot C_{ZERO}} \text{ (eq. 26)}$$

$$\omega_{P1\_COMP} = \frac{1}{R_{DC} \cdot C_{ZERO}} \text{ (eq. 27)}$$

$$\omega_{P2\_COMP} = \frac{1}{R_{ZERO} \cdot \left(\frac{C_{POLE} \cdot C_{ZERO}}{C_{POLE} + C_{ZERO}}\right)} \cong \frac{1}{R_{ZERO} \cdot C_{POLE}} \text{ if } C_{POLE} \ll C_{ZERO} \text{ (eq. 28)}$$

Closed loop gain = Power stage gain x EA gain

Example

Start the compensator design by calculating the critical frequencies for the boost power stage at the minimum input voltage and maximum load.

$$f_{PBOOST} = \frac{2}{2\pi \cdot R_L \cdot C_{OUT}} \text{ (eq. 29)}$$

$$f_{ESR} = \frac{1}{2\pi \cdot R_C \cdot C_{OUT}} \text{ (eq. 30)}$$

For a converter operating in boost mode, the inductor selection determines the RHP frequency and hence the stability of converter in deep boost mode. Calculate the RHP zero frequency in deep boost mode using the calculated inductor value.

$$f_{RHP} = \frac{R_L \cdot (1 - D_{BOOST\_MAX})}{2\pi \cdot L} \text{ (eq. 31)}$$

Where:

R_L : output Load in Ω. $R_L = \frac{V_{OUT}}{I_{OUT}}$

C_{OUT} : output capacitance in F, choosen to be 214µF

R_C : output capacitor ESR in Ω, chosen to be 3.5mΩ

D_{BOOST_MAX} : maximum duty cycle in boost mode calculated earlier

L : inductance value calculated earlier, in H

Using above values, we find f_{PBOOST} = 372Hz, f_{ESR} = 213kHz, and f_{RHP} = 9.2kHz.

With RHP zero at 9.2kHz, the loop cutoff frequency for a stable operation must be less than 1/4 of the RHP zero frequency in deep boost mode.

Therefore, a target bandwidth for the closed-loop converter close to 1.8kHz is selected. The zero of the error amplifier must be placed well below the bandwidth to give enough phase boost at the crossover frequency. Typically, the zero is

placed close to the low-frequency pole. In such a case, resistor (R_{ZERO}) of the compensation can be calculated using the equation below:

$$R_{ZERO} = 2\pi \cdot f_{BW\_BOOST} \cdot \frac{G_{CS} \cdot C_{OUT}}{g_m \cdot (1 - D_{BOOST\_MAX})} \cdot \frac{(R_{BOT} + R_{TOP})}{R_{TOP}} \text{ (eq. 32)}$$

Where:

f_{BW_BOOST} : desired converter bandwidth in boost mode

g_m : error-amplifier transconductance, in A/V

R_{TOP}, R_{BOT} : top and bottom internal feedback network resistances, in Ω

$$R_{TOP} = 96k\Omega$$

$$R_{BOT} = \frac{R_{TOP}}{\frac{V_{OUT\_MAX}}{1.25V} - 1} \text{ (eq. 33)}$$

Choosing f_{BW_BOOST} = 1.8kHz yields R_{ZERO} = 11kΩ

And with f_{ZCOMP} = 1.2kHz,

$$C_{ZERO} = \frac{1}{R_{ZERO} \cdot 2\pi \cdot f_{ZCOMP}} \text{ (eq. 34)}$$

Therefore, C_{ZERO} = 12nF.

C_{POLE} decides the location of high-frequency pole. Select the high-frequency pole location higher than the bandwidth in buck mode so that it does not affect the phase margin and helps attenuate any high-frequency noises.

For f_{P2COMP} = 140kHz,

$$C_{POLE} = \frac{1}{R_{ZERO} \cdot 2\pi \cdot f_{P2COMP}} \text{ (eq. 35)}$$

Which yields C_{POLE} = 100pF.

For this example, the following component values would be selected: R_{ZERO} = 11kΩ, C_{ZERO} = 12nF, and C_{POLE} = 100pF.

External MOSFET Selection

Four external MOSFETs are required for the H-bridge buck-boost architecture supported by the MAX25430, as shown in the Typical Application Circuit. During the buck-mode of operation, Qt2 remains on and Qb2 remains off. Qt1 and Qb1 switch to regulate the output voltage. During the boost mode, Qt1 remains on, Qb1 remains off, and Qt2 and Qb2 switch to regulate the output voltage. In the buck-boost region, all four switches are used to control the output voltage. The MOSFETs must be selected based on certain critical parameters such as on-resistance, breakdown voltage, output capacitance, and input capacitances. A low R_{DSON} reduces the conduction losses in the MOSFET and a small gate/output capacitance reduces switching losses. Typically, a lower R_{DSON} MOSFET would have higher gate charge for the same breakdown voltage. Hence, a compromise must be made depending on conditions to which the MOSFET is subjected.

The MAX25430 comes with a 5V gate drive with a high current capability to support switching of 4 MOSFETs at high frequency. In the buck-boost region, the device switches between pure buck and boost modes to reduce the gate-drive current and increases the efficiency.

Boost Cap and Diode Selection

A bootstrap circuit is used to drive the floating gates of high-side switches Qt1 and Qt2. Boost cap provides the gate charge to the high side FET during the high-side turn-on and is recharged when the bottom switch turns on. Hence, the capacitance value of the boost capacitor must be selected such that the voltage drop during the discharge is under acceptable limits. Choosing a very large capacitor value slows down the charging of the capacitor, and it might not completely charge in the minimum off-time of the top switch.

Select the boost diode based on the average gate-drive current and blocking voltage for the diode. The maximum blocking voltage for the diode must be high enough to block the maximum drain-to-source voltage for the FET. A fast reverse-recovery diode would prevent any current being sourced into the bias supply from drain-to-source voltage. For the MAX25430 devices, the gate drive is powered by the BIAS regulator, which is 5V (typ).

Since the boost capacitor provides gate charge to the top switch, the value of the boost capacitance needed for less than a ΔV_{BOOST} ripple on boost capacitor can be written as:

$$C_{BOOST} \geq \frac{Q_G}{\Delta V_{BOOST}} \text{ (eq. 36)}$$

Average gate-drive current through the diode can be calculated as:

$$I_G = Q_G \cdot f_{SW} \text{ (eq. 37)}$$

where Q_G = total gate charge of the top MOSFET.

Shield Short-to-Battery

The Shield Short-to-Battery protection circuit requires that the total ground-path resistance from USB ground to system ground is approximately 13mΩ. This is required to achieve the correct threshold detection values and avoid false detection or surge currents larger than desired.

In applications where R_S is required for low-side current sensing by the TCPM, an N-CH FET with V_{DS} = 40V (min) should be chosen such that $R_{DS(ON)} + R_S$ = 13mΩ (V_{GS} = 4.5V). If R_S is not required, choose a FET such that $R_{DS(ON)}$ = 13mΩ. The 1nF shield capacitor must be rated for 50V (min).

A single NVTFS5C471NLTAG can be used as an N-Channel FET meeting the requirements with no R_S resistor.

USB Cable Compensation

The figure below shows a DC model of the voltage-correction function of MAX25430.

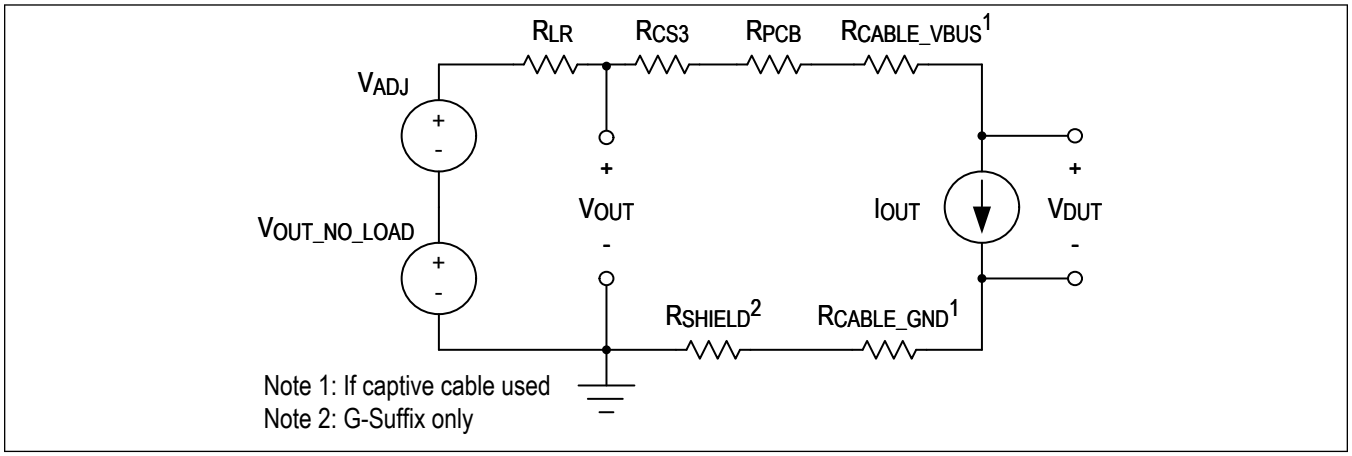


Figure 34. DC Voltage Adjustment Model

Without voltage adjustment (V_{ADJ} = 0, GAIN[5:0] = 0), the voltage seen by the device at the end of the captive cable (V_{DUT}) will decrease linearly as load current increases. To compensate for this, the output voltage target of the buck-boost controller should increase linearly with load current (see Figure 35).

The increase in V_{OUT} over load current is called V_{ADJ}, such that:

$$V_{ADJ} = R_{COMP} \cdot I_{OUT} \text{ (eq. 38)}$$

And R_{COMP} is the slope of V_{OUT} over the load current:

$$R_{COMP} = GAIN\left[5:0\right] \cdot R_{COMP\_LSB} \cdot \frac{R_{CS3}}{20m\Omega} \text{ (eq. 39)}$$

Where:

R_{COMP_LSB} is the gain setting LSB and is equal to 8mΩ, typically.

The R_{COMP} adjustment discrete values available on MAX25430 can be selected with the GAIN[5:0] register and are based on a 20mΩ sense resistor. Use equation 41 to select the appropriate setting based on the calculated R_{COMP} value.

The R_{COMP} value must be calculated to take into account all series element and voltage drops in the charging path, including ground return. User cable can be of different length and type, and therefore should not be included in the calculations.

For $V_{DUT} = V_{OUT\_NO\_LOAD}$; $0 \le I_{OUT} \le 5A$, R_{COMP} must equal the sum of the system resistances. Calculate the minimum R_{COMP} for the system so that V_{DUT} stays constant:

$$R_{COMP\_SYS} = R_{LR} + R_{CS3} + R_{PCB} + R_{CABLE\_VBUS} + R_{CABLE\_GND} \text{ (eq. 40)}$$

Where:

R_{CABLE_VBUS} and R_{CABLE_GND} are the VBUS and GND resistance of the USB captive cable, respectively (including the effect from the cable shield, if it conducts current)

R_{LR} is the converter's load regulation expressed in mΩ (2mΩ typ.)

R_{PCB} is the resistance of any additional V_{BUS} parasitics (PCB trace, ferrite, and the connector).

For G-Suffix devices, R_{SHIELD} is the series resistance of the Shield Short to Battery Protection external FET and any PCB GND trace parasitics.

Find the setting for GAIN[5:0] using the minimum R_{COMP}:

$$GAIN\left[5:0\right] = ceiling\left(\frac{R_{COMP\_SYS}}{R_{COMP\_LSB}}\right) \text{ (eq. 41)}$$

The nominal DUT voltage can then be estimated at any load current by:

$$V_{DUT} = V_{OUT\_NO\_LOAD} + I_{OUT}\left(R_{COMP\_LSB} \cdot GAIN\left[5:0\right] - R_{COMP\_SYS}\right) \text{ (eq. 42)}$$

These equations presume a 20mΩ sense resistor, which is recommended. Use equation 39 to scale for other resistance values.

The nominal cable resistance (with tolerance) for both V_{BUS} and GND should be determined from the cable manufacturer. In addition, be sure to include the resistance from the connector at the end of the captive cable. Determine the desired operating temperature range for the application, and consider the change in resistance over temperature. Contact Maxim for assistance with optimizing the cable compensation for your application.

Example

With R_{LR} = 2mΩ, R_{CS3} = 20mΩ, R_{PCB} = 40mΩ, R_{CABLE} = 150mΩ, R_{SHIELD} = 13mΩ, the total system resistance is then R_{COMP_SYS} = 2 + 20 + 40 + 150 + 13 = 225mΩ.

In this application, the voltage drop at the far end of the captive cable is 675mV when the load current is 3A. Therefore, cable compensation is required to comply with the USB and Apple specifications.

The desired GAIN[5:0] register setting is then ceiling(225/8) = 29 = 0x1D, which sets the adjustment level to 232mΩ.

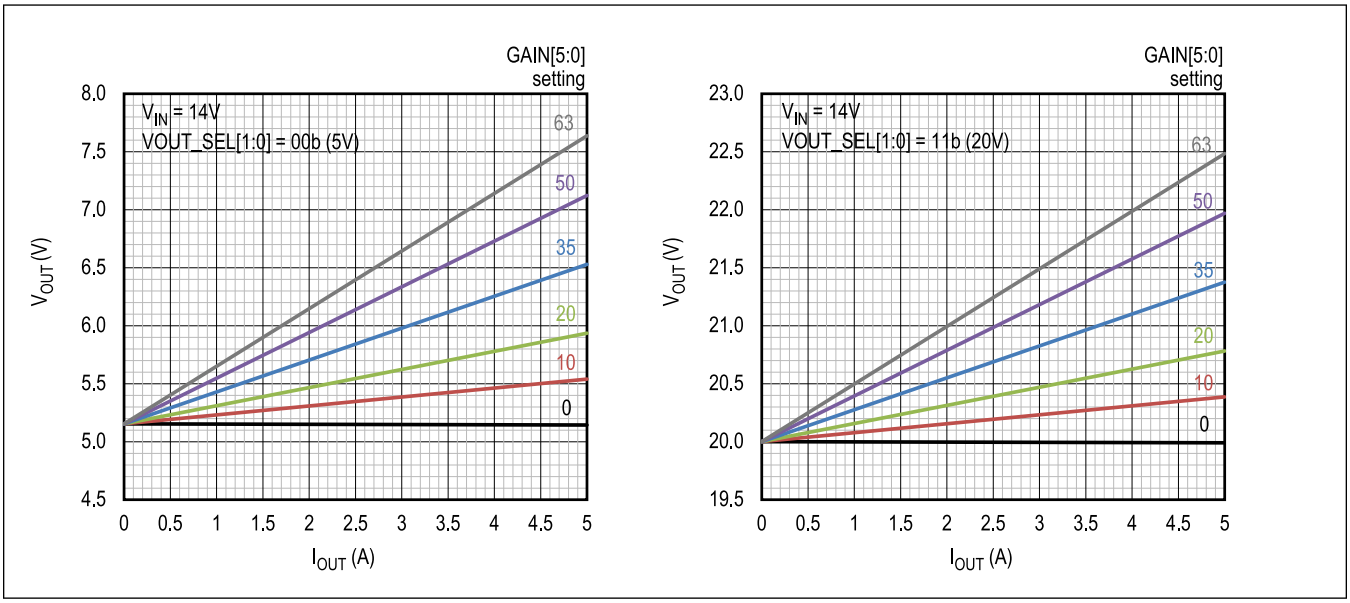


Figure 35. Increase in OUT vs. USB Current

Capacitors on CC lines

To comply with the USB-PD specification, a cReceiver capacitance must be present on each CC lines to ground when the BMC driver is not transmitting. Maxim recommends using 270pF ceramic capacitors to meet this requirement.

On MAX25430A, the capacitors can be placed on either CC or HVCC side. On MAX25430B, the capacitors should be placed on the HVCC side. Refer to the Application Diagrams at end of datasheet.

Table 13. cReceiver Specification from USB-PD

	Min	Max	Unit
cReceiver	200	600	pF

Table 14. cReceiver Capacitance Breakdown

	Min	Max	Unit
MAX25430 device capacitance on HVCC pins at 25°C	120	150	pF
External capacitor X7R 10% Tolerance	243	297	pF
Total	363	447	pF

VCONN voltage drop budgeting

Care must be taken when designing a VCONN source. Resistance in the VCONN switch, PCB traces and connector will impact the voltage seen by the e-marked cable under load. This is even more important when using a 3.3V supply to provide VCONN power. Use the formula below to estimate the VCONN voltage drop from the power supply to the user's port (assuming no captive cable).

$$V_{CONN\_DROP} = I_{VCONN} \cdot \left(R_{PCB1} + R_{ON} + R_{PCB2} + R_{CON}\right) = I_{VCONN} \cdot R_{VCONN\_TOTAL} \text{ (eq. 43)}$$

With:

R_{PCB1}: the PCB trace resistance from the VCONN source (DC/DC or LDO)

R_{ON} : the MAX25430 VCONN switch resistance

R_{PCB2}: the PCB trace resistance from the HVCC pin of MAX25430 to the Type-C Receptacle

R_{CON}: the contact resistance of the Type-C Receptacle CC pin

The Type-C specification requires the source to provide at least 3.0V under 1W of power at the receptacle for ports including the SSTX/SSRX signals (USB 3.0 or higher) but also for VCONN-Powered USB Devices (VPD) such as applications with remote LED lightning in a captive cable. For other applications, where charging above 3A is needed, the VCONN power required is 100mW at 3.0V.

Table 15. VCONN Requirements

Port Features			VCONN Requirements
D+/D-	SSTX/SSRX, VPD	>3A	
No	No	No	Not required
Yes	No	No	Not required
Yes	Yes	No	1W
No	No	Yes	100mW
Yes	No	Yes	100mW
Yes	Yes	Yes	1W

For a given VCONN power and voltage to meet at the port, the required current is calculated :

$$I_{VCONN\_PMIN} = \frac{P_{MIN}}{V_{DUT\_MIN}} = \frac{1W}{3.0V} = 0.33A \text{ (eq. 44)}$$

The minimum VCONN supply voltage needed to guarantee V_{DUT_MIN} at P_{MIN} at the receptacle is:

$$VCC_{MIN} = V_{DUT\_MIN} + R_{VCONN\_TOTAL} \cdot I_{VCONN\_PMIN} \text{ (eq. 45)}$$

Example

R_{PCB1} = 10mΩ; R_{ON_MAX} = 600mΩ; R_{PCB2} = 20m; R_{CON}=40m

$$VCC_{MIN} = 3.22V$$

For a 3.3V supply with a 2% output voltage tolerance, the lowest voltage supplied is:

$$VCC_{LOW} = VCC_{TYP} \cdot (1 - VCC_{TOL}) = 3.3 \cdot (1 - 0.02) = 3.234V > \quad VCC_{MIN} \text{ (eq. 46)}$$

Future-Proofing Your Design for PPS

Maxim recommends placing component footprints for a Type-2 compensation network from the NC pin to AGND to insure PCB design retro-compatibility with future USB-PD PPS pin-to-pin compatible products. Those products will require an external current loop compensation network connected to the existing MAX25430's NC pin.

The component footprints can be placed on the same or opposite PCB side as the IC. Connect the NC pin to GND through a 0R resistor when using MAX25430.

Additionally, the R_{CS3} external current sense resistor will be required for future USB-PD PPS pin-to-pin compatible products.

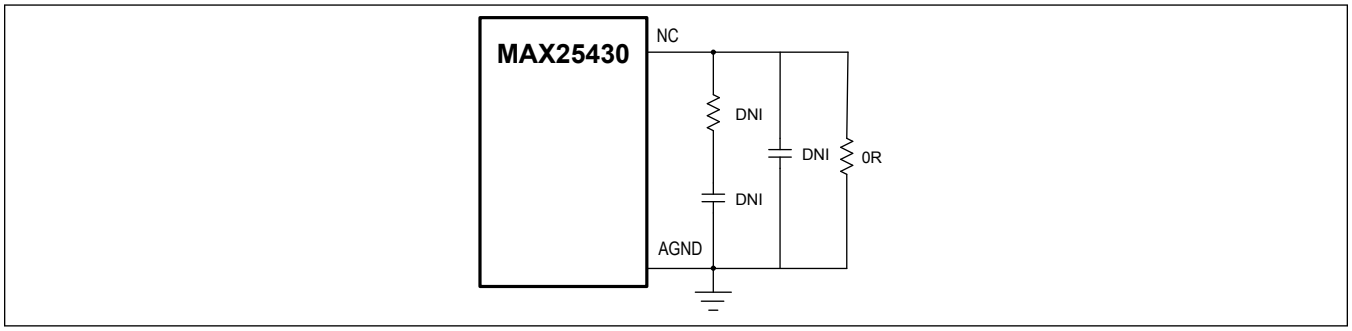


Figure 36. NC Pin Future Components

PCB Layout Guidelines

Buck-Boost PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and thermals.

Follow the guidelines below for a good PCB layout:

1) Arrange the high-power components in a compact layout away from the sensitive signals such as the current-sense and gate-drive signals, etc., to avoid stray noise pickup.

2) Place the input capacitor and the input current-sense resistor close to the input MOSFETs (Qt1 and Qb1) to make a small input current AC loop. High-frequency AC currents flow in this loop in buck mode Figure 37 and a small loop helps with the EMI and noise performance. Add high-frequency decoupling caps to improve the high-frequency performance.

3) Place the output capacitor and the output current-sense resistor close to the output MOSFETs (Qt2 and Qb2) to make a small output-current AC loop. High-frequency AC currents flow in this loop in boost mode Figure 37 and a small loop helps with the EMI and noise performance. Add high-frequency decoupling caps to improve the high-frequency performance.

4) The switching nodes (LX1 and LX2) carry high-frequency, high-current switching signals. Make LX1 and LX2 areas small to reduce parasitic inductance in the switching nodes. Since high currents flow through these nodes, a compromise must be made between thermal dissipation and noise mitigation.

5) Use a Kelvin sense connection for the current-sense resistors and route the sense traces close to each other to ensure a balanced measurement of the differential signal. Route these traces away from other noisy traces.

6) Use short and thick traces for gate connection to avoid any gate ringing.

7) Using internal PCB layers as a ground plane helps to improve EMI performance. A solid ground plane immediately below the top layer act as a shield against radiated noise. Have multiple vias spread around the board, especially near the ground connections, to have better overall ground connection.

8) Connect the PGND and AGND pins directly to the exposed pad under the IC. This ensures the shortest connection path between AGND and PGND.

9) Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add several small vias or one large via on the copper pad for efficient heat transfer.

10) Place the BIAS ceramic capacitor as close as possible to the BIAS pin. The BIAS pin carries significant transients and supplies everything in the IC. Low inductance from the pin to the capacitor and low inductance to the GND return plane is key. Pay extra care in reducing parasitic inductance to reduce EMI. As the AGND pin is located after the IN and COMP pins, a trade-off must be made. Always give more importance to the BIAS capacitor placement over the IN-pin decoupling capacitor and compensation network as it helps filter out high di/dt switching currents.

11) Place the compensation network components close to the COMP pin. Minimize trace inductance and provide a short ground return path using several vias to the ground plane underneath. Place the compensation network components away from the power stage in order to prevent high frequency switching noise to couple into the feedback loop.

12) Place the bootstrap capacitors close to the respective BST and LX pins to minimize inductance.

13) Leave the option the place series gate and BST resistors on the PCB to mitigate possible EMI issues at a later design stage.

14) Place the 100nF and 1uF ceramic capacitor close to the IN pin with a short path to the ground layer underneath. Place the 100nF capacitor closer to the pin.

15) Place vias as close to the AGND pins as possible to provide a low impedance path to the ground plane underneath

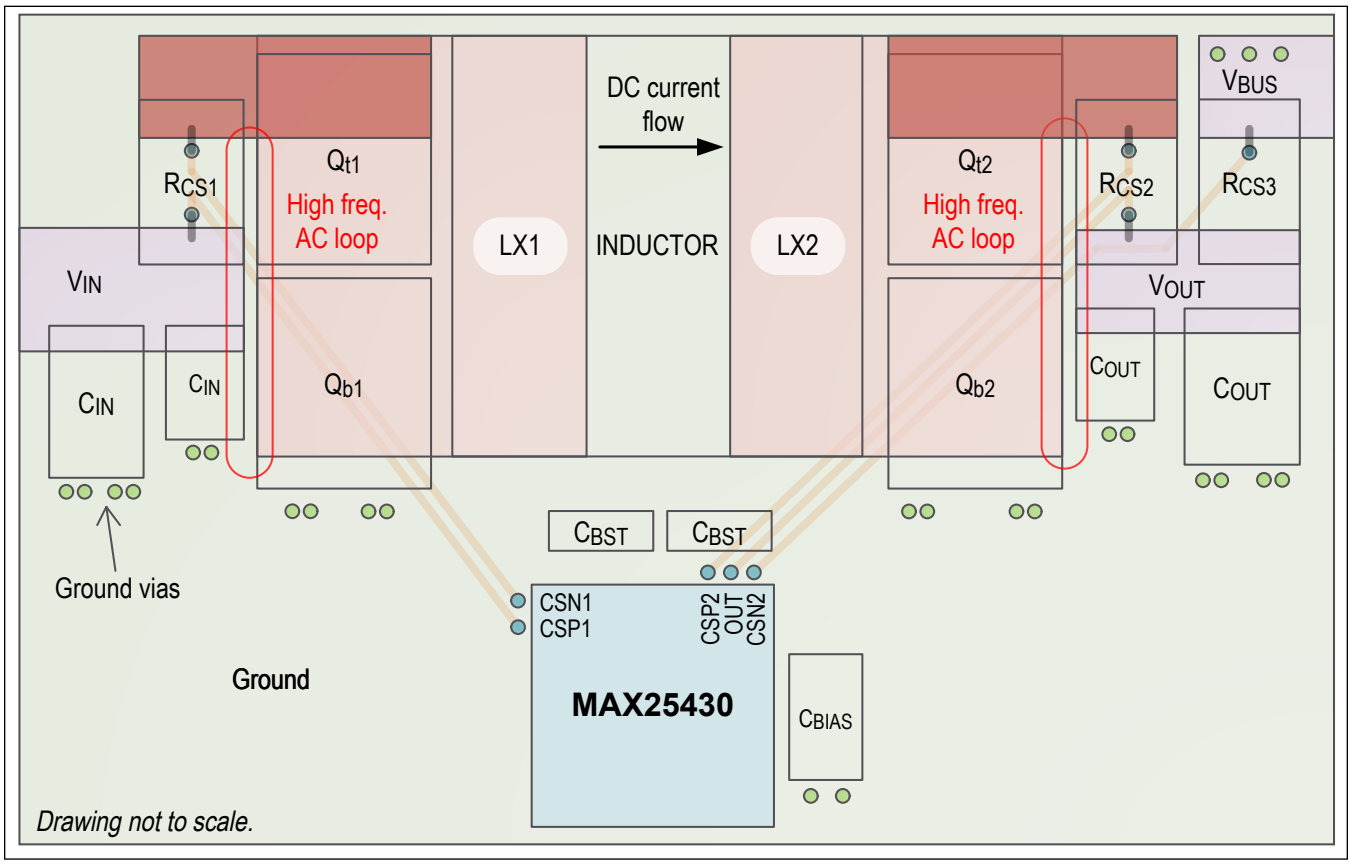


Figure 37. Recommended Buck-Boost PCB Layout

USB PCB Layout Guidelines

1) Place the VDD_USB ceramic capacitor close to the respective pin and with a low impedance to ground. Use vias to the ground plane underneath. The VDD_USB capacitor helps provide low impedance AC return path to ground during OV transients or ESD events on the USB data protection switches.

2) Place the VCONN ceramic capacitor close to the respective pin and with a low impedance to ground. Use vias to the ground plane underneath. The VCONN capacitor helps provide a low impedance AC return path to ground on the respective HVCC pin during a VCONN Short-to-VBUS event. The VCONN capacitor also helps minimize droop on the upstream supply during high inrush current events such as capacitive load switching or a hot short-to-ground event.

3) Keep the HVCC traces large and short to minimize VCONN voltage drop from the MAX25430 to the Type-C receptacle.

4) Refer to *USB Eye Diagram* section for recommendations when MAX25430 is used in the USB Hi-Speed signal path.

5) On MAX25430B devices, place the VDD_BMC ceramic capacitor close to the respective pin with a low impedance to ground. Use vias to the ground plane underneath.

Shield Short-to-Battery PCB Layout Guidelines

The FET and resistor R_S (if used) should be placed as close as possible to the Type-C connector and the FET must be connected to the connector with a plane. Where either the FET or R_S connects to system ground, there should be several vias placed for a low-impedance path to ground. If R_S is not used in the application, connect the source of the Shield FET directly to the system ground. The 1nF capacitor from SHIELD_SNS to ground should also be placed closely to the Type-C connector.

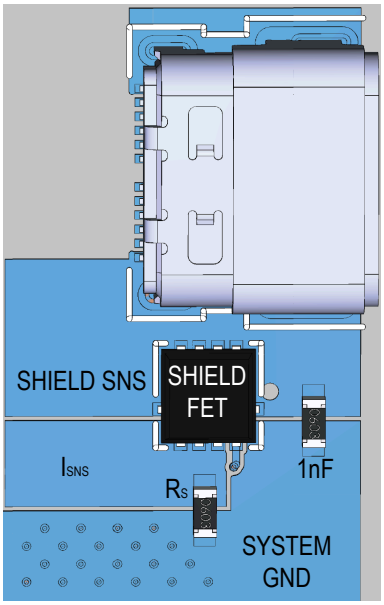


Figure 38. Recommended Shield Short-to-Battery Component Layout

USB Eye Diagram

USB Hi-Speed mode requires careful PCB layout with 90Ω controlled differential impedance, with matched traces of equal length and with no stubs or test points. MAX25430 includes high-bandwidth USB data switches (>1GHz). This means data-line tuning is generally not required.

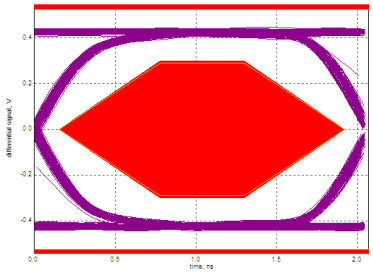


Figure 39. Near-Eye Diagram (with No MAX25430)

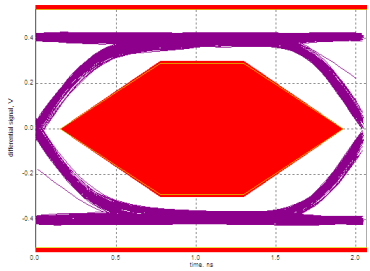


Figure 40. Untuned Near-Eye Diagram (with MAX25430)

ESD Protection

The MAX25430 requires no external ESD protection. All Maxim devices incorporate ESD protection structures to protect against electrostatic discharges encountered during handling and assembly. After an ESD event, the MAX25430 continues to work without latch-up, while competing solutions can latch-up and require the power to be cycled. When used with the configuration shown in the Typical Application Circuit, the MAX25430 is characterized for protection to the following limits:

1. ±15kV IEC 61000-4-2 (150pF, 330Ω) Air Gap
2. ±8kV IEC 61000-4-2 (150pF, 330Ω) Contact
3. ±15kV ISO 10605 (330pF, 2kΩ) Air Gap
4. ±8kV ISO 10605 (330pF, 2kΩ) Contact

Note: All application-level ESD testing is performed on the standard evaluation kit.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for test setup, test methodology, and test results.

Human Body ESD

Figure 41 shows the Human Body Model, and Figure 42 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

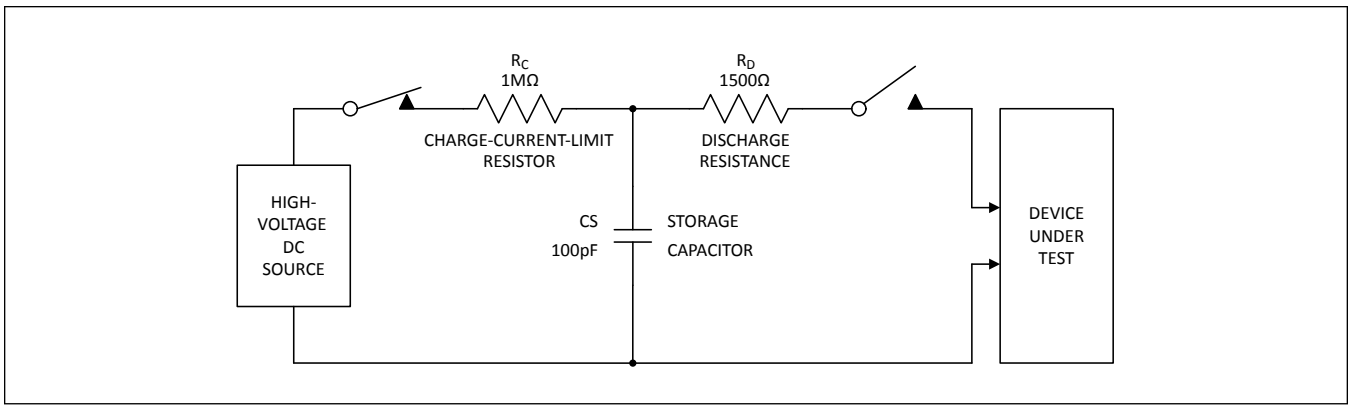


Figure 41. Human Body ESD Test Model

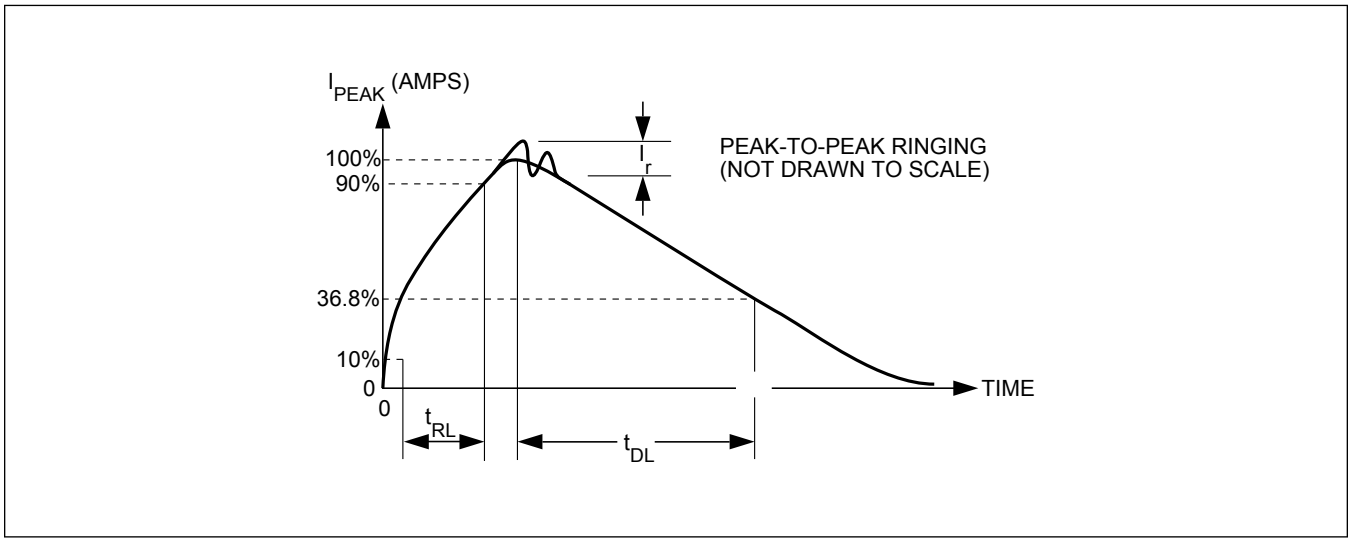


Figure 42. Human Body Current Waveform

IEC 61000-4-2 ESD

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. MAX25430 helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. Because the series resistance is lower in the IEC 61000-4-2 ESD test model Figure 43, the ESD withstand-voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 44 shows the current waveform for the 8kV, IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

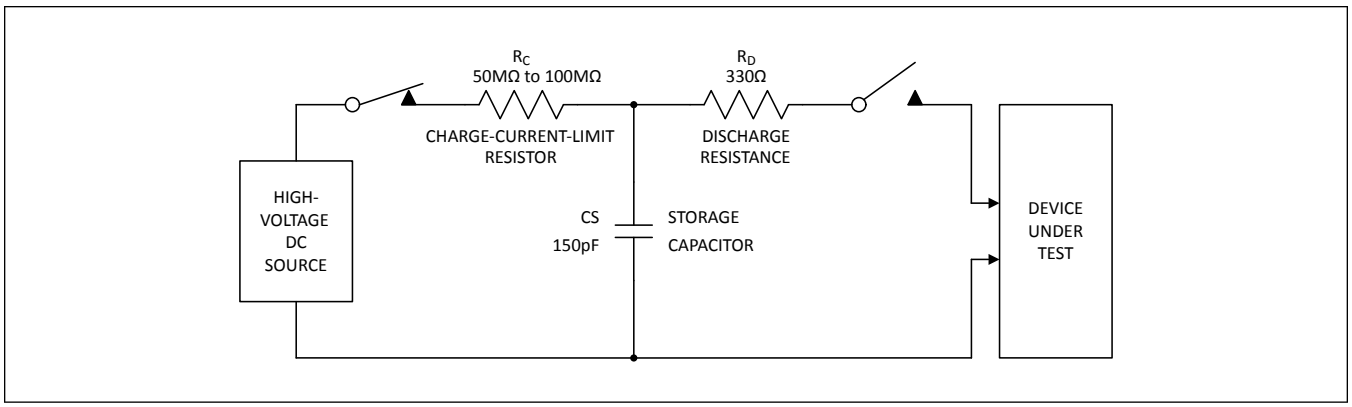


Figure 43. IEC 61000-4-2 ESD Test Model

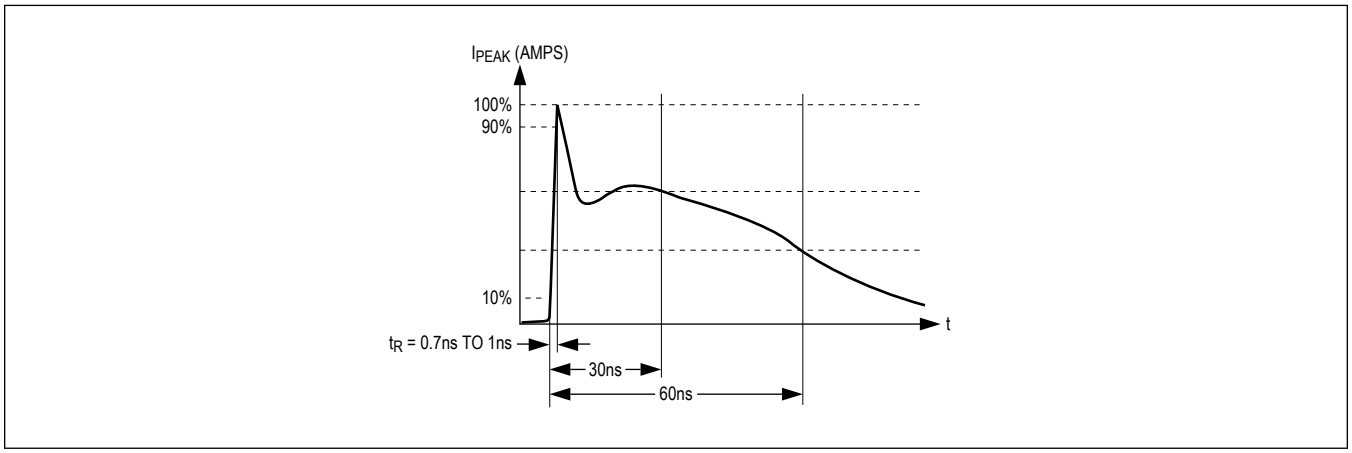
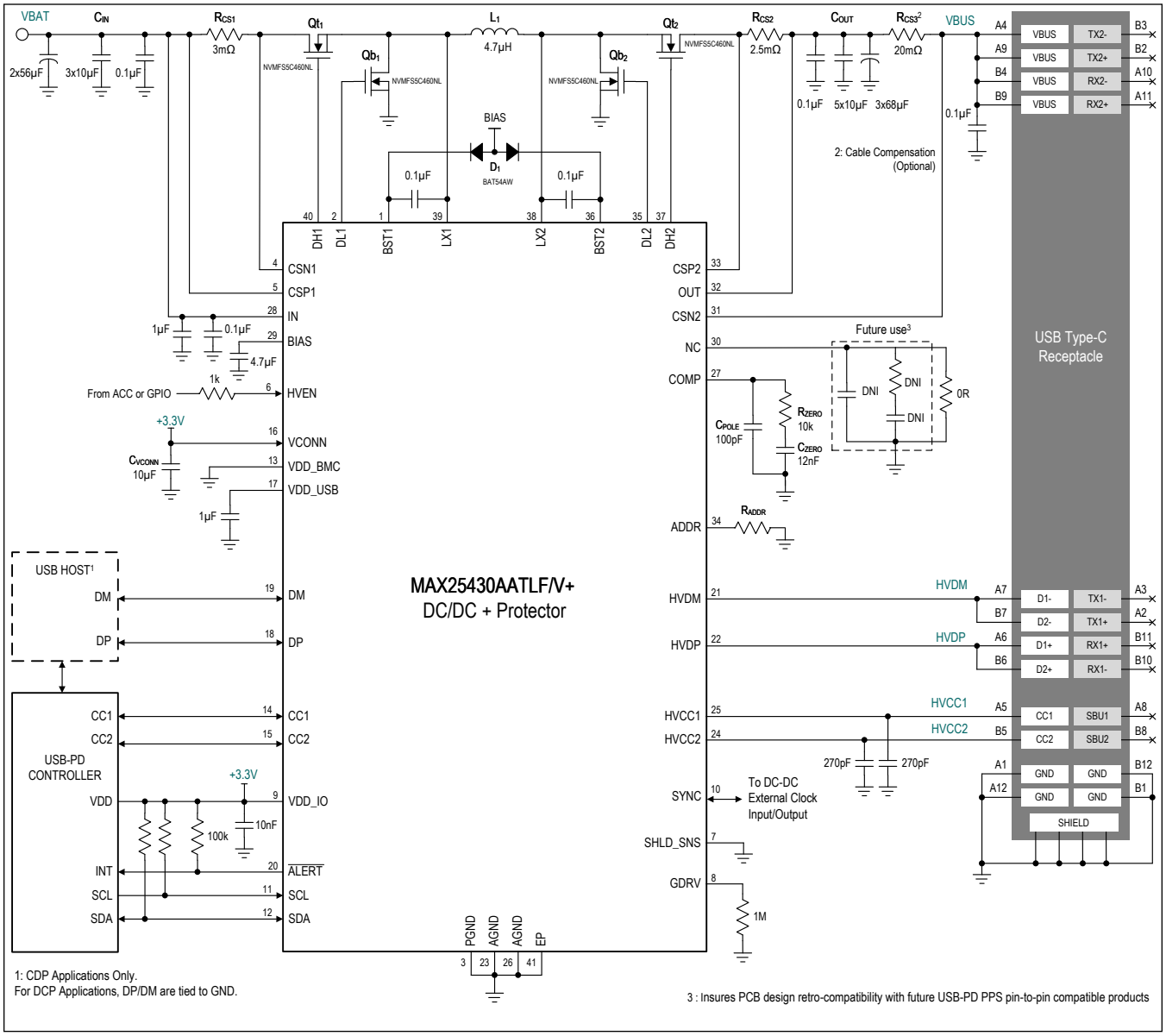


Figure 44. IEC 61000-4-2 Current Waveform

Typical Application Circuits

MAX25430A Application Diagram

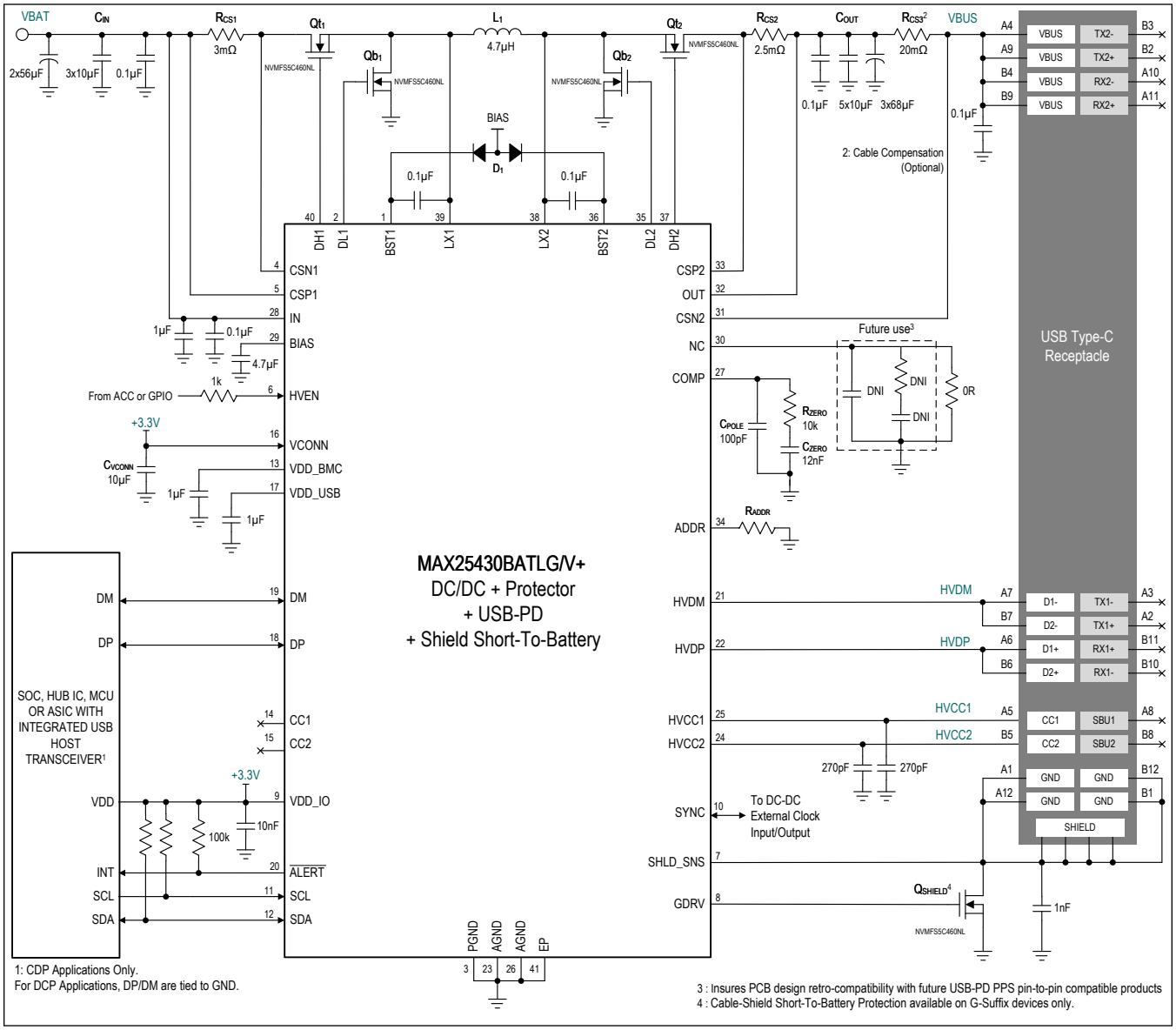
The figure below shows MAX25430AATLF/V+ with an external USB-PD Controller in a 100W Single-Port Application operating at 400kHz.



Typical Application Circuits (continued)

MAX25430B Application Diagram

The figure below shows MAX25430BATLG/V+ with an external TCPM in a 100W Single-Port USB-PD Application operating at 400kHz .



Ordering Information

PART NUMBER	TEMP RANGE	USB-PD ARCHITECTURE	VOLTAGE CONTROL METHOD	MAX VBUS VOLTAGE	CABLE SHIELD SHORT TO BATTERY PROTECTION	DEVICE ID	PIN-PACKAGE
MAX25430AATLF/V+	-40°C to +125°C	USB-PD Controller Protection	I2C	20V	No	0x0A00	40-Pin TQFN-EP
MAX25430AATLG/V+*		USB-PD Controller Protection	I2C	20V	Yes	0x0A00	
MAX25430BATLF/V+*		Integrated[1]	I2C	20V	No	0x0200	
MAX25430BATLG/V+*		Integrated[1]	I2C	20V	Yes	0x0200	

For variants with different options contact factory.

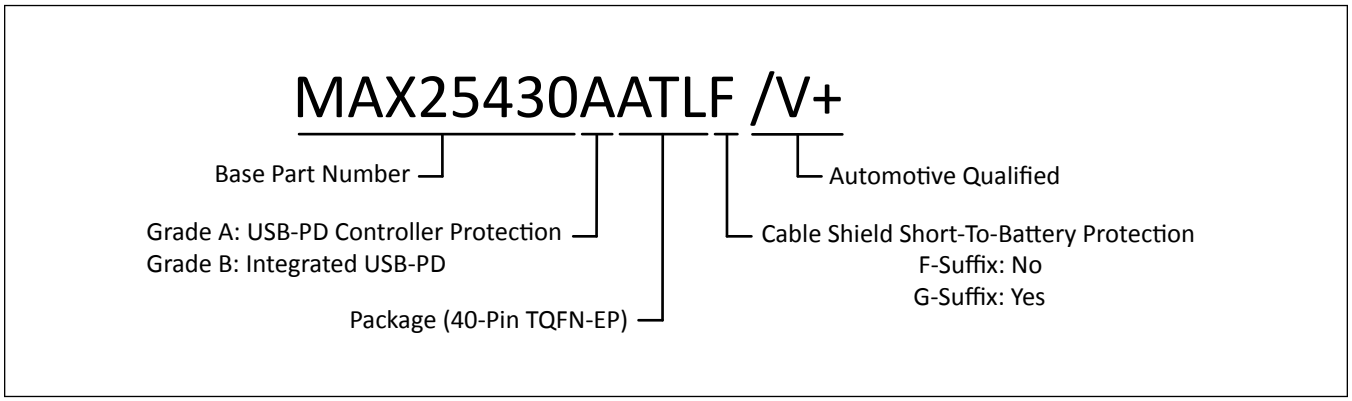
/V+ Denotes Automotive Qualified Parts

For Tape and Reel versions add the suffix 'T' to the end of the part number (i.e. MAX25430AATLG/V+T)

+ Denotes a lead (Pb) free/RoHS compliant package

** Future product – contact factory for availability*

1 Variant with integrated USB-PD BMC analog front-end (TCPC) for use with an external I2C Master which contains the USB-PD FW stack (TCPM)



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/20	Initial release	—