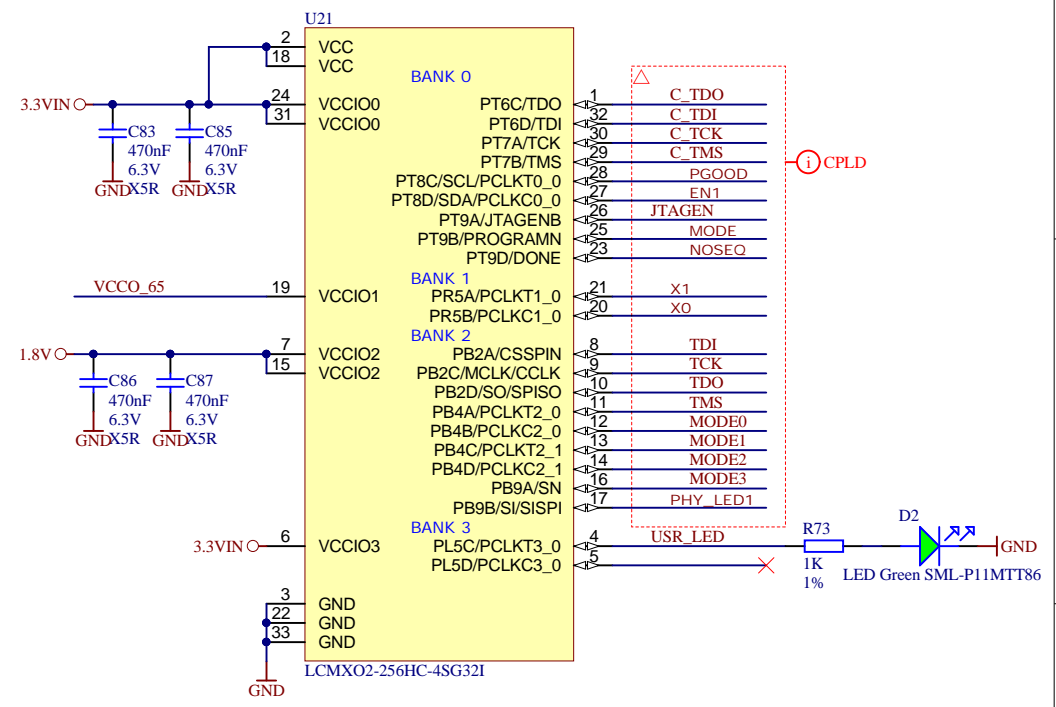
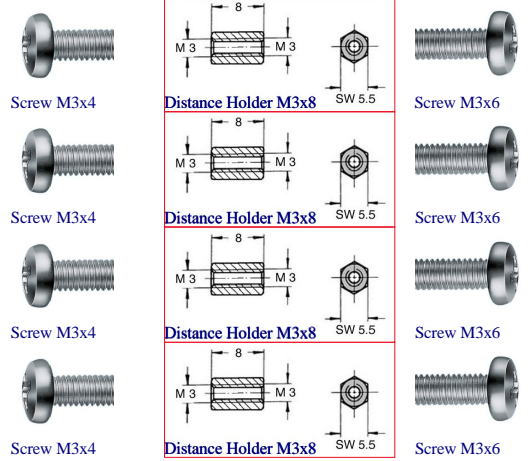
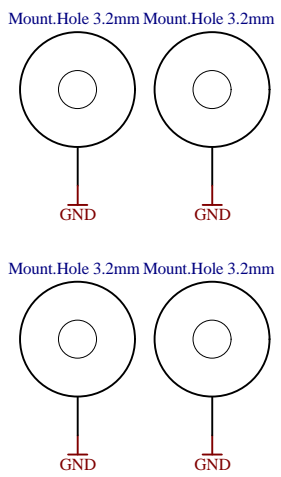
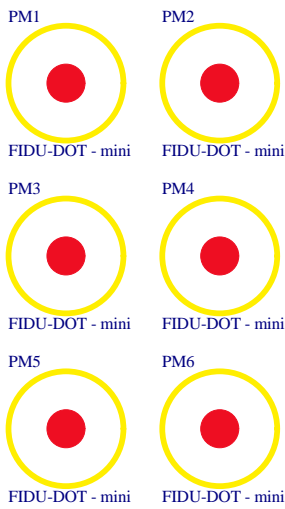
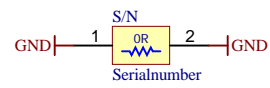


U_USB-PHY	USB-PHY.SchDoc
U_ETH-PHY	ETH-PHY.SchDoc
U_B_HD	B_HD.SchDoc
U_B64	B64.SchDoc
U_B65	B65.SchDoc
U_B66	B66.SchDoc
U_CONFIG	CONFIG.SchDoc
U_B_MIO	B_MIO.SchDoc
U_B_PS_GT	B_PS_GT.SchDoc
U_CLK	CLK.SchDoc

U_B2B-Connectors	B2B-Connectors.SchDoc
U_eMMC	eMMC.SchDoc
U_PS_DDR	PS_DDR.SchDoc
U_ZU_POWER	ZU_POWER.SchDoc
U_ZU_PS_POWER	ZU_PS_POWER.SchDoc
U_DDR4-RAM_2	DDR4-RAM_2.SchDoc
U_DDR4-RAM	DDR4-RAM.SchDoc
U_POWER	POWER.SchDoc
U_POWER_1	POWER_1.SchDoc

Serial  
Serialnumber 6,3 x 6.3mm



Assembly variant	02CG-1ED
Created by	VariantCreatedBy
Modified by	VariantModifiedBy
Modified at	VariantDateModification
SVN Revision	8646



Title: TE0820		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 1 of 21
Filename: TE0820.SchDoc		

1

2

3

4

A

A

B

B

C

C

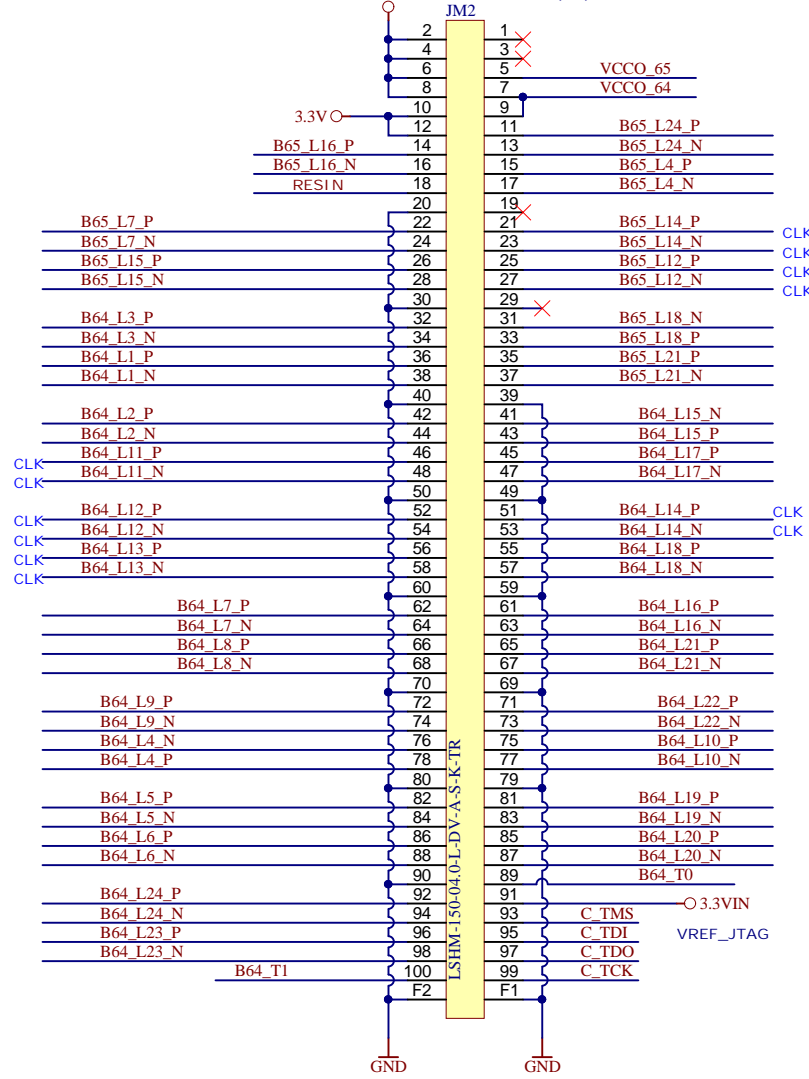
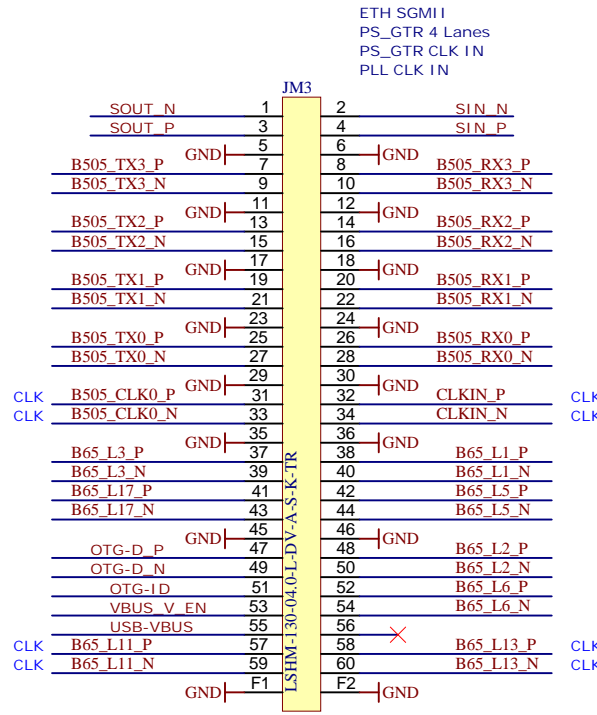
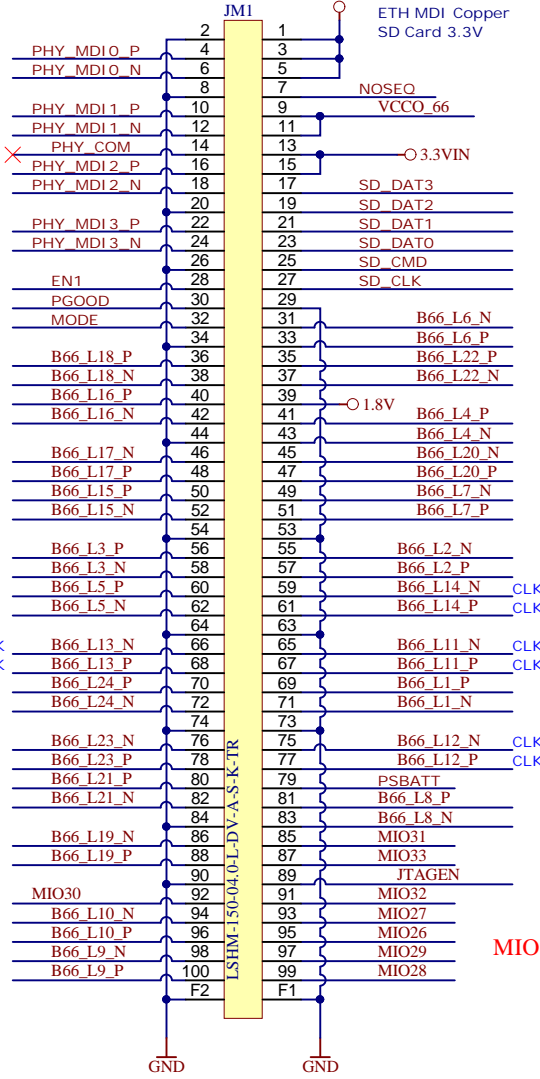
D

D

B66(HP) 48 IO, 24 LVDS Pairs  
 MIO501 8 IO, 3.3V  
 ETH MDI Copper  
 SD Card 3.3V

B65(HP) 16 IO, 8 LVDS Pairs  
 USB OTG  
 ETH SGMII  
 PS\_GTR 4 Lanes  
 PS\_GTR CLK IN  
 PLL CLK IN

B65(HP) 18 IO, 9 LVDS Pairs  
 B64(HP) 50 IO, 24 LVDS Pairs



VCCO64, VCCO65, VCCO66 ->>> max. 1.8V (HP bank's)

MIO[29..26] ->PJTAG1



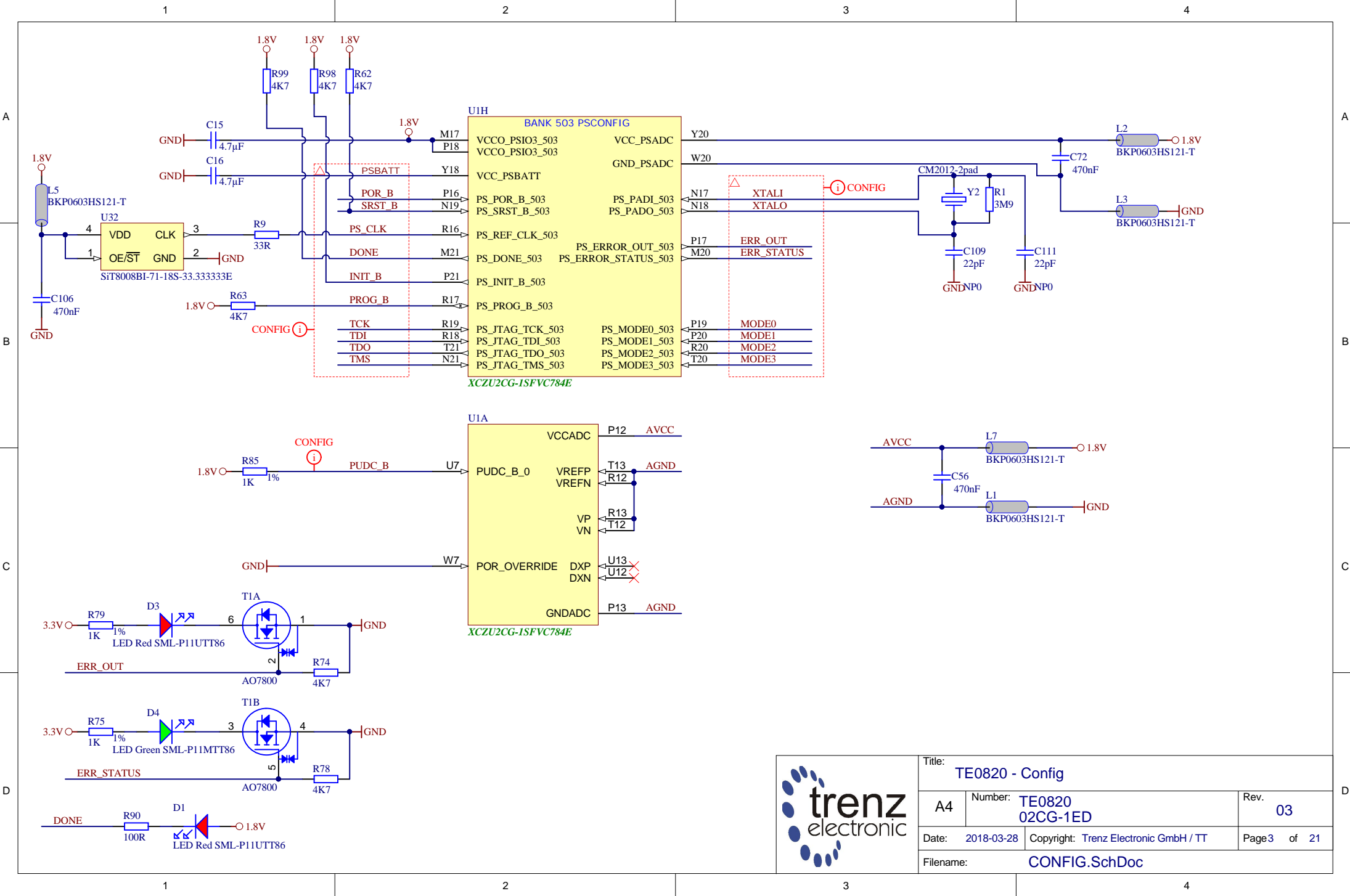
Title: TE0820 - B2B Connectors		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 2 of 21
Filename: B2B-Connectors.SchDoc		

1

2

3

4



Title: TE0820 - Config		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 3 of 21
Filename: CONFIG.SchDoc		

A

A

B

B

C

C

D

D

UIC

BANK 26 HD (ZU4/5 BANK 46 HD)

F14	VCCO_26
C15	VCCO_26
B15	IO_L1P_AD11P_26
A15	IO_L1N_AD11N_26
B14	IO_L2P_AD10P_26
A14	IO_L2N_AD10N_26
B13	IO_L3P_AD9P_26
A13	IO_L3N_AD9N_26
C14	IO_L4P_AD8P_26
C13	IO_L4N_AD8N_26
D15	IO_L5P_HDGC_AD7P_26
D14	IO_L5N_HDGC_AD7N_26
E14	IO_L6P_HDGC_AD6P_26
E13	IO_L6N_HDGC_AD6N_26
G13	IO_L7P_HDGC_AD5P_26
F13	IO_L7N_HDGC_AD5N_26
F15	IO_L8P_HDGC_AD4P_26
E15	IO_L8N_HDGC_AD4N_26
G15	IO_L9P_AD3P_26
G14	IO_L9N_AD3N_26
H14	IO_L10P_AD2P_26
H13	IO_L10N_AD2N_26
K14	IO_L11P_AD1P_26
J14	IO_L11N_AD1N_26
L14	IO_L12P_AD0P_26
L13	IO_L12N_AD0N_26

BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44
AG12	VCCO_44
AG10	IO_L1P_AD11P_44
AH10	IO_L1N_AD11N_44
AF11	IO_L2P_AD10P_44
AG11	IO_L2N_AD10N_44
AH12	IO_L3P_AD9P_44
AH11	IO_L3N_AD9N_44
AE10	IO_L4P_AD8P_44
AF10	IO_L4N_AD8N_44
AE12	IO_L5P_HDGC_AD7P_44
AF12	IO_L5N_HDGC_AD7N_44
AC12	IO_L6P_HDGC_AD6P_44
AD12	IO_L6N_HDGC_AD6N_44
AD11	IO_L7P_HDGC_AD5P_44
AD10	IO_L7N_HDGC_AD5N_44
AB11	IO_L8P_HDGC_AD4P_44
AC11	IO_L8N_HDGC_AD4N_44
AA11	IO_L9P_AD3P_44
AA10	IO_L9N_AD3N_44
W10	IO_L10P_AD2P_44
Y10	IO_L10N_AD2N_44
Y9	IO_L11P_AD1P_44
AA8	IO_L11N_AD1N_44
AB10	IO_L12P_AD0P_44
AB9	IO_L12N_AD0N_44

UIB

XCZU2CG-1SFVC784E

BANK 24 HD (ZU4/5 BANK 44 HD)

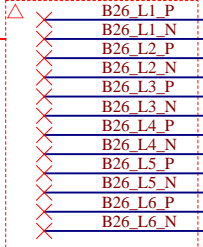
AA14	VCCO_24
AD13	VCCO_24
AE15	IO_L1P_AD15P_24
AE14	IO_L1N_AD15N_24
AG14	IO_L2P_AD14P_24
AH14	IO_L2N_AD14N_24
AG13	IO_L3P_AD13P_24
AH13	IO_L3N_AD13N_24
AE13	IO_L4P_AD12P_24
AF13	IO_L4N_AD12N_24
AD13	IO_L5P_HDGC_24
AD14	IO_L5N_HDGC_24
AC14	IO_L6P_HDGC_24
AC13	IO_L6N_HDGC_24
AA13	IO_L7P_HDGC_24
AB13	IO_L7N_HDGC_24
AB15	IO_L8P_HDGC_24
AB14	IO_L8N_HDGC_24
W14	IO_L9P_AD11P_24
W13	IO_L9N_AD11N_24
Y14	IO_L10P_AD10P_24
Y13	IO_L10N_AD10N_24
W12	IO_L11P_AD9P_24
W11	IO_L11N_AD9N_24
Y12	IO_L12P_AD8P_24
AA12	IO_L12N_AD8N_24

BANK 25 HD (ZU4/5 BANK 45 HD)

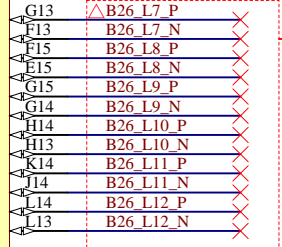
B12	VCCO_25
E11	VCCO_25
J11	IO_L1P_AD15P_25
J10	IO_L1N_AD15N_25
K13	IO_L2P_AD14P_25
K12	IO_L2N_AD14N_25
H11	IO_L3P_AD13P_25
G10	IO_L3N_AD13N_25
J12	IO_L4P_AD12P_25
H12	IO_L4N_AD12N_25
G11	IO_L5P_HDGC_25
G12	IO_L5N_HDGC_25
F11	IO_L6P_HDGC_25
F12	IO_L6N_HDGC_25
F11	IO_L7P_HDGC_25
D10	IO_L7N_HDGC_25
E12	IO_L8P_HDGC_25
D11	IO_L8N_HDGC_25
C11	IO_L9P_AD11P_25
B10	IO_L9N_AD11N_25
B11	IO_L10P_AD10P_25
A10	IO_L10N_AD10N_25
A12	IO_L11P_AD9P_25
A11	IO_L11N_AD9N_25
D12	IO_L12P_AD8P_25
C12	IO_L12N_AD8N_25

XCZU2CG-1SFVC784E

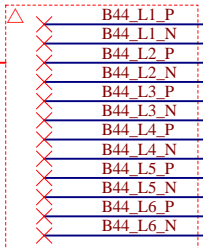
B26



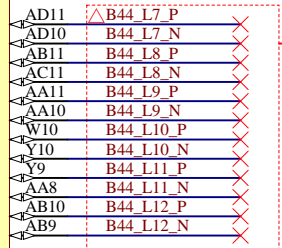
B26



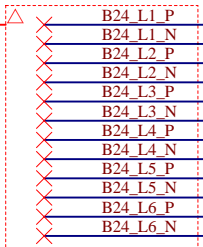
B44



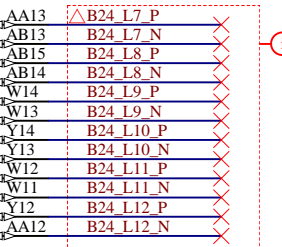
B44



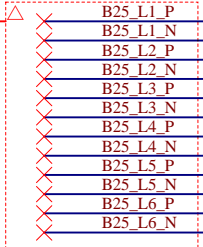
B24



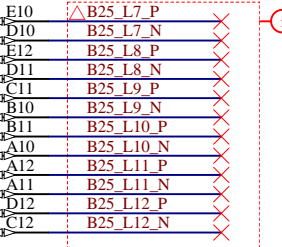
B24



B25



B25



Title: TE0820 - HD Banks		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 4 of 21
Filename: B_HD.SchDoc		

1

2

3

4

A

A

B

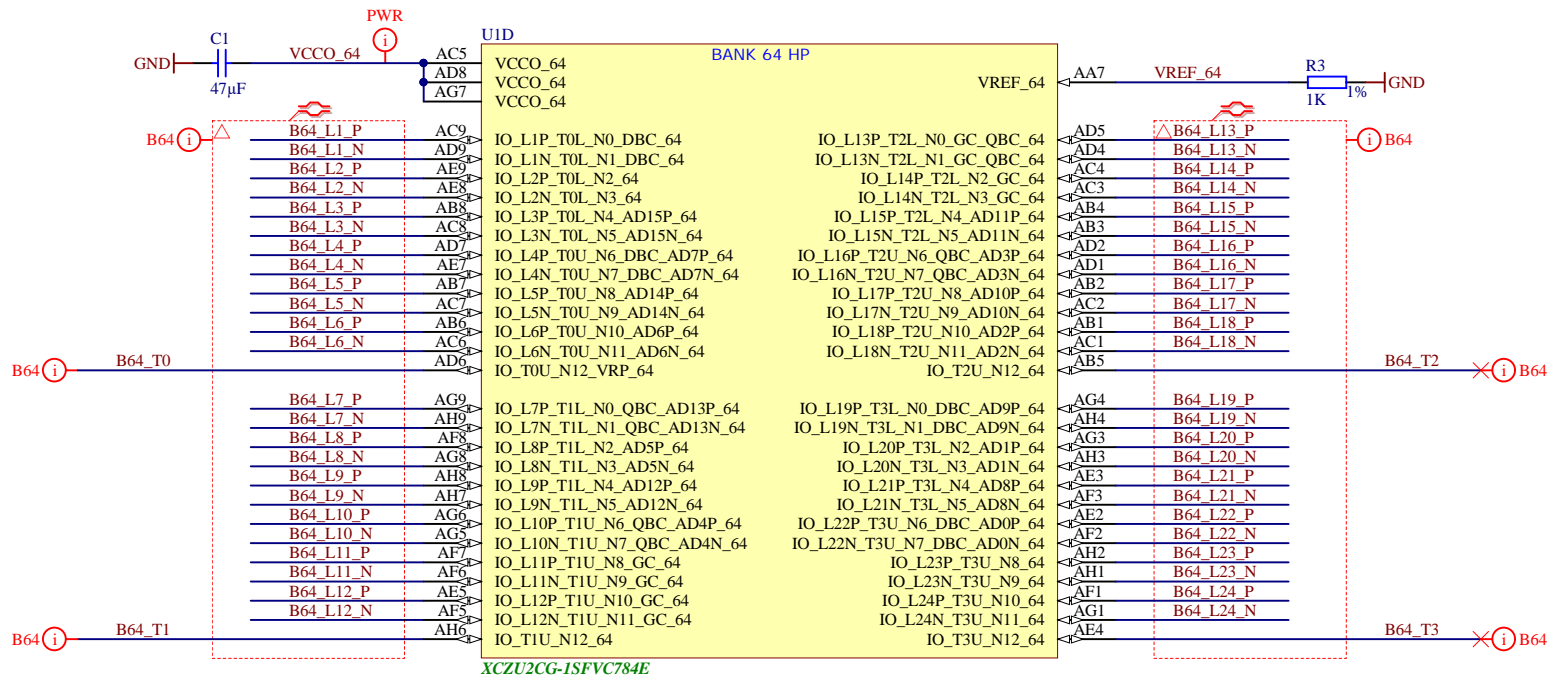
B

C

C

D

D



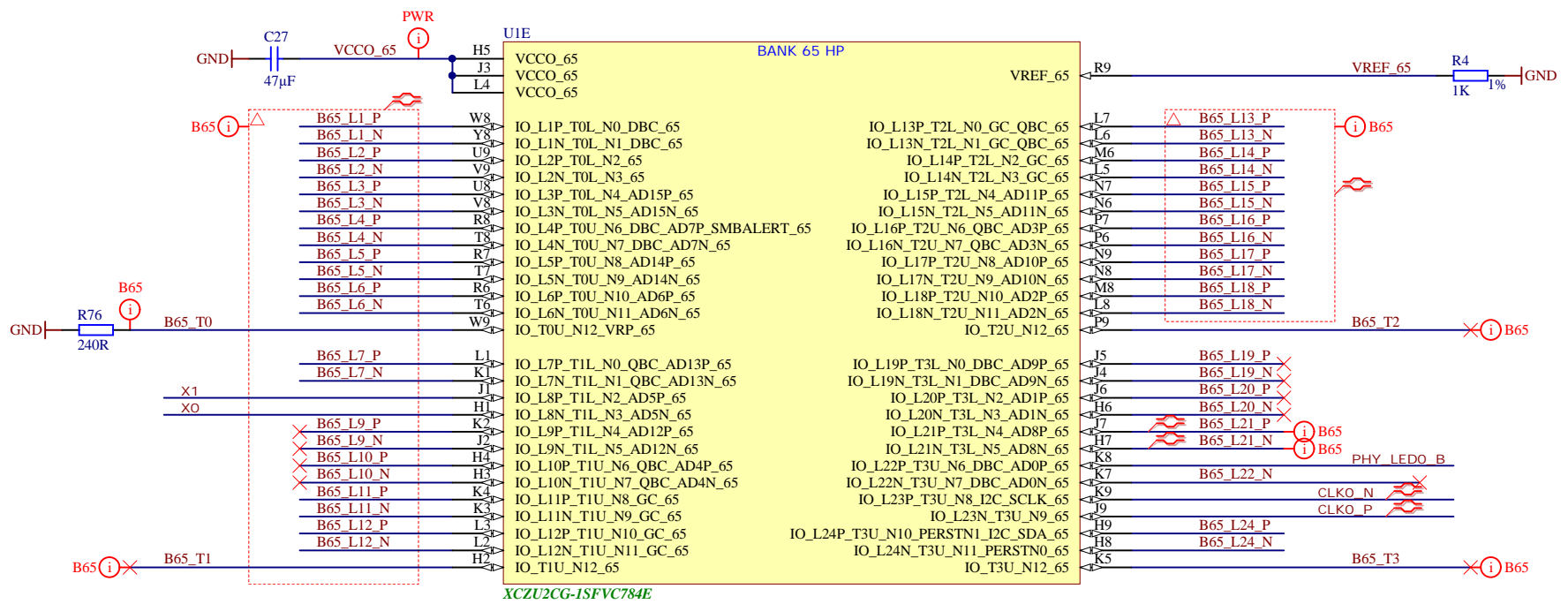
Title: TE0820 - B64		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 5 of 21
Filename: B64.SchDoc		

1

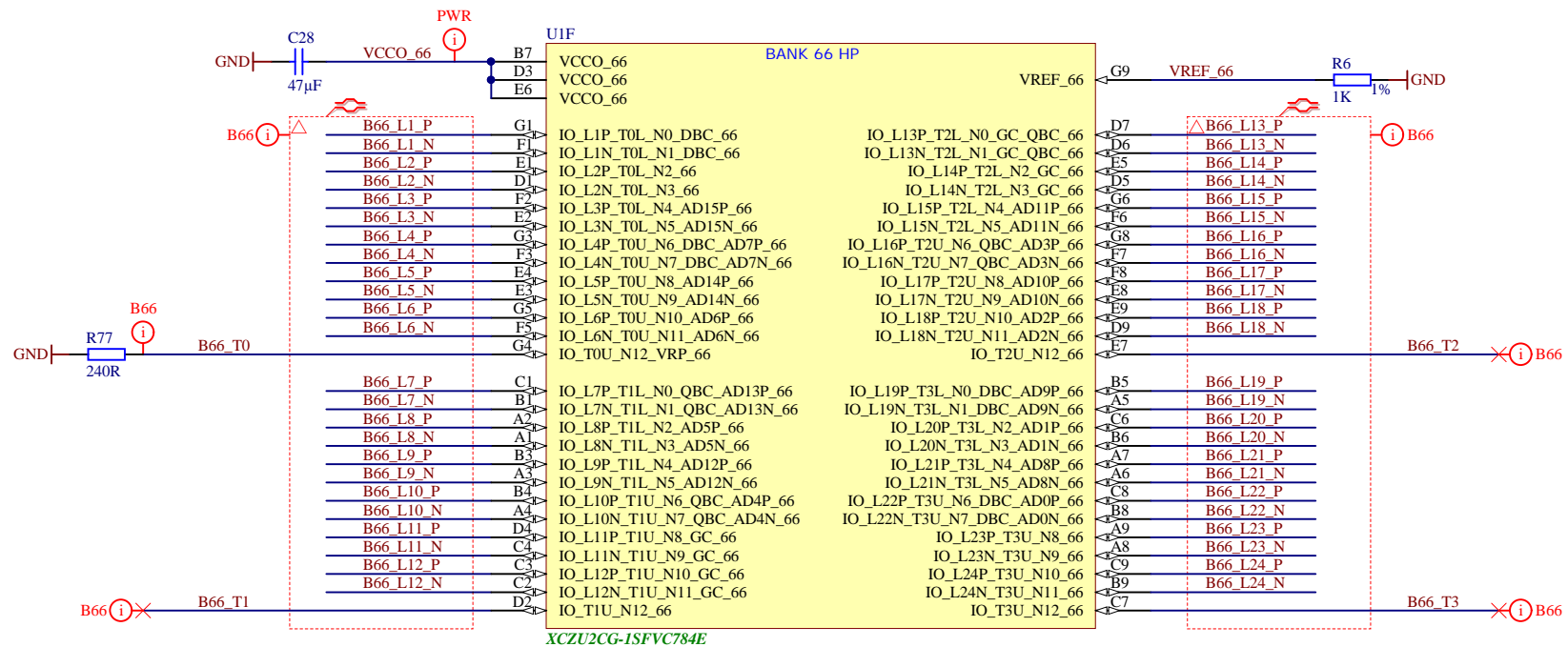
2

3

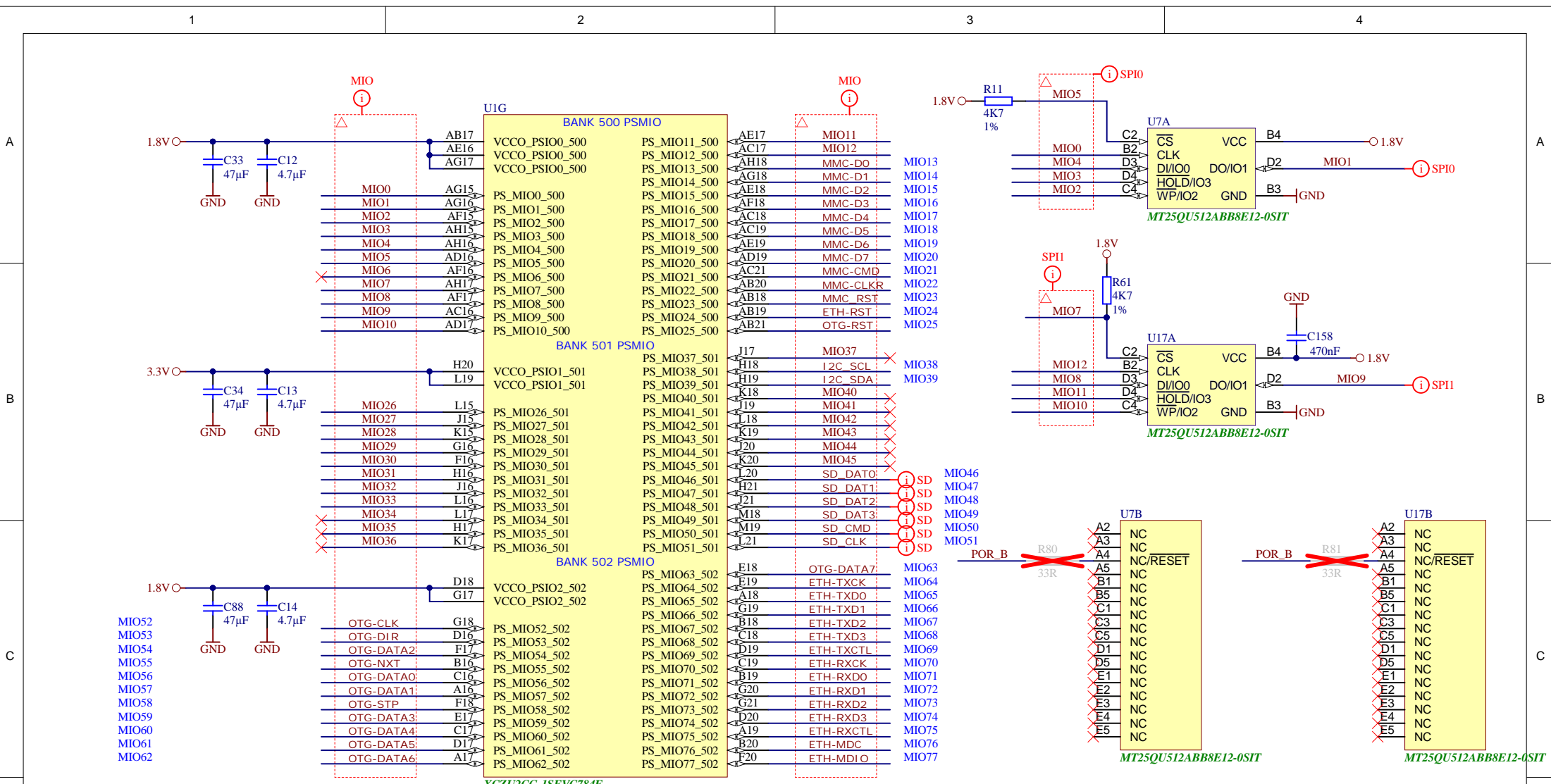
4



Title: TE0820 - B65		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 6 of 21
Filename: B65.SchDoc		

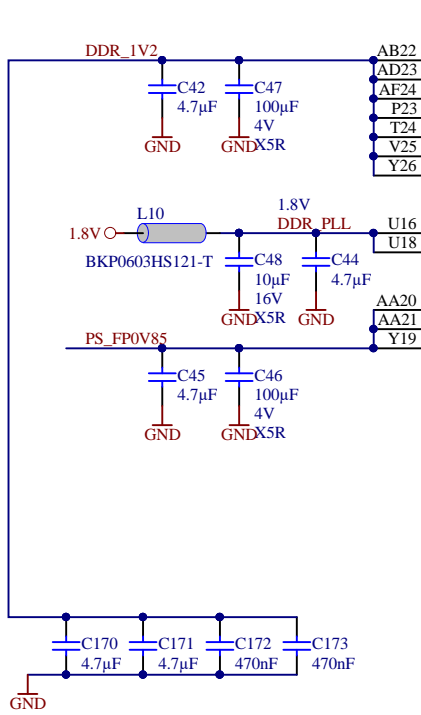


Title: TE0820 - B66		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 7 of 21
Filename: B66.SchDoc		



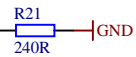
		Title: TE0820 - MIO Banks	
		A4	Number: TE0820 02CG-1ED
Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT	Rev. 03
Filename: B_MIO.SchDoc		Page 8 of 21	





U1I		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSINTFP_DDR	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSINTFP_DDR	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSINTFP_DDR	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSINTFP_DDR	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSINTFP_DDR	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSINTFP_DDR	PS_DDR_A8_504	AA22	DDR4-A8
PS_DDR_A9_504	PS_DDR_A9_504	AB23	DDR4-A9
PS_DDR_A10_504	PS_DDR_A10_504	AA25	DDR4-A10
PS_DDR_A11_504	PS_DDR_A11_504	AA26	DDR4-A11
PS_DDR_A12_504	PS_DDR_A12_504	AB25	DDR4-A12
PS_DDR_A13_504	PS_DDR_A13_504	AB26	DDR4-A13
PS_DDR_A14_504	PS_DDR_A14_504	AB24	DDR4-A14
PS_DDR_A15_504	PS_DDR_A15_504	AC24	DDR4-A15
PS_DDR_A16_504	PS_DDR_A16_504	AC23	DDR4-A16
PS_DDR_A17_504	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504	PS_DDR_CS_N0_504	W27	DDR4-CS
PS_DDR_CS_N1_504	PS_DDR_CS_N1_504	V26	
PS_DDR_BA0_504	PS_DDR_BA0_504	V23	DDR4-BA0
PS_DDR_BA1_504	PS_DDR_BA1_504	W22	DDR4-BA1
PS_DDR_BG0_504	PS_DDR_BG0_504	W24	DDR4-BG0
PS_DDR_BG1_504	PS_DDR_BG1_504	V22	
PS_DDR_PARITY_504	PS_DDR_PARITY_504	V24	DDR4-PAR
PS_DDR_RAM_RST_N_504	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
PS_DDR_ACT_N_504	PS_DDR_ACT_N_504	Y23	DDR4-ACT
PS_DDR_ALERT_N_504	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
PS_DDR_ZQ_504	PS_DDR_ZQ_504	U24	
PS_DDR_ODT0_504	PS_DDR_ODT0_504	U28	DDR4-ODT0
PS_DDR_ODT1_504	PS_DDR_ODT1_504	U26	

XCZU2CG-1SFVC784E

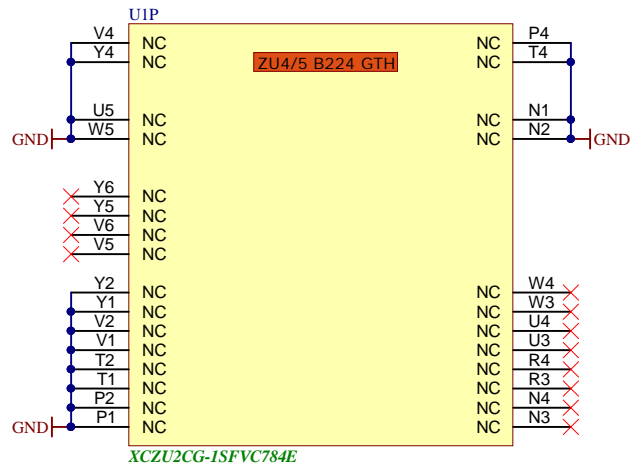
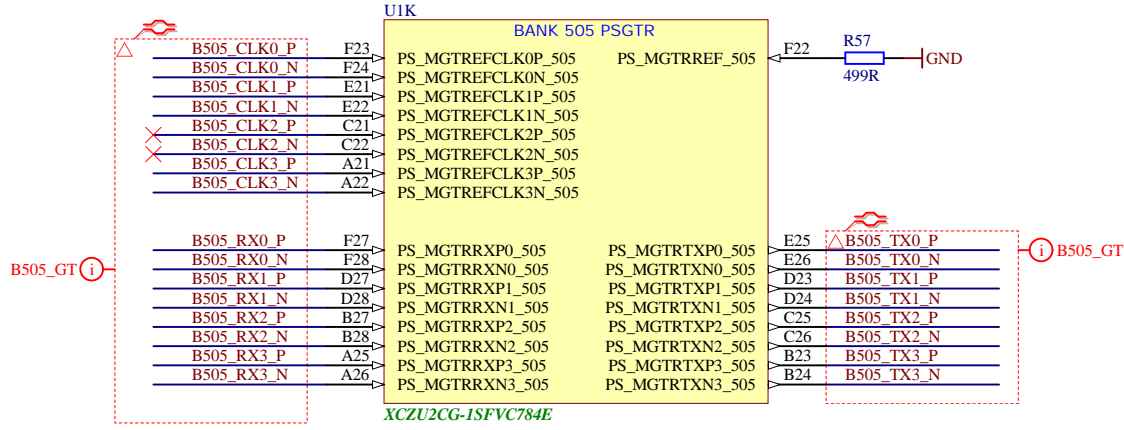


U1J		BANK 504 PSDDR	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2_N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3_N	AE27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
PS_DDR_DQS_P4_504	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
PS_DDR_DQS_N4_504	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
PS_DDR_DQS_P5_504	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
PS_DDR_DQS_N5_504	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
PS_DDR_DQS_P6_504	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
PS_DDR_DQS_N6_504	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
PS_DDR_DQS_P7_504	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
PS_DDR_DQS_N7_504	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
PS_DDR_DQS_P8_504	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
PS_DDR_DQS_N8_504	T27	PS_DDR_DQS_N8_504	PS_DDR_DM8_504

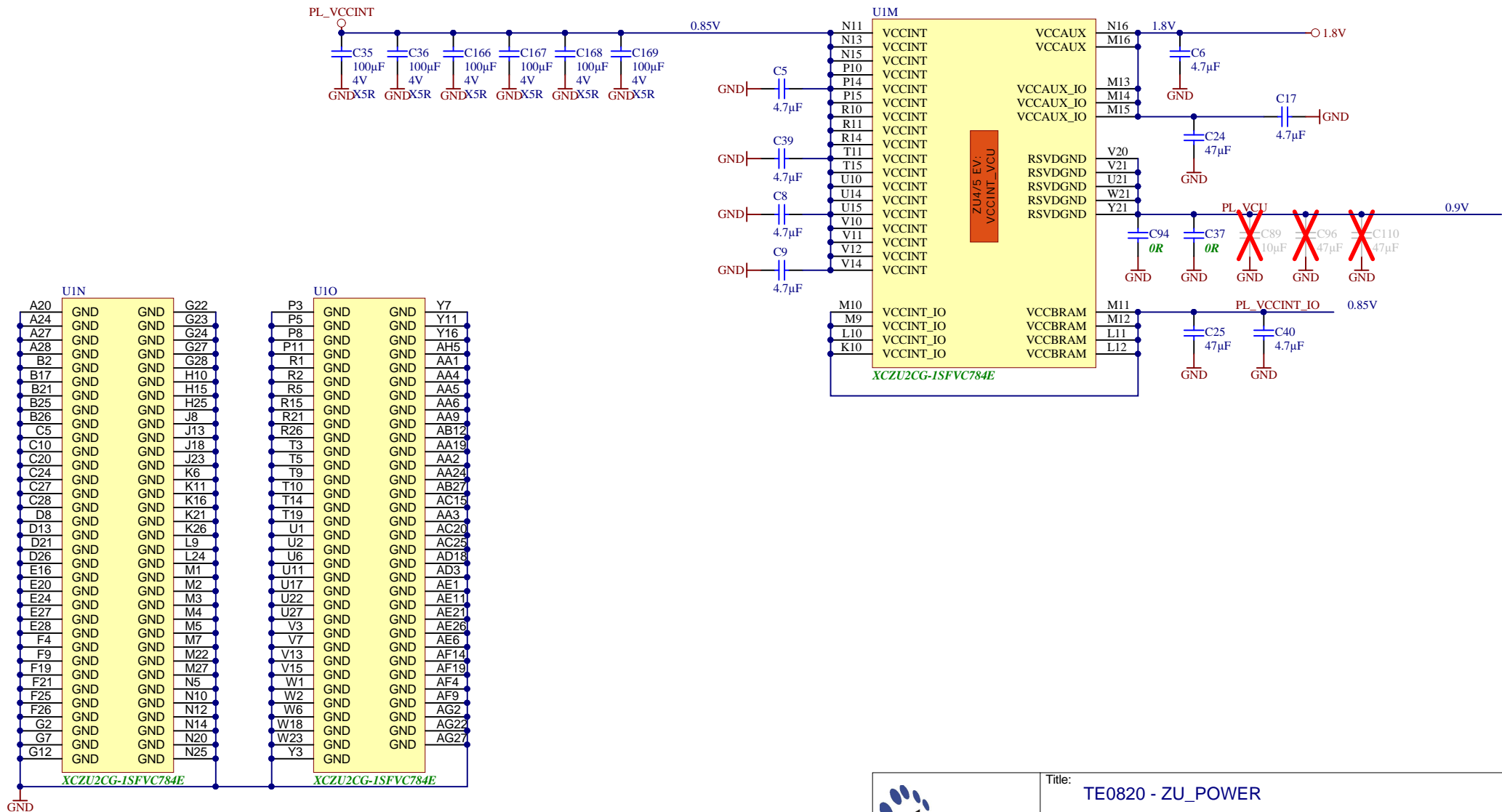
XCZU2CG-1SFVC784E



Title: TE0820 - PS_DDR		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 9 of 21
Filename: PS_DDR.SchDoc		



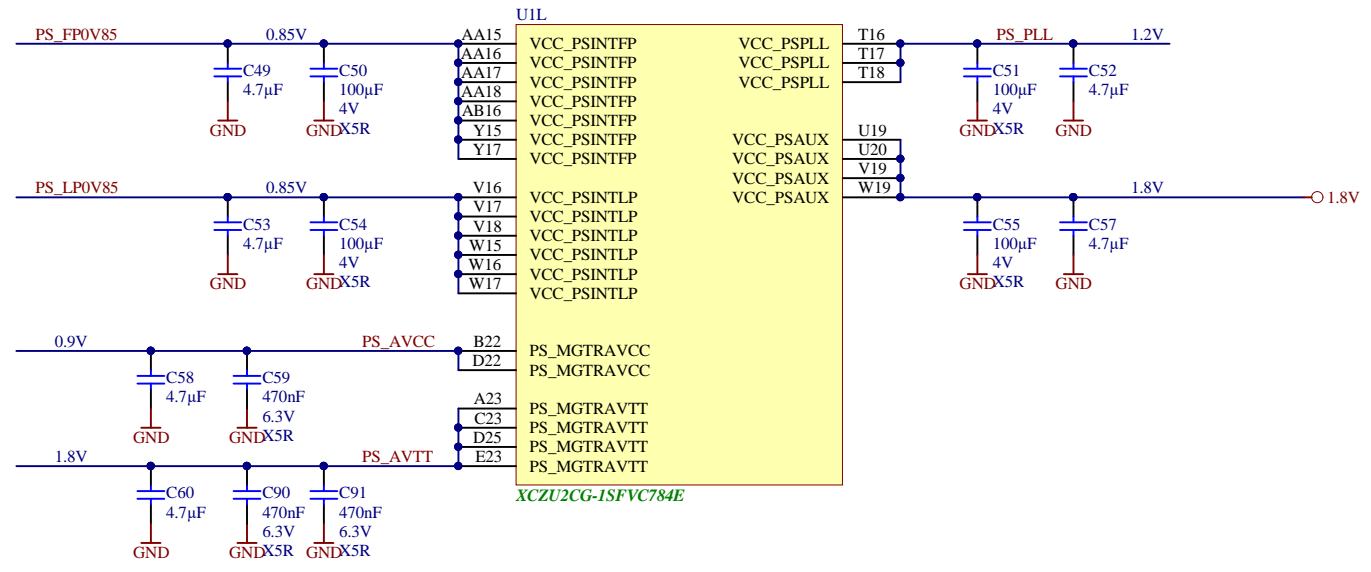
	Title: TE0820 - PS_GT		
	A4	Number: TE0820 02CG-1ED	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 10 of 21
	Filename: B_PS_GT.SchDoc		




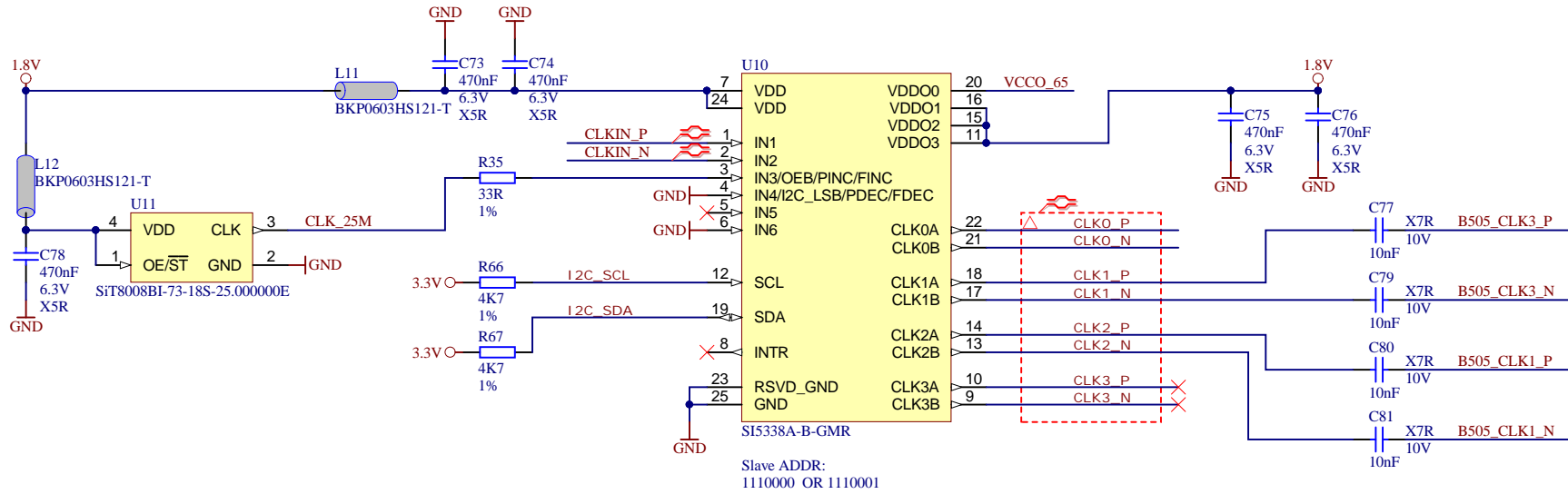
U1N				U1O				Y7			
A20	GND	GND	G22	P3	GND	GND	Y11				
A24	GND	GND	G24	P5	GND	GND	Y16				
A27	GND	GND	G27	P8	GND	GND					
A28	GND	GND	G28	P11	GND	GND	AH5				
B2	GND	GND	H10	R1	GND	GND	AA1				
B17	GND	GND	H10	R2	GND	GND	AA4				
B21	GND	GND	H15	R5	GND	GND	AA5				
B25	GND	GND	H25	R15	GND	GND	AA6				
B26	GND	GND	J8	R21	GND	GND	AA9				
C5	GND	GND	J13	R26	GND	GND	AB12				
C10	GND	GND	J18	T3	GND	GND	AA19				
C20	GND	GND	J23	T5	GND	GND	AA2				
C24	GND	GND	K6	T9	GND	GND	AA24				
C27	GND	GND	K11	T10	GND	GND	AB27				
C28	GND	GND	K16	T14	GND	GND	AC15				
D8	GND	GND	K21	T19	GND	GND	AA3				
D13	GND	GND	K26	U1	GND	GND	AC20				
D21	GND	GND	L9	U2	GND	GND	AC25				
D26	GND	GND	L24	U6	GND	GND	AD18				
E16	GND	GND	M1	U11	GND	GND	AD3				
E20	GND	GND	M2	U17	GND	GND	AE1				
E24	GND	GND	M3	U22	GND	GND	AE11				
E27	GND	GND	M4	U27	GND	GND	AE21				
E28	GND	GND	M5	V3	GND	GND	AE26				
F4	GND	GND	M7	V7	GND	GND	AE6				
F9	GND	GND	M22	V13	GND	GND	AF14				
F19	GND	GND	M27	V15	GND	GND	AF19				
F21	GND	GND	N5	W1	GND	GND	AF4				
F25	GND	GND	N10	W2	GND	GND	AF9				
F26	GND	GND	N12	W6	GND	GND	AG2				
G2	GND	GND	N14	W18	GND	GND	AG22				
G7	GND	GND	N20	W23	GND	GND	AG27				
G12	GND	GND	N25	Y3	GND	GND					




Title: TE0820 - ZU_POWER		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 11 of 21
Filename: ZU_POWER.SchDoc		



	Title: TE0820 - ZU_PS_POWER		
	A4	Number: TE0820 02CG-1ED	Rev. 03
	Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 12 of 21
	Filename: ZU_PS_POWER.SchDoc		



	Title: TE0820 - CLK		
	A4	Number: TE0820 02CG-1ED	Rev. 03
	Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 13 of 21
	Filename: CLK.SchDoc		

A

B

C

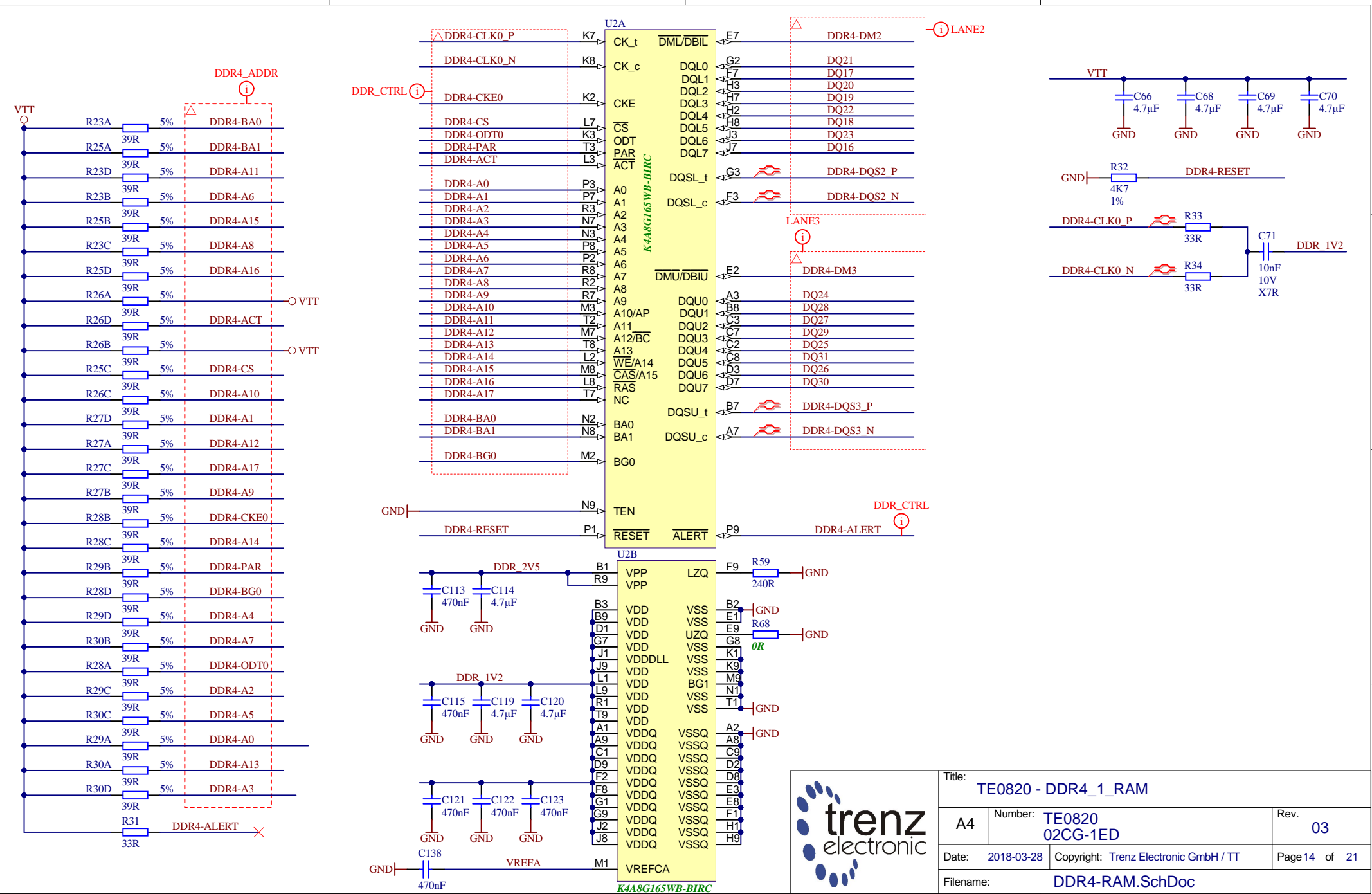
D

A

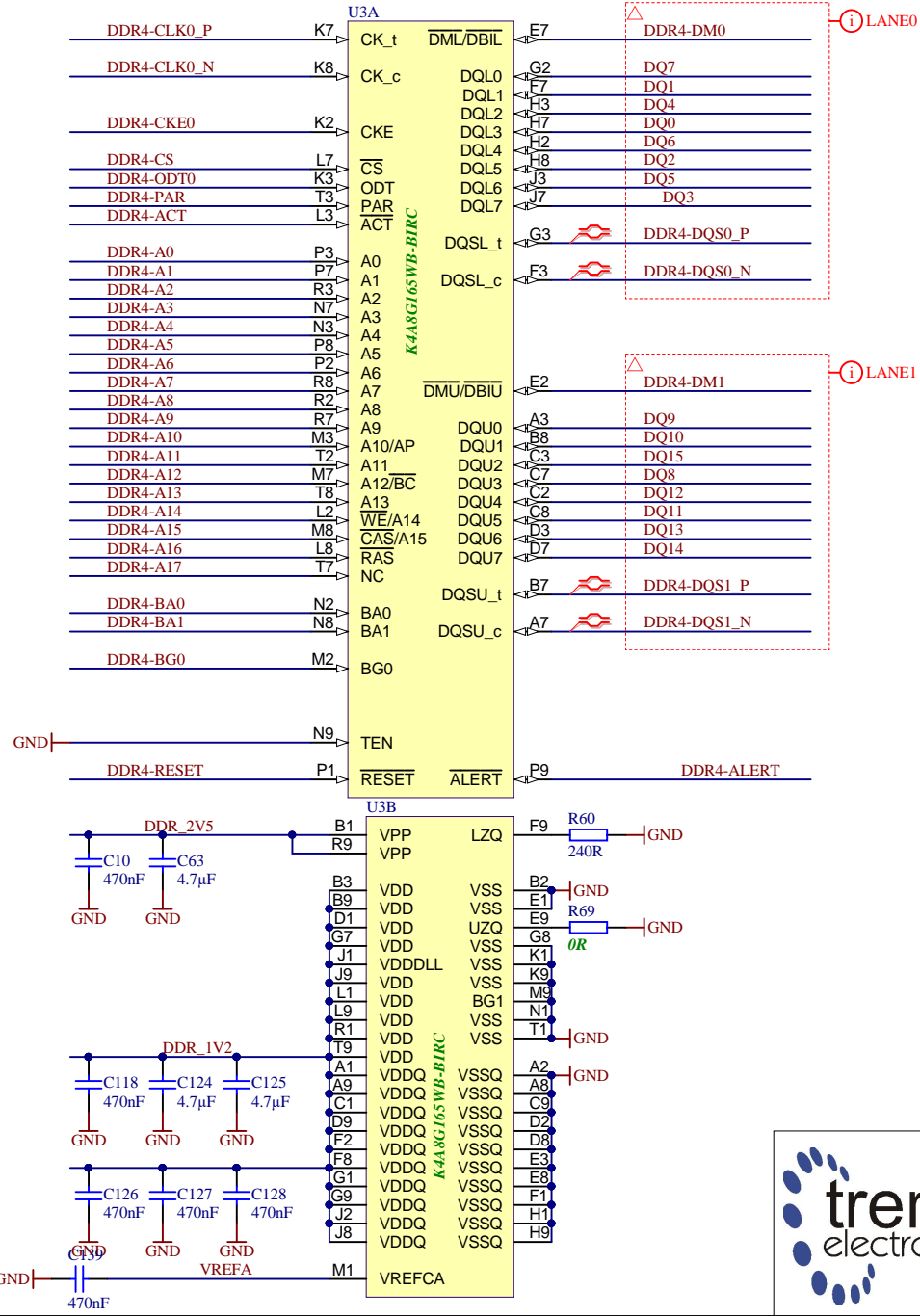

B

C

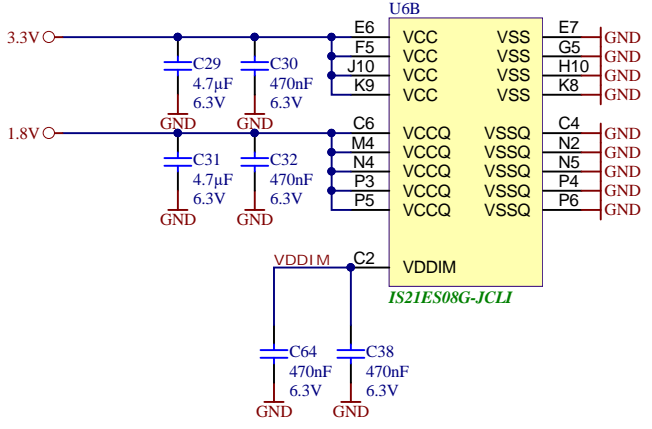
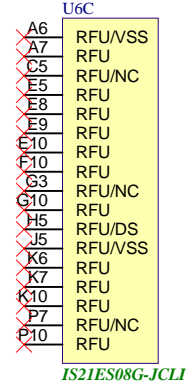
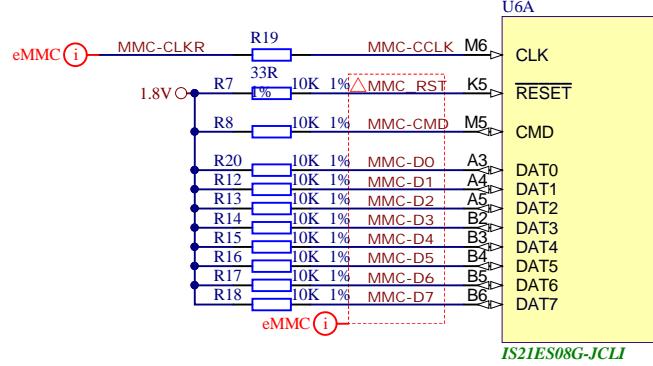
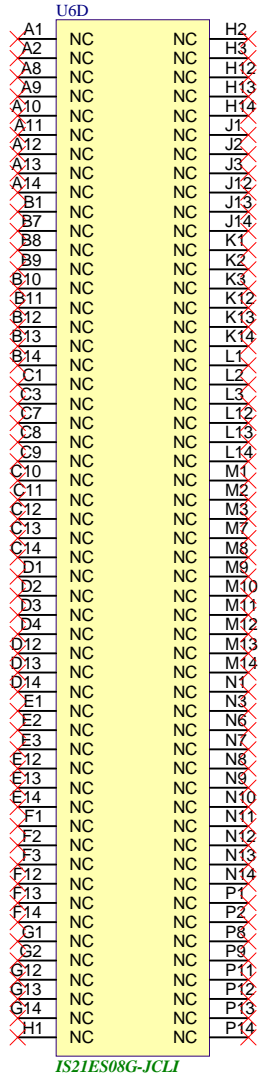
D



Title: TE0820 - DDR4_1_RAM		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 14 of 21
Filename: DDR4-RAM.SchDoc		

Title: TE0820 - DDR4_2_RAM		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 15 of 21
Filename: DDR4-RAM_2.SchDoc		



Title: TE0820 - eMMC		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 16 of 21
Filename: eMMC.SchDoc		

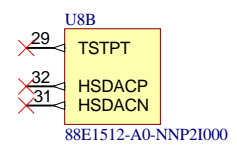
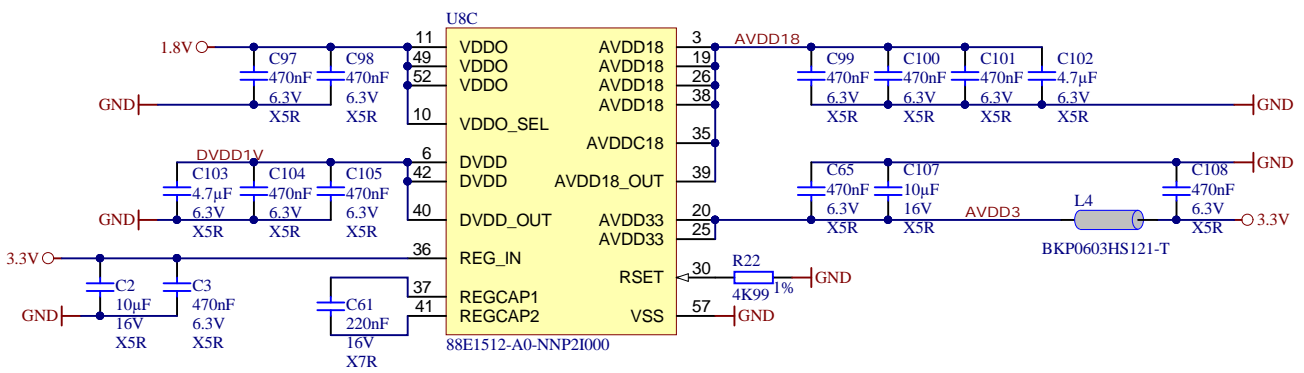
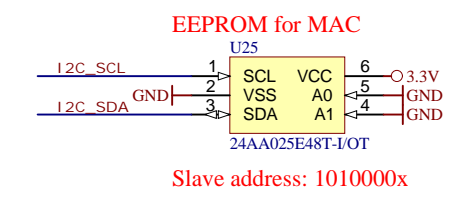
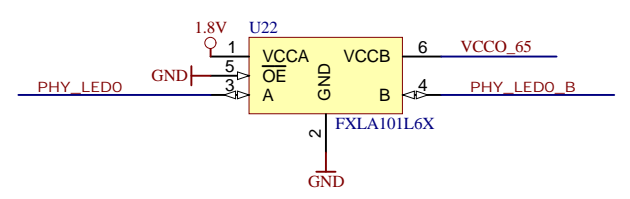
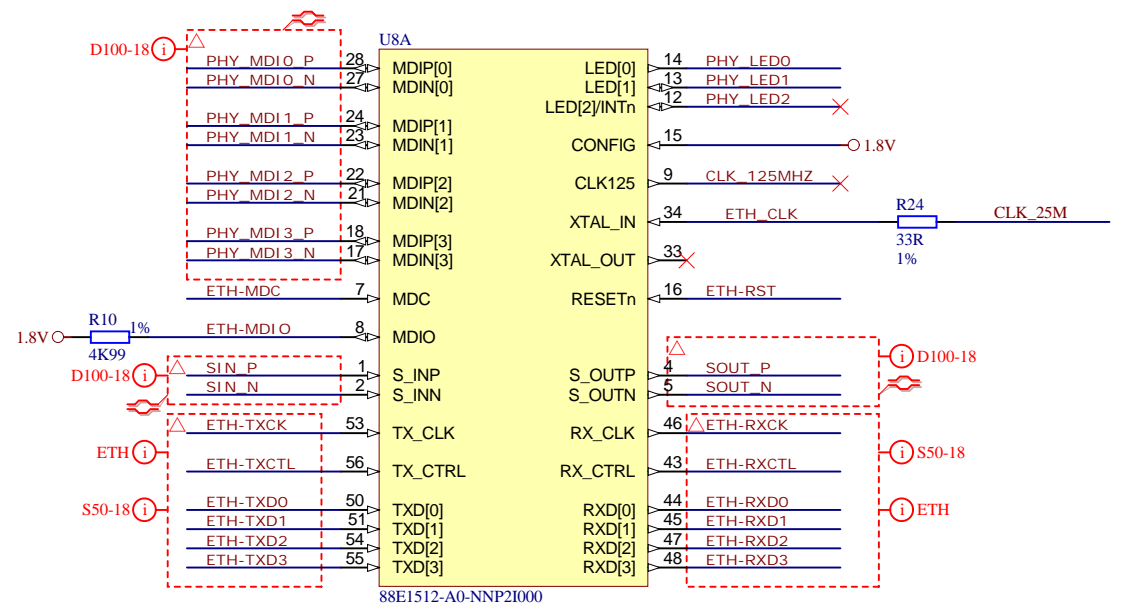


A

B

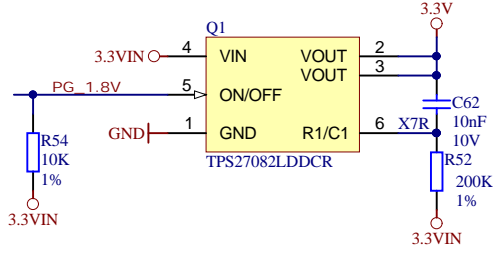
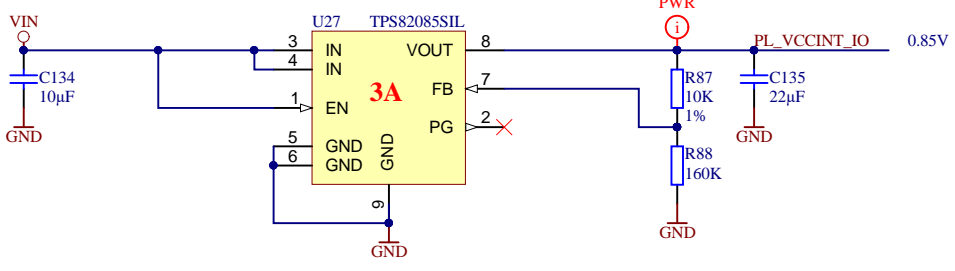
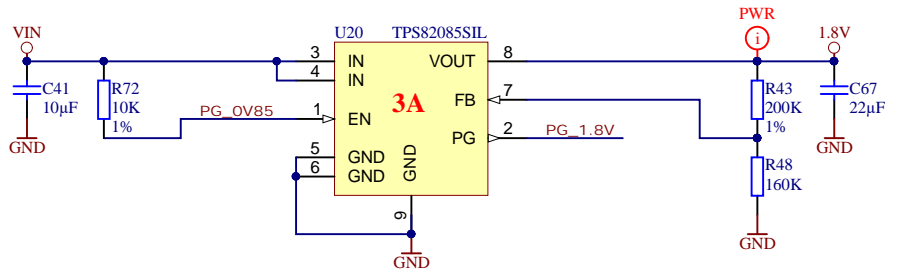
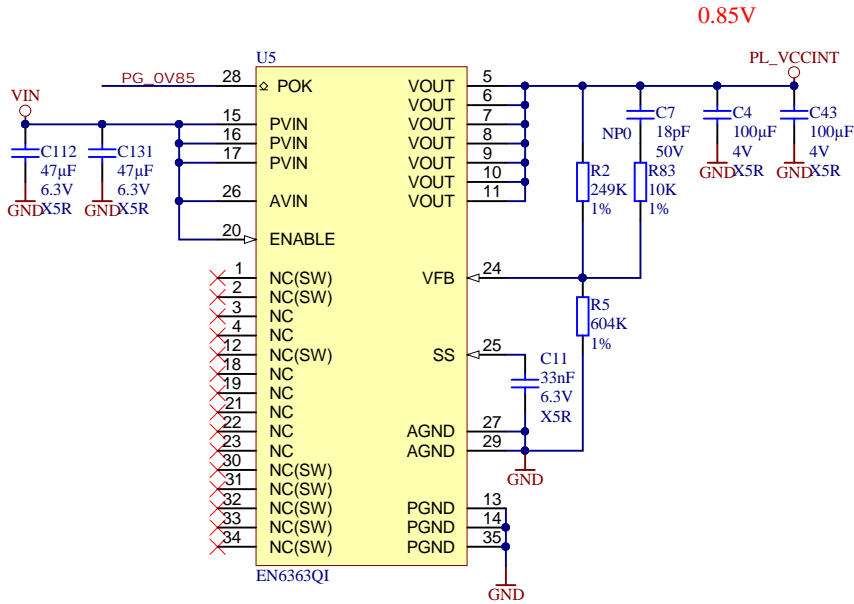
C

D

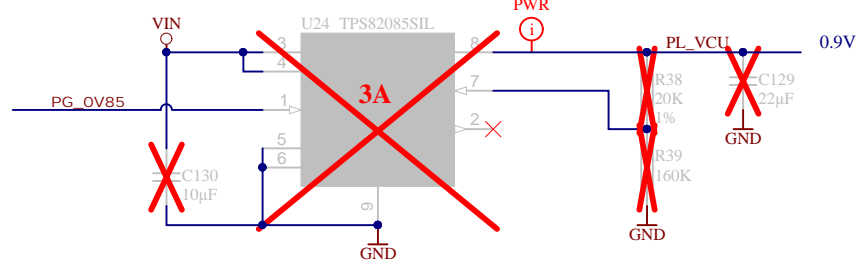


Title: TE0820 - Eth_PHY		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: 2015 Trenz Electronic GmbH	Page 17 of 21
Filename: ETH-PHY.SchDoc		

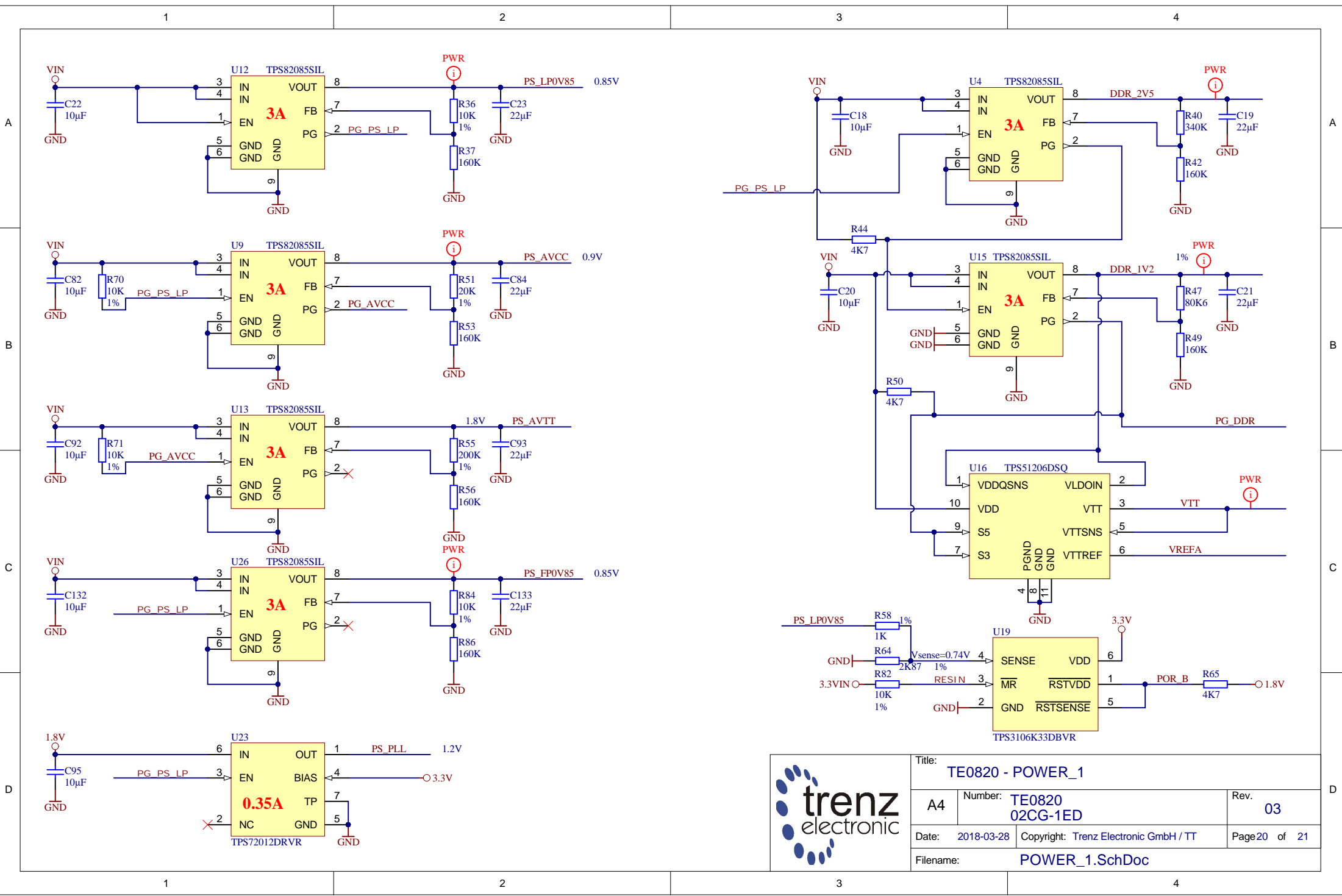





NOTE: in variants with VCU R38 was 40.2K, this has been corrected to 20K (Xilinx documentation DS925) for further details just see Design Note Number: DN-20200904  
<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>



Title: TE0820 - POWER		
A4	Number: TE0820 02CG-1ED	Rev. 03
Date: 2018-03-28	Copyright: Trenz Electronic GmbH / TT	Page 19 of 21
Filename: POWER.SchDoc		



			Title: TE0820 - POWER_1	
			A4	Number: TE0820 02CG-1ED
Date: 2018-03-28		Copyright: Trenz Electronic GmbH / TT		Page 20 of 21
Filename: POWER_1.SchDoc				


CHANGES REV01 to REV02

- 1) Added MAC EEPROM (slave address:)
- 2) LIB components update
- 3) Fixed SD Card connection
- 4) Fixed sense connection from DCDC
- 5) Made correct power connection for VCU (removed DCDC, added resistors and caps like as Xilinx recommended)
- 6) Added resistors for variants (ZU+ with/without VCU)
- 7) Added termination resistors (240R) to VRP pins fro all HP-banks

CHANGES REV02 to REV03

- 1) Fixed VCU connection: add additional DCDC (0.9V)
- 2) LIB components update
- 3) Change package 1K resistors (0402 -> 0201)
- 4) Added LEDs (1x user LED, 1x LED for ERR\_STATUS, 1xLED for ERR\_OUT)
- 5) Change obsolete 2xSPI Flash (256MBit) -> 2xSPI Flash (512MBit)
- 6) Added additional DCDCs (PL\_VCCINT\_IO, PS\_FP0V85)
- 7) Changed DCDC (U5) 6A (optional 4A)

Design Note Number: DN-20200904 (<https://wiki.trenz-electronic.de/display/PD/Design+Note+TE0820-03+with+Video+Codec+++EV>)  
 The internal supply voltage for the video codec unit (VCU) is set via Resistors R38 and R39. For the above mentioned affected SoMs R38 is set to 40.2 kOhm resulting in a PL\_VCU voltage of 1.0V. This is above the recommended operation specification.  
 Up to the issue date of this design note no adverse effects have been reported. For all serial numbers not mentioned under affected products R38 is 20 kOhm resulting in xilinx recommended 0.9V internal VCU voltage.  
 If your product is affected and revision is required please contact sales@trenz-electronic.de (subject = DN-20200904) for further instructions.

		Title: <b>TE0820 - Revision Changes</b>		
		A4	Number: <b>TE0820 02CG-1ED</b>	Rev. <b>03</b>
		Date: <b>2018-03-28</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>21</b> of <b>21</b>
		Filename: <b>Revision Changes.SchDoc</b>		