



Product Change Notification / SYST-27MDVE453

Date:

28-Jul-2022

Product Category:

Ethernet Switches

PCN Type:

Document Change

Notification Subject:

Data Sheet - KSZ8563R 3-Port 10/100 Ethernet Switch with RGMII/MII/RMII Interface and IEEE 1588v2 - Data Sheet

Affected CPNs:

[SYST-27MDVE453_Affected_CPN_07282022.pdf](#)
[SYST-27MDVE453_Affected_CPN_07282022.csv](#)

Notification Text:

SYST-27MDVE453

Microchip has released a new Datasheet for the KSZ8563R 3-Port 10/100 Ethernet Switch with RGMII/MII/RMII Interface and IEEE 1588v2 - Data Sheet of devices. If you are using one of these devices please read the document located at [KSZ8563R 3-Port 10/100 Ethernet Switch with RGMII/MII/RMII Interface and IEEE 1588v2 - Data Sheet](#).

Notification Status: Final

Description of Change: -Section 4.1.5, "Auto-Negotiation" Updated description from "mode" to "speed." Also added the following sentence: "With parallel detection, the duplex will always be half-duplex." -Section 4.1.5, "Auto-Negotiation" Updated description from "mode" to "speed." Also added the following sentence: "With parallel detection, the duplex will always be half-duplex." -Section 4.1.7, "LinkMD[®] Cable Diagnostics" Updated to add additional details and test script. Section 4.11.1, "Media Independent Interface (MII)" Updated description to remove half duplex operation. -Section 5.1.2.2, "In-Band Management (IBA) Control Register" Added the following note to bit 31: "If using I2C, do not enable IBA." -Section 5.1.3.2, "LED Strap-In Register" Changed definition from: "Strap-in values of Select RXD and LED pins [RXD2_1, RXD2_0, LED1_1, LED1_0]" to "Strap-in values of Select RXD and LED pins [RXD1, RXD0, LED1_1, LED1_0]". -Section 5.1.4.72, "Global PM Available Register" New register added for Packet Memory Available Block Count. -Section 5.1.5.3, "VLAN Table Entry 2 Register" Updated description of bits 2-0 from "1 = Untag packets upon egress at this port; 0 = Do not untag upon egress at this port" to "1 = Forward to this port; 0 = Do not forward to this port". -Section 5.1.6.1, "Global PTP Clock Control Register" Added the following note to bit 1: "The PTP Clock must be enabled when using the time stamp units (TSU) or trigger output units (TOU), even if IEEE 1588 is not implemented." -Section 5.1.6.21, "Trigger Output Unit Control 2 Register" Added the following note: "The minimum value for this parameter is 0x50." -Section 5.1.6.24, "Trigger Output Unit Control 5 Register" Removed the

following advisory: "This register contains the PTP event trigger output PPS signal pulse width for unit 2 and path delay compensation for unit 1." -Section 5.2.2.1, "PHY Basic Control Register" Updated bit 7 from "Collision Test" to "Reserved". Added the following note after bit 6: "Bit 6 must be set to 0 when auto-negotiation is disabled". -Section 5.2.2.1, "PHY Basic Control Register" Updated bit 10 default value from "0b" to "1b". -Section 5.2.2.2, "PHY Basic Status Register" Updated bit 0 default from "0" to "1". -Section 5.2.2.4, "PHY ID Low Register" Updated value from "0x1631" to "0x1637". -Section 5.2.2.18, "Port Special Register" Added register. -Section 5.2.7.4, "Port Authentication Control Register" Updated bit 2 definition from "1 = Enable; 0 = Enable" to "1 = Enable; 0 = Disable". -Section 5.2.9.2, "Port Control 1 Register" Updated address range from "0xNA04 - 0xNA03" to "0xNA04 - 0xNA07". Updated type from "RO" to "RW". Updated default value of bits 2-0 from "0b" to "1b". -Section 5.2.9.3, "Port Transmit Queue Memory Register" Added register. -Section 5.4.1, "MMD LED Mode Register" Added the following text to bit 4: "For Single-LED mode, set this bit and also set bit 9 in register 0xN13C-0xN13D." -Table 5-7, "MMD Register Map" Updated example of MMD Register Read from: "Register 11h - 13h for the LED mode status" to "Register 00h for the MMD LED Mode Register." -Table 3-3, "Configuration Strap Descriptions" Added the following note to LED1_1: "If using I2C, do not enable IBA." -Table 4.8.5, "Energy Efficient Ethernet (EEE)" Corrected "disabled by default" to "enabled by default". Additionally, added the following sentence: "EEE is enabled or disabled in the MMD EEE Advertisement register." -Section 5.4.2, "MMD EEE Advertisement Register" Changed Bit 2 definition: from "1000BASE-T EEE Enable; 1 = 1000 Mbps EEE capable; 0 = No 1000 Mbps EEE capability" to "Always set bit 2 to the same value as bit 10." -Table 4-6, "Tail Tag Frame Format" Updated byte number for Tail Tagging from "2" to "1". -Table 3-2, "Pin Descriptions" For Power Management Event PME_N, updated buffer type from "IPU/O8" to "I/O8" and added the following note: "An external pull-up or pull-down resistor is required to set the desired strapping level." -Table 3-2, "Pin Descriptions" Updated pin RX_ER so that RMII mode is with MII mode. -Table 3-3, "Configuration Strap Descriptions" Updated RX_ER, PME_N description to remove "Default" from bit 1 and added the following note: "Note that PME_N does not have an internal pullup or pull-down, so an external pull-up or pull-down resistor is always required." -Table 6-12, "Power-up and Reset Timing Values" Updated Note 3 to indicate the following: "The power supplies may be powered down in any sequence."

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 28 Jul 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[KSZ8563R 3-Port 10/100 Ethernet Switch with RGMII/MII/RMII Interface and IEEE 1588v2 - Data Sheet](#)

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Affected Catalog Part Numbers (CPN)

KSZ8563RNXI

KSZ8563RNXI-TR

KSZ8563RNXV

KSZ8563RNXV-TR

KSZ8563RNXV-TRVAO

KSZ8563RNXV-VAO