MX25V2033F

2.3V-3.6V, 2M-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- 2.3V-3.6V *for Read, Erase and Program Operations*
- *Unique ID Data (UID) Support*
- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Additional 4K bits secured OTP*
- *HOLD FEATURE*

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2.3V-3.6V 2M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 2,097,152 x 1 bit structure or 1,048,576 x 2 bits (two I/O mode) structure or 524,288 x 4 bits (four I/O mode)structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K/64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - Operation Voltage: 2.3V-3.6V for Read, Erase and Program Operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Status Register Feature
- Command Reset
- Program/Erase Suspend and Program/Erase Resume
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Unique ID (Please contact local Macronix for detailed information)

PERFORMANCE

- High Performance
  - Fast Read:
    - 1 I/O:
      80MHz with 8 dummy cycles (2.7V-3.6V)
      50MHz with 8 dummy cycles (2.3V-2.7V)
    - 2 I/O:
      80MHz with 4 dummy cycles (2.7V-3.6V)
      50MHz with 4 dummy cycles (2.3V-2.7V)
    - 4 I/O:
      60MHz with 4 dummy cycles (2.7V-3.6V)
      33MHz with 4 dummy cycles (2.3V-2.7V)
  - Fast program time: 1ms /page (256-byte)
  - Byte program time: 30us
  - Fast erase time:
    50ms(typ.)/sector (4K-byte per sector);
    0.3s(typ.)/block (32K-byte per block);
    0.6s(typ.)/block (64K-byte per block);
    2s(typ.)/chip.
- Low Power Consumption
- Minimum 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
  The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
- Additional 4K bits secured OTP
  - Features unique identifier.
  - Factory locked identifiable and customer lockable
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- HOLD#/SIO3
  - HOLD feature, to pause the device without deselecting the device or Serial input & Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (150mil)
  - 8-land USON (2x3mm)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25V2033F is 2Mb bits Serial NOR Flash memory, which is configured as 262,144 x 8 internally. When it is in four I/O mode, the structure becomes 524,288 bits x 4 or 1,048,576 bits x 2.

MX25V2035F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25V2033F MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

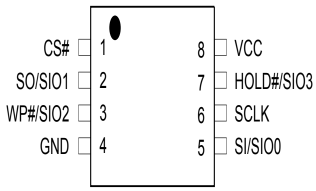
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

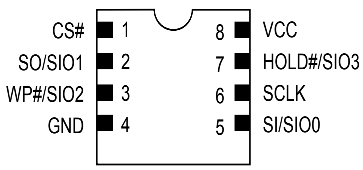
The MX25V2033F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

3. PIN CONFIGURATIONS

8-PIN SOP (150mil)



8-LAND USON (2x3mm)

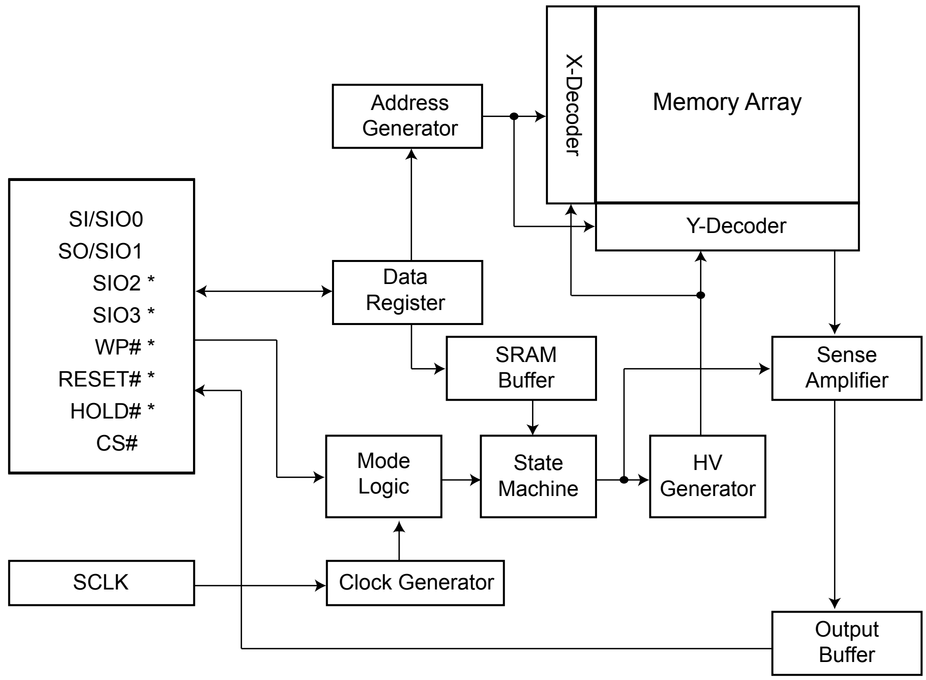


4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
HOLD#/SIO3	To pause the device without deselecting the device or Serial Data Input & Output (for 4xI/O read mode)
VCC	Power Supply
GND	Ground

Note: The pin of HOLD#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration. However, the internal pull up function will be disabled if the system has physical connection to HOLD#/SIO3 or WP#/SIO2 pin.

5. BLOCK DIAGRAM



* Depends on part number options.

6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except toggling the CS#. For more detail please see *"10-20. Deep Power-down (DP)"*.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

  I. Block lock protection
  \- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 1. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

  \- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect (SRWD) bit. If the system goes into four I/O mode, the feature of HPM will be disabled.

Table 1. Protected Area Sizes

Status bit				Protect Level	Density	2Mb	Portion	Sector
BP3	BP2	BP1	BP0					
X	X	0	0	0 (None)	0	None	None	None
0	X	0	1	1 (1 block)	64KB	Block 3rd	Upper 1/4	Sector 48th-63rd
0	X	1	0	2 (2 blocks)	128KB	Block 2nd-3rd	Upper 1/2	Sector 32nd-63rd
1	X	0	1	3 (1 block)	64KB	Block 0th	Lower 1/4	Sector 0th-15th
1	X	1	0	4 (2 blocks)	128KB	Block 0th-1st	Lower 1/2	Sector 0th-31st
X	X	1	1	5 (4 blocks)	256KB	All	All	All

Note: X means “Don’t Care”

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker.

- Security register bit 0 indicates whether the secured OTP area is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 8. Security Register Definition"* for security register bit definition and *"Table 2. 4K-bit Secured OTP Definition"* for address range definition.

Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 2. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000-xxx1FF	4096-bit	Determined by Factory	Determined by customer

7. MEMORY ORGANIZATION

Table 3. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
3	7	63	03F000h	03FFFFh
	|	:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
	|	:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
	|	:	:	:
	2	16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
	|	:	:	:
	0	2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

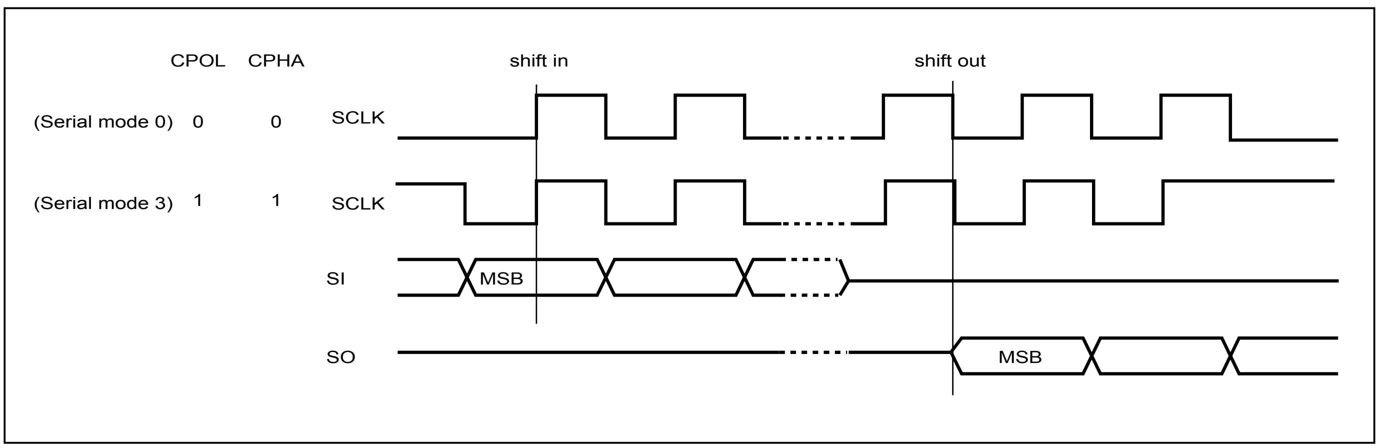
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, DREAD, 2READ, 4READ, QREAD, RES, REMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, SUSPEND, RESUME, RSTEN, RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

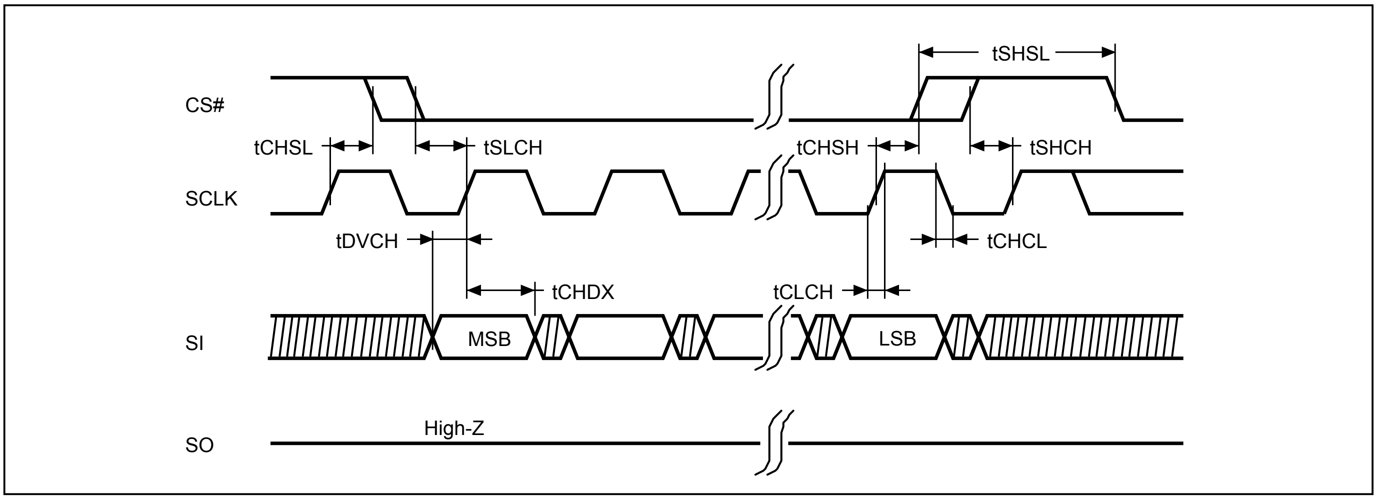


Figure 3. Output Timing

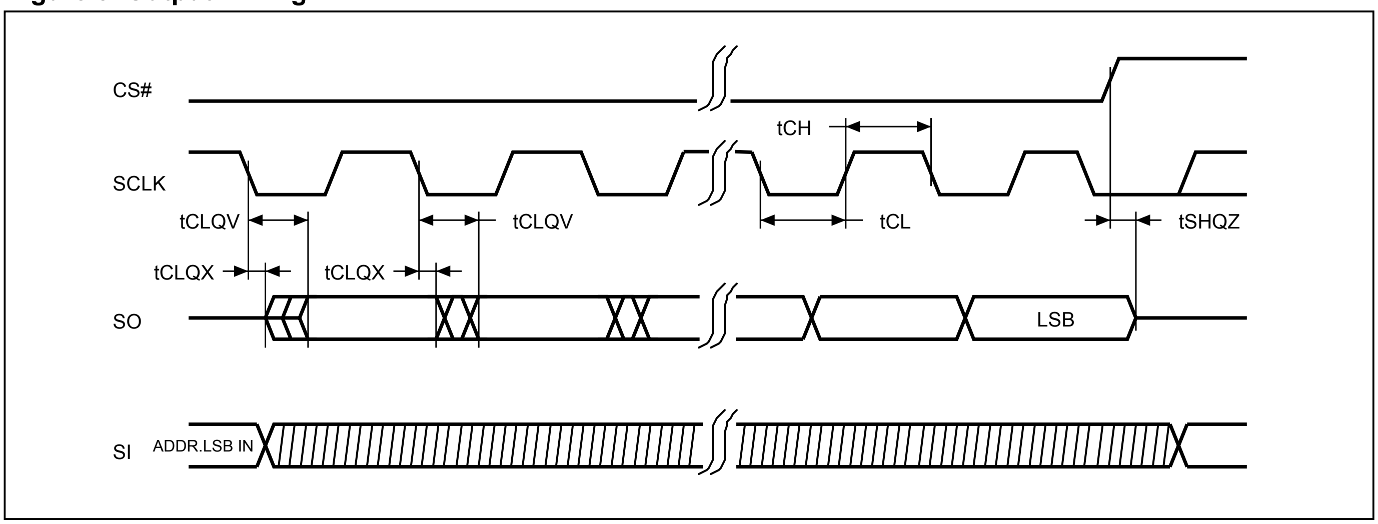
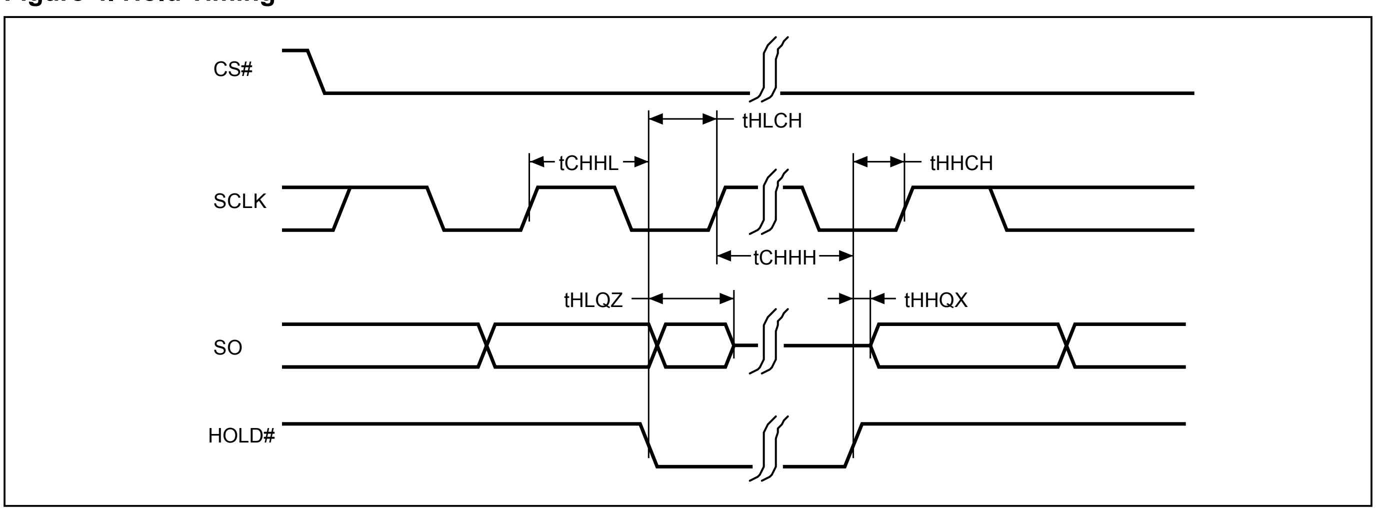


Figure 4. Hold Timing



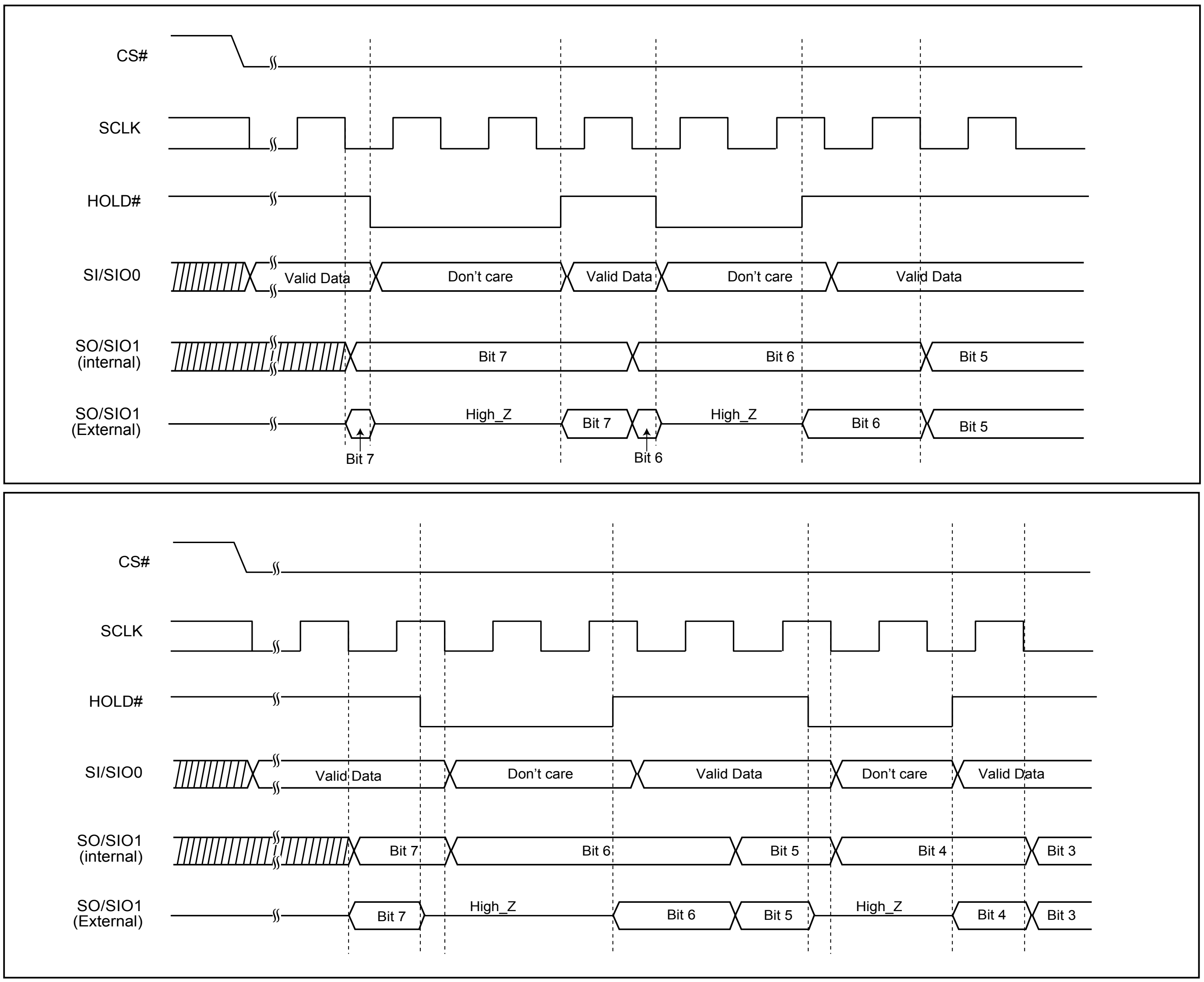
* SI is "don't care" during HOLD operation.

9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure 5. Hold Condition Operation



During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.

10. COMMAND DESCRIPTION

Table 4. COMMAND DESCRIPTION

	COMMAND (byte)	I/O	1st byte	2nd byte	3rd byte	4th byte	5th byte	Action
Read/Write Array	**READ (Normal Read)**	1	03 (hex)	ADD1	ADD2	ADD3		n bytes read out until CS# goes high
	Fast Read (Fast Read Data)	1	0B (hex)	ADD1	ADD2	ADD3	Dummy	n bytes read out until CS# goes high
	DREAD (1 x I / 2O Read Command)	2	3B (hex)	ADD1	ADD2	ADD3	Dummy	
	2READ (2 x I/O Read Command)	2	BB (hex)	ADD1	ADD2	ADD3	Dummy	n bytes read out by 2 x I/O until CS# goes high
	QREAD (1 x I / 4O Read Command)	4	6B (hex)	ADD1	ADD2	ADD3	Dummy	
	4READ (4 x I/O Read Command)	4	EB (hex)	ADD1	ADD2	ADD3	Dummy	n bytes read out by 4 x I/O until CS# goes high
	SE (Sector Erase)	1	20 (hex)	ADD1	ADD2	ADD3		Erase the selected sector
	BE 32K (Block Erase 32KB)	1	52 (hex)	ADD1	ADD2	ADD3		Erase the selected 32KB block
	BE (Block Erase 64KB)	1	D8 (hex)	ADD1	ADD2	ADD3		Erase the selected 64KB block
	CE (Chip Erase)	1	60 or C7 (hex)					Erase the whole chip
	PP (Page Program)	1	02 (hex)	ADD1	ADD2	ADD3		Program the selected page
	4PP (Quad Page Program)	4	38 (hex)	ADD1	ADD2	ADD3		Program the selected page
	READ UID	1	5A (hex)	ADD1	ADD2	ADD3	Dummy	Read UID
Register/ Setting	**WREN (Write Enable)**	1	06 (hex)					Set the (WEL) write enable latch bit
	WRDI (Write Disable)	1	04 (hex)					Reset the (WEL) write enable latch bit
	RDSR (Read Status Register)	1	05 (hex)					Read out the status register
	WRSR (Write Status Register)	1	01 (hex)	Values	Values			Write new values to the status register
	PGM/ERS Suspend (Suspends Program/ Erase)	1	75/B0 (hex)					program/erase operation is interrupted by suspend command
	PGM/ERS Resume (Resumes Program/ Erase)	1	7A/30 (hex)					to continue performing the suspended program/erase sequence
	DP (Deep Power- down)	1	B9 (hex)					Enter deep power down mode
	RDP (Release from deep power down)	1	AB (hex)					release from deep power down mode

	COMMAND (byte)	I/O	1st byte	2nd byte	3rd byte	4th byte	5th byte	Action
ID/Reset	**RDID (Read Identification)**	1	9F (hex)					Output manufacturer ID and 2-byte device ID
	RES (Read Electronic ID)	1	AB (hex)	x	x	x		Read out 1-byte Device ID
	REMS (Read Electronic Manufacturer & Device ID)	1	90 (hex)	x	x	ADD (Note 1)		Output the manufacturer ID and device ID
	ENSO (Entered Secured OTP)	1	B1 (hex)					to enter the 4K-bit secured OTP mode
	EXSO (Exit Secured OTP)	1	C1 (hex)					to exit the 4K-bit secured OTP mode
	RDSCUR (Read Security Register)	1	2B (hex)					to read value of security register
	WRSCUR (Write Security Register)	1	2F (hex)					to set the lockdown bit as "1" (once lockdown, cannot be updated)
	RSTEN (Reset Enable)	1	66 (hex)					
	RST (Reset Memory)	1	99 (hex)					*(Note 3)*

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 3: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

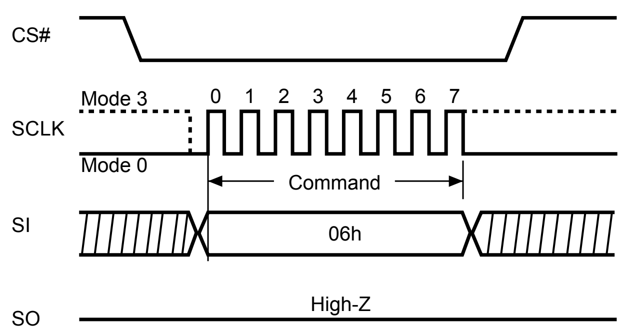
10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

The SIO[3:1] are "don't care" .

Figure 6. Write Enable (WREN) Sequence



10-2. Write Disable (WRDI)

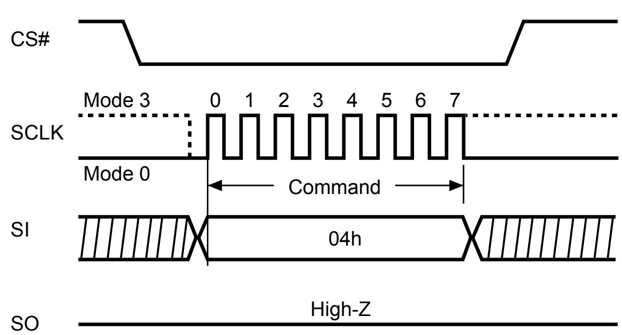
The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

The SIO[3:1] are "don't care".

The WEL bit is reset by following situations:
- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Program/Erase Suspend
- Completion of Softreset command
- Completion of Write Security Register (WRSCUR) command

Figure 7. Write Disable (WRDI) Sequence



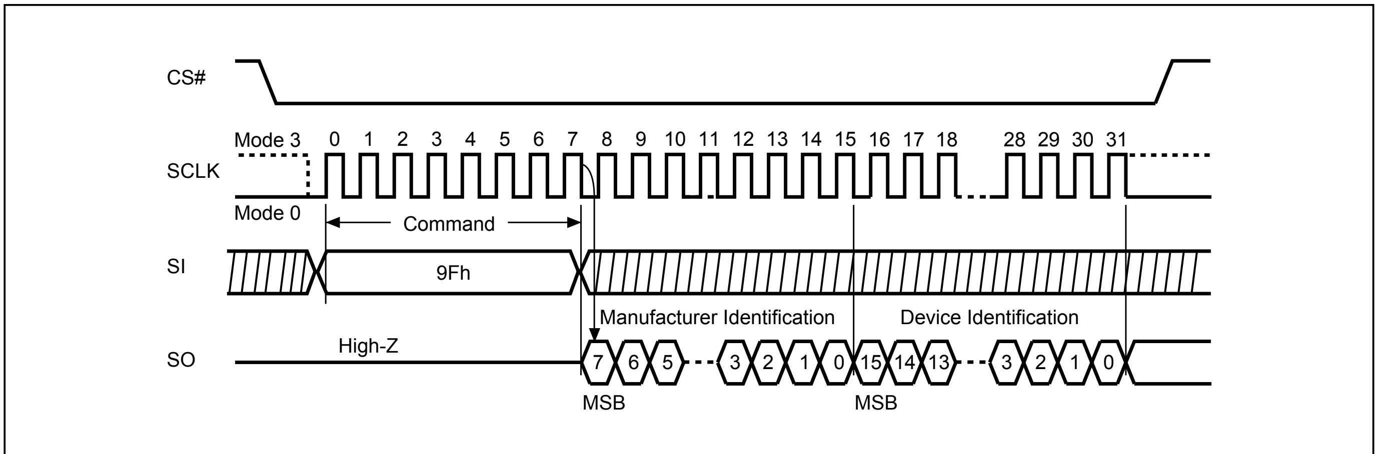
10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 5. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 8. Read Identification (RDID) Sequence

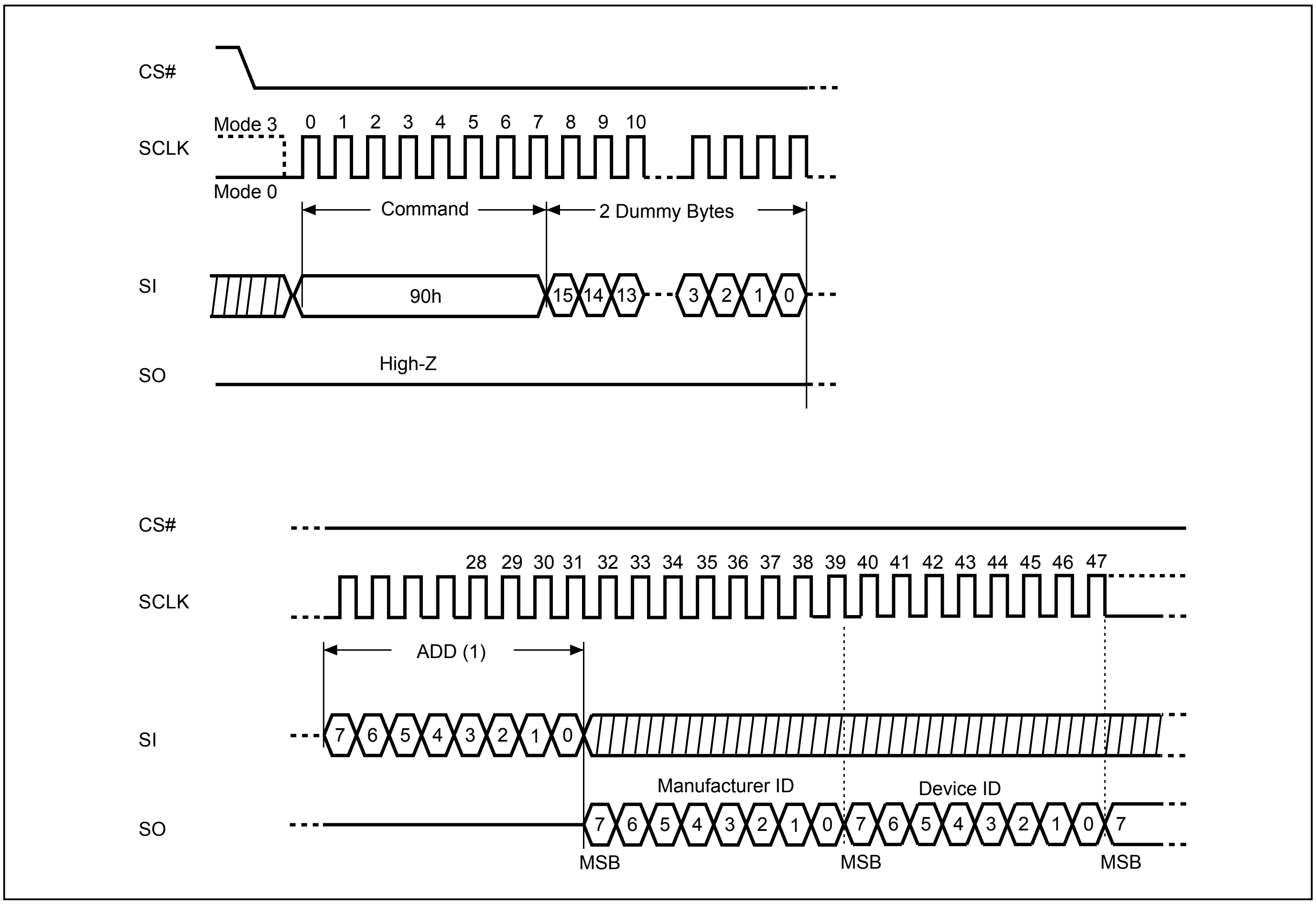


10-4. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *"Table 5. ID Definitions".*

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7-A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 9. Read Electronic Manufacturer & Device ID (REMS) Sequence



Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

10-5. ID Read

User can execute this ID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Table 5. ID Definitions

Command Type	MX25V2033F		
RDID	Manufacturer ID	Memory Type	Memory Density
	C2	20	12
RES	Electronic ID		
	11		
REMS	Manufacturer ID	Device ID	
	C2	11	

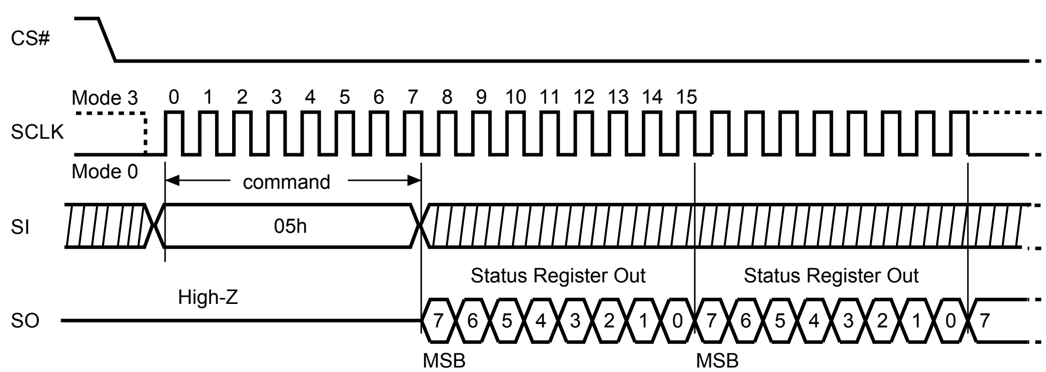
10-6. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

The SIO[3:1] are "don't care".

Figure 10. Read Status Register (RDSR) Sequence



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 11. Program/Erase flow with read array data

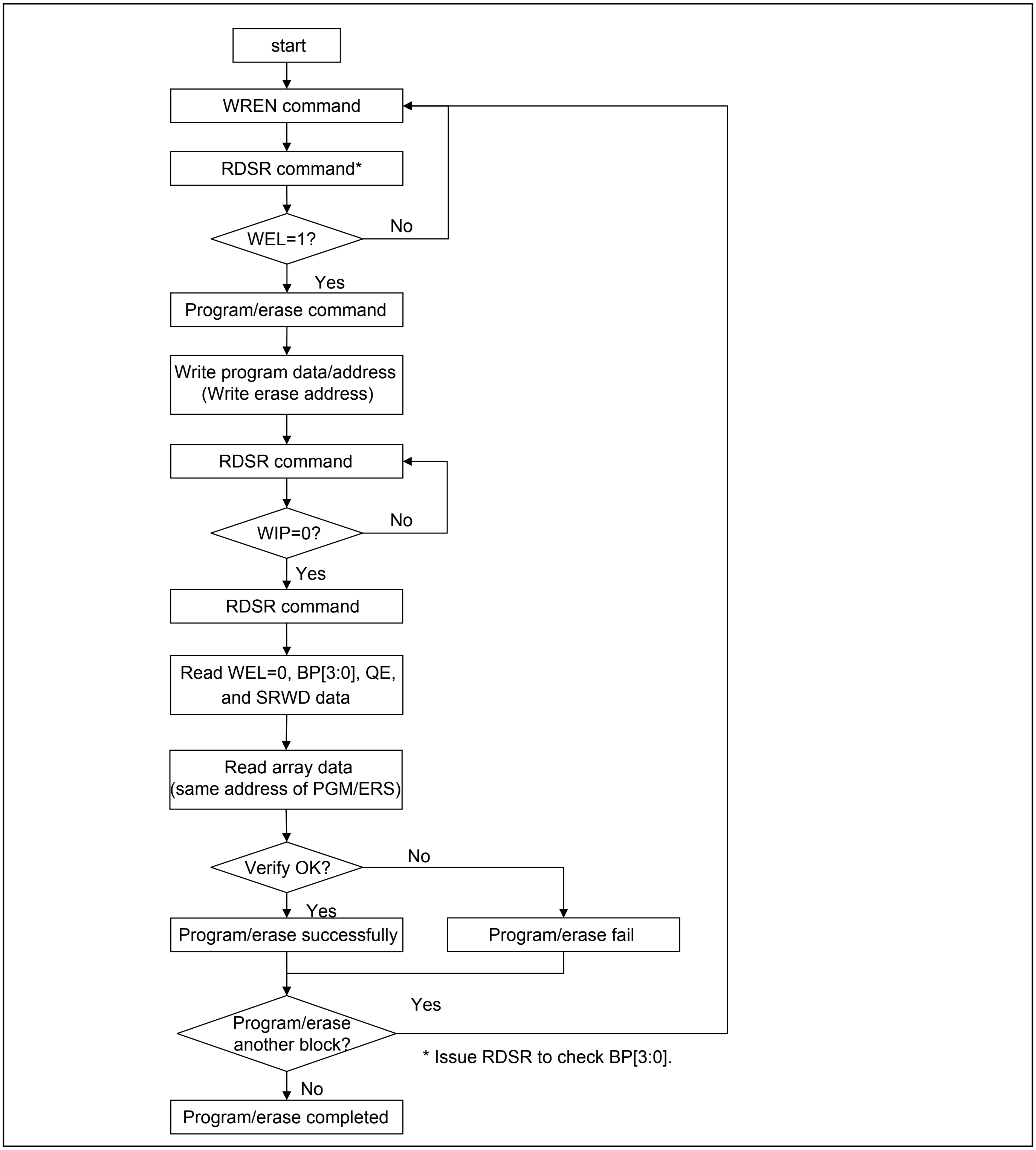
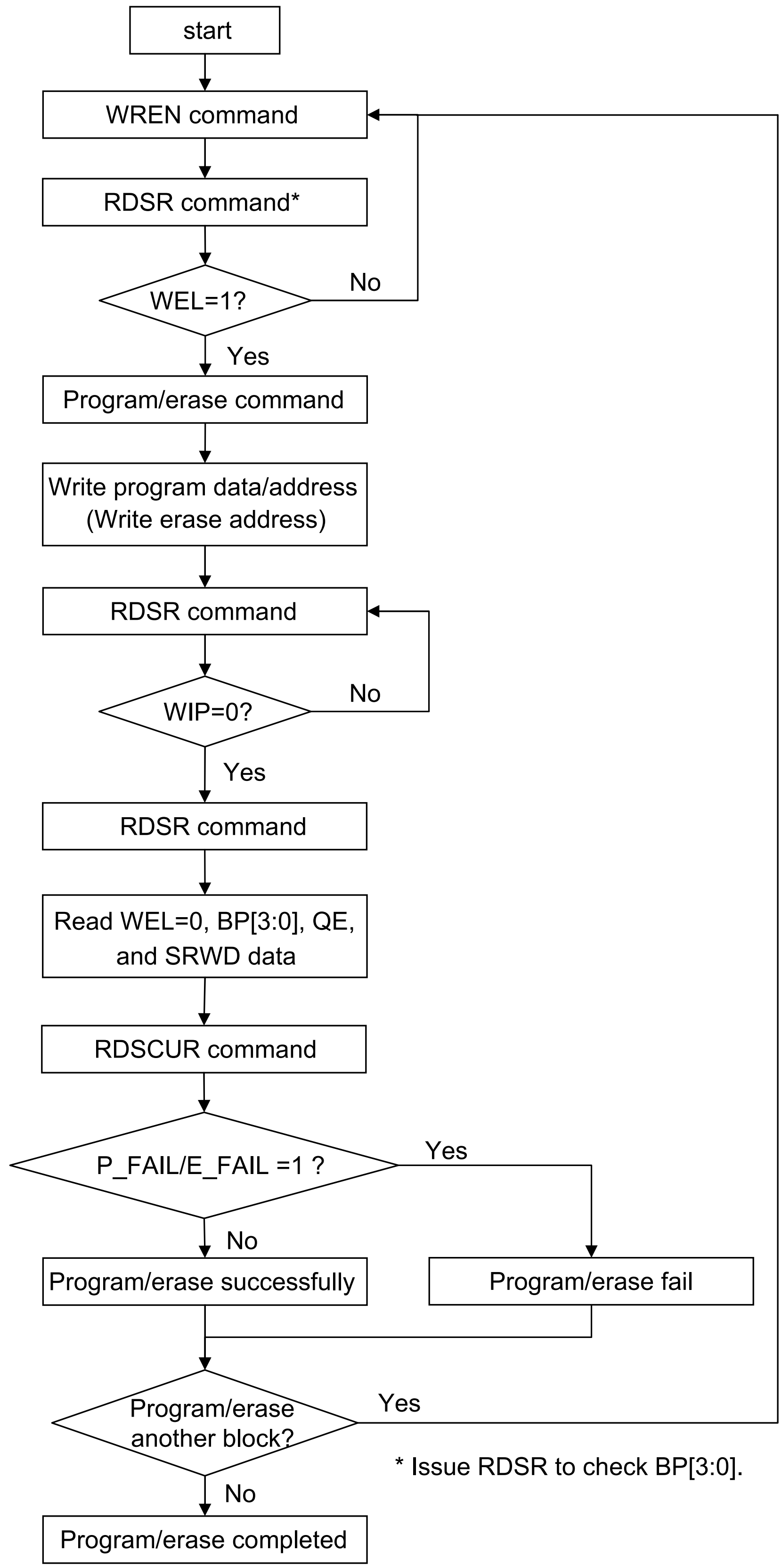


Figure 12. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to “1” by the WREN instruction. WEL needs to be set to “1” before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to “0” when a program or erase operation completes. To ensure that both WIP and WEL are “0” and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be “0” before checking that WEL is also “0”. If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to “0”.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 1. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE/BE32K) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default, which is un-protected.

QE bit. The Quad Enable (QE) bit is a non-volatile bit with a factory default of “0”. When QE is “0”, Quad mode commands are ignored; pins WP#/SIO2 and HOLD#/SIO3 function as WP# and HOLD#, respectively. When QE is “1”, Quad mode is enabled and Quad mode commands are supported along with Single and Dual mode commands. Pins WP#/SIO2 and HOLD#/SIO3 function as SIO2 and SIO3, respectively, and their alternate pin functions are disabled. Enabling Quad mode also disables the HPM and HOLD features.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 6. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disabled 0=status register write enabled	1=Quad Enabled 0=not Quad Enabled	*(note 1)*	*(note 1)*	*(note 1)*	*(note 1)*	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: Please refer to the *"Table 1. Protected Area Sizes"*.

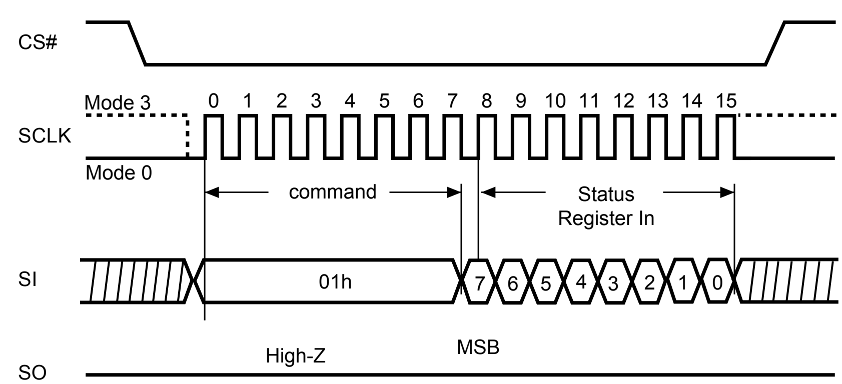
10-7. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 1. Protected Area Sizes"*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ send WRSR instruction code→ Status Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 13. Write Status Register (WRSR) Sequence



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note:
If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:
To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

Table 7. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be programmed or erased.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be programmed or erased.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 1. Protected Area Sizes"*.

Figure 14. WRSR flow

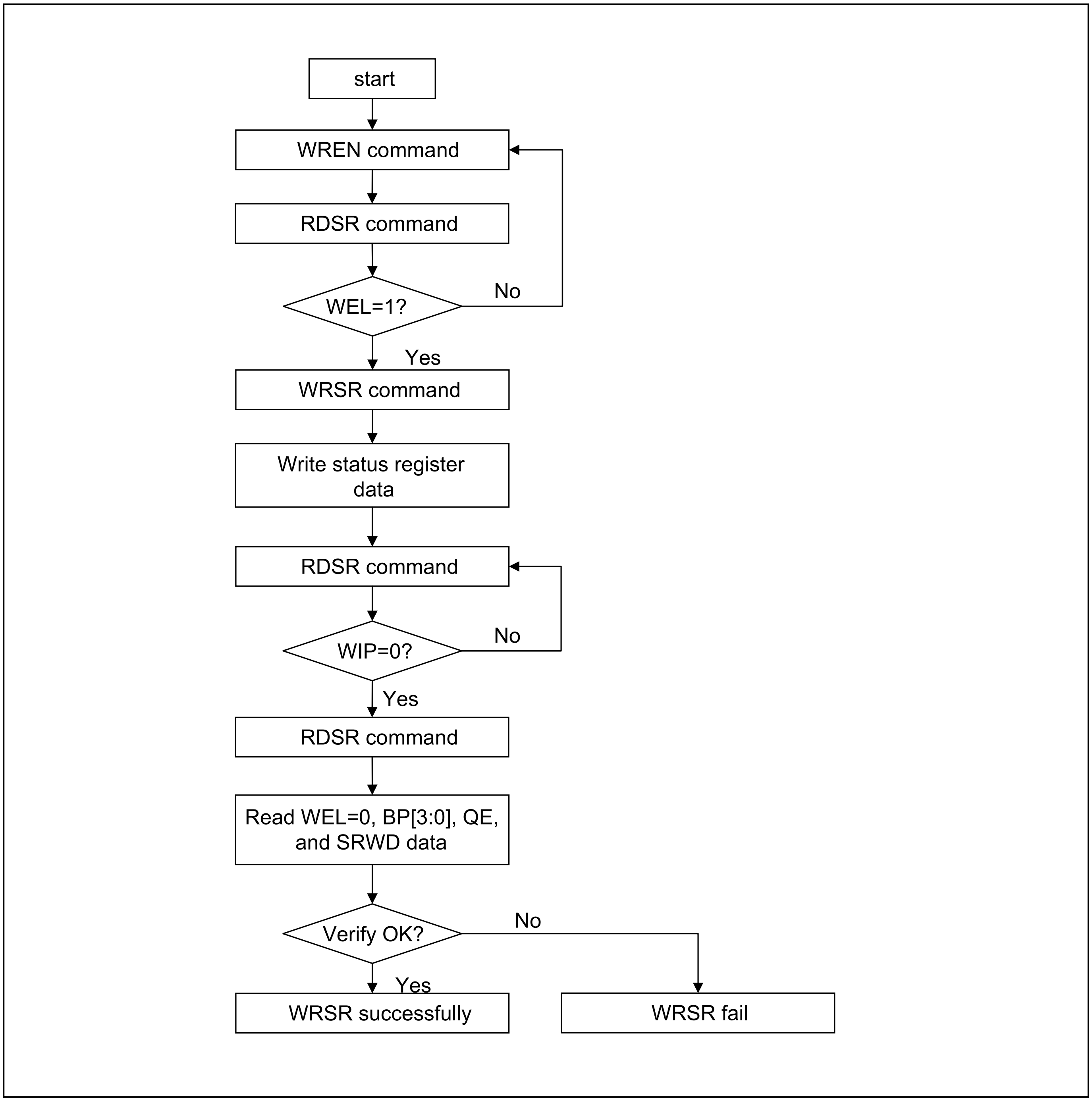
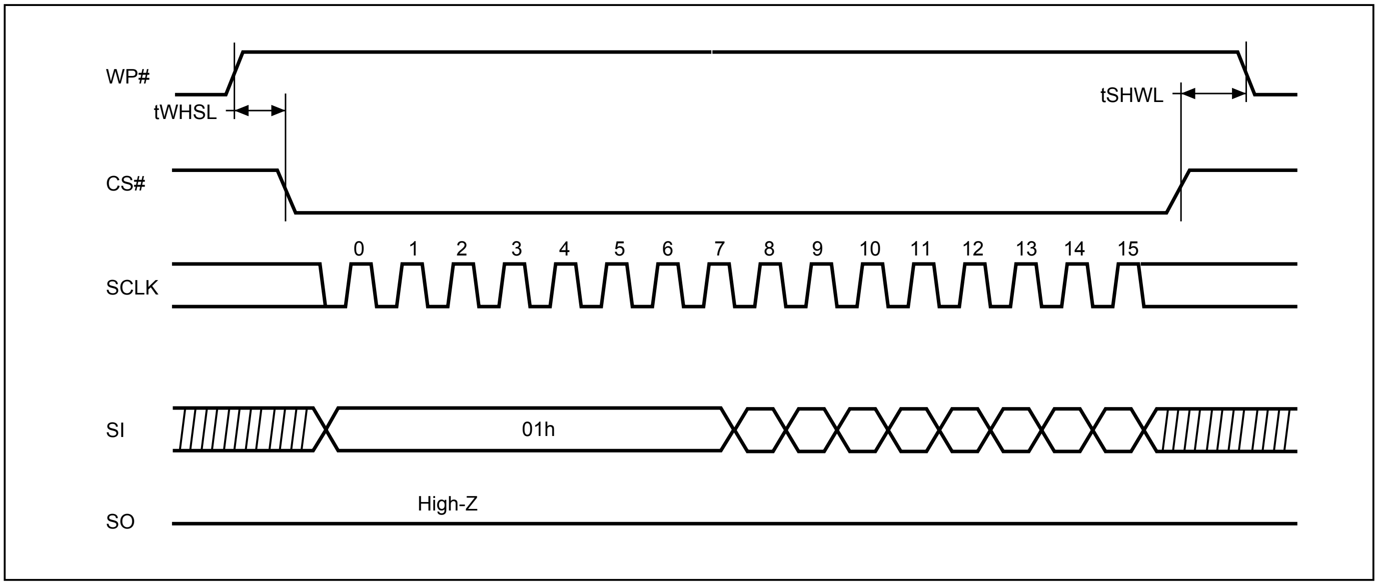


Figure 15. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



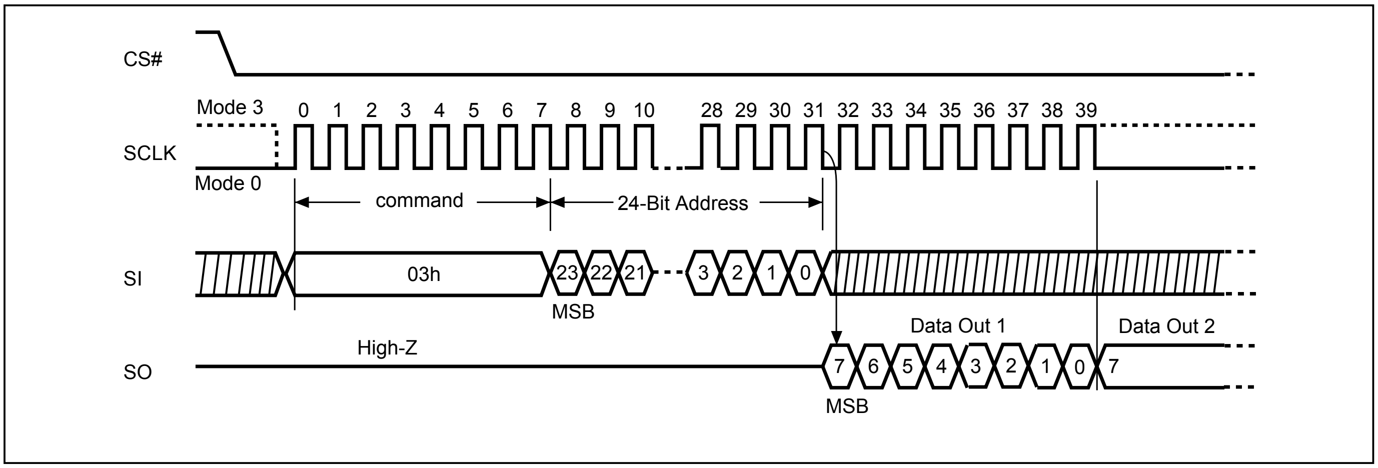
Note: WP# must be kept high until the embedded operation finish.

10-8. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 16. Read Data Bytes (READ) Sequence



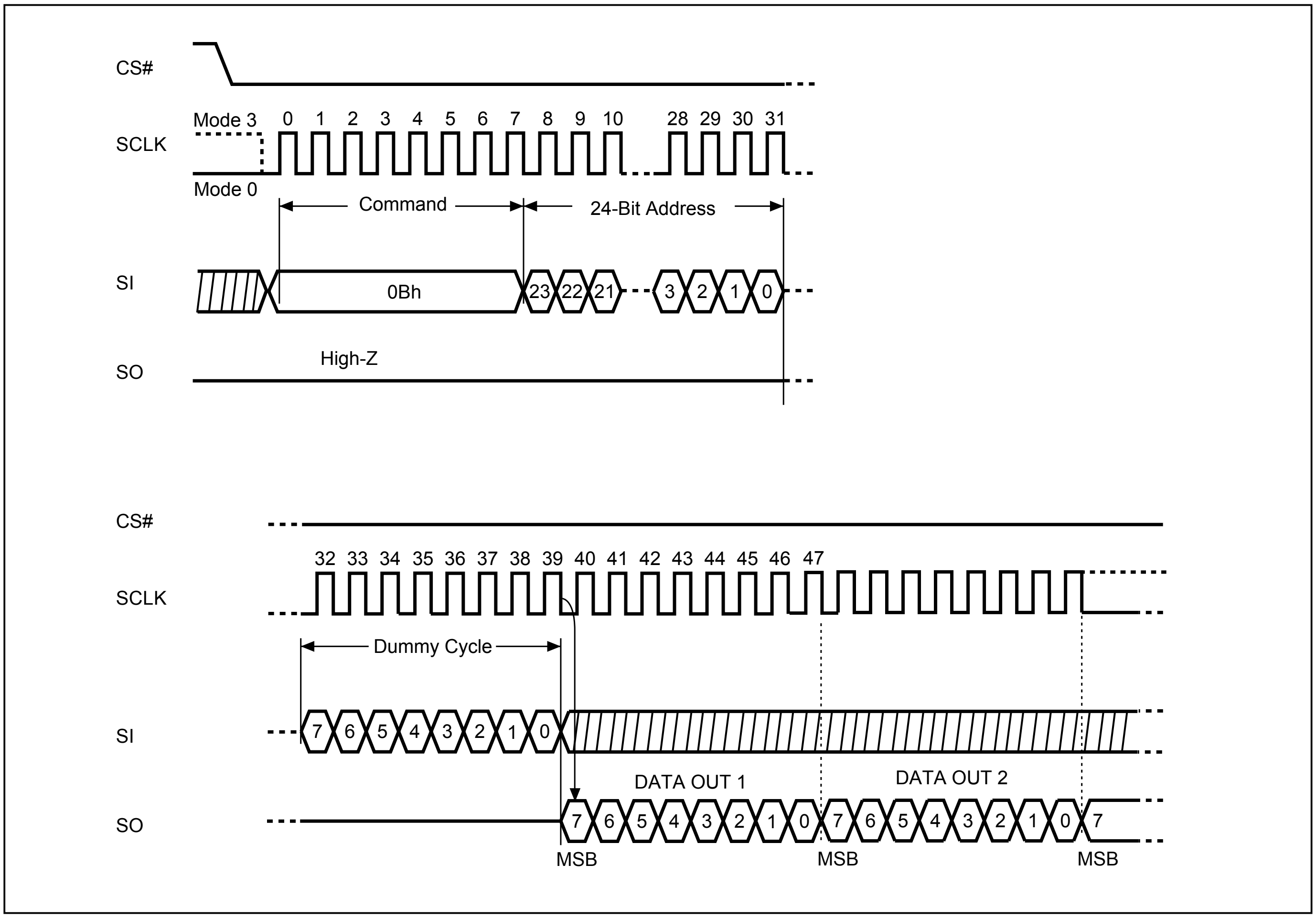
10-9. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 17. Read at Higher Speed (FAST_READ) Sequence



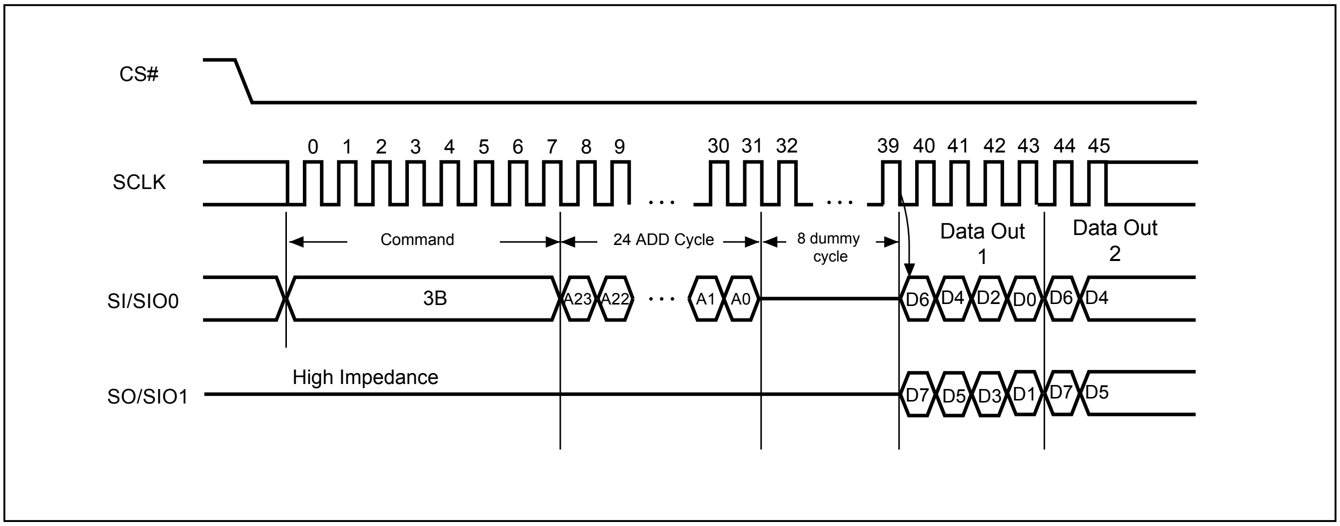
10-10. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 18. Dual Read Mode Sequence (Command 3Bh)



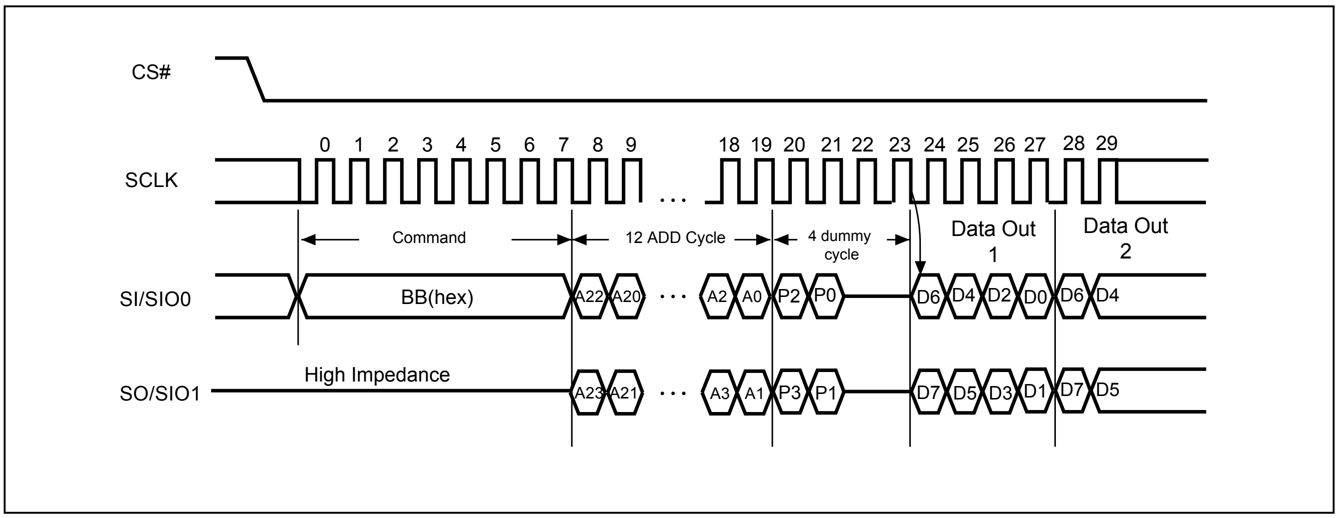
10-11.2 x I/O Read Mode (2READ)

The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 19. 2 x I/O Read Mode Sequence (Command BBh)



Note: SI/SIO0 or SO/SIO1 should be kept "0h" or "Fh" in the first two dummy cycles. In other words, P2=P0 or P3=P1 is necessary.

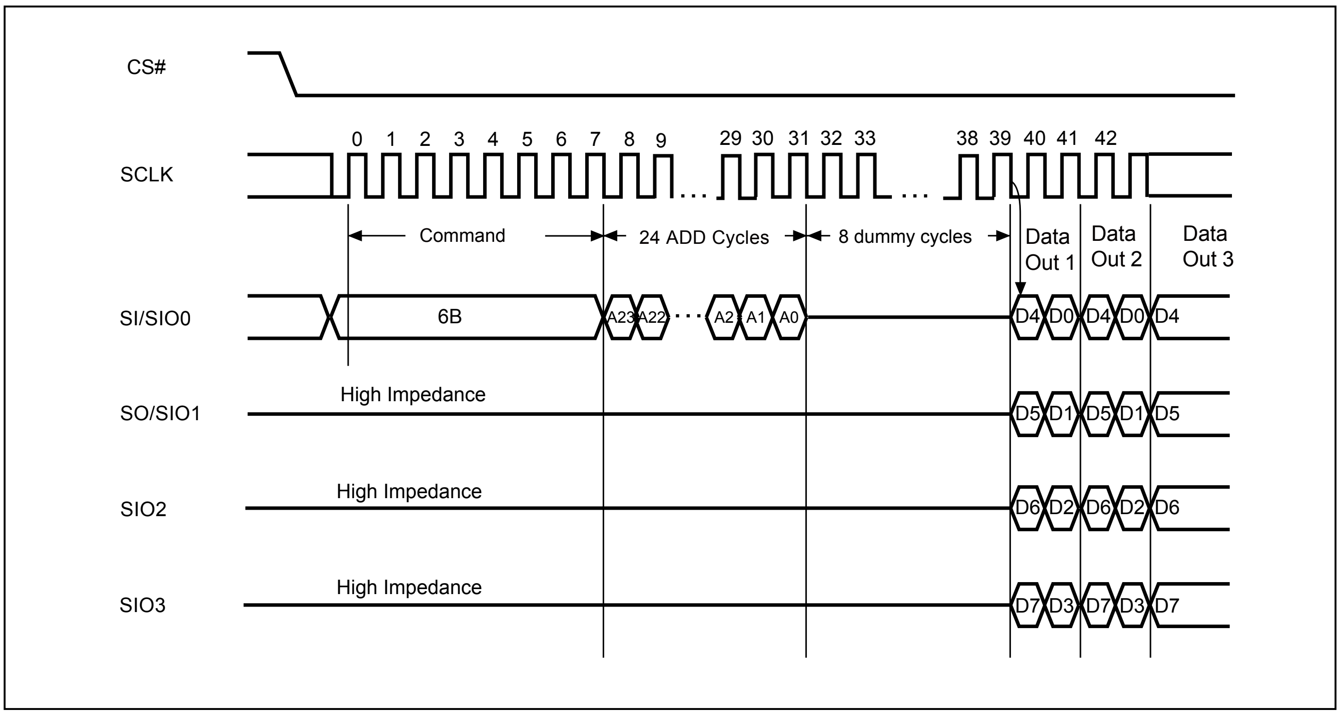
10-12. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 20. Quad Read Mode Sequence (Command 6Bh)



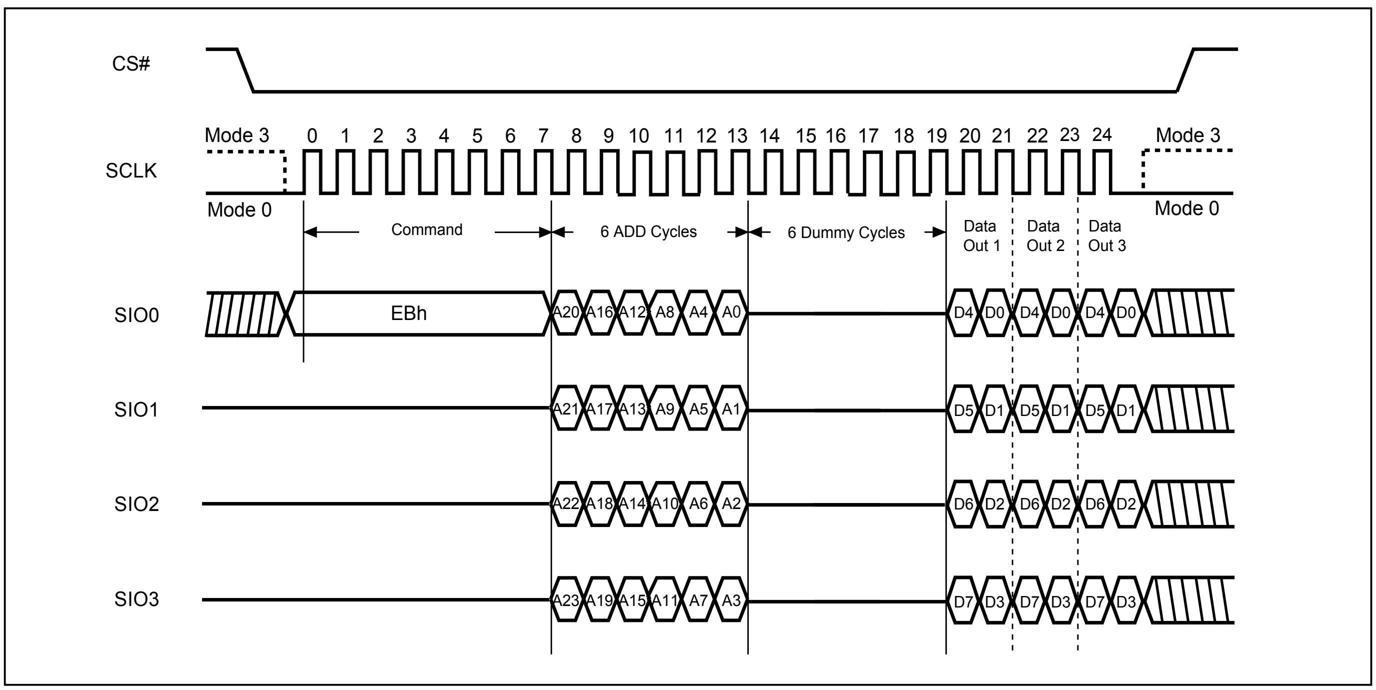
10-13. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→6 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 21. 4 x I/O Read Mode Sequence



10-14. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to *"Table 3. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

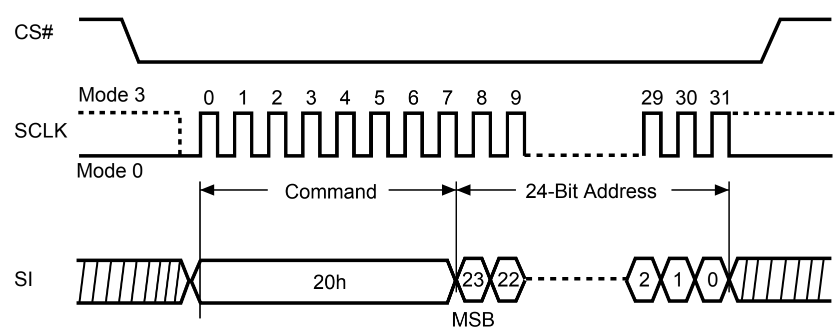
Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Figure 22. Sector Erase (SE) Sequence



10-15. Block Erase (BE32K)

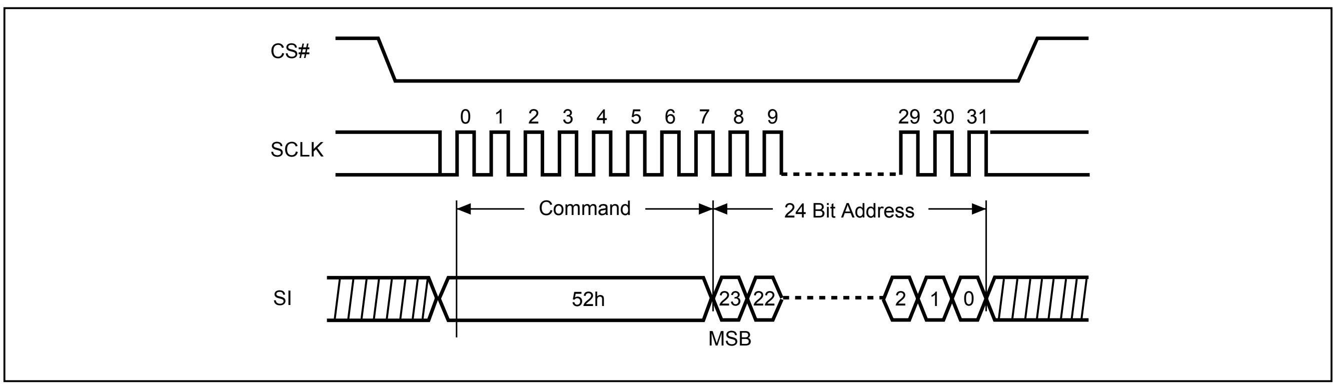
The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (please refer to *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3-0, the array data will be protected (no change) and the WEL bit still be reset.

Figure 23. Block Erase 32KB (BE32K) Sequence (Command 52h)



10-16. Block Erase (BE)

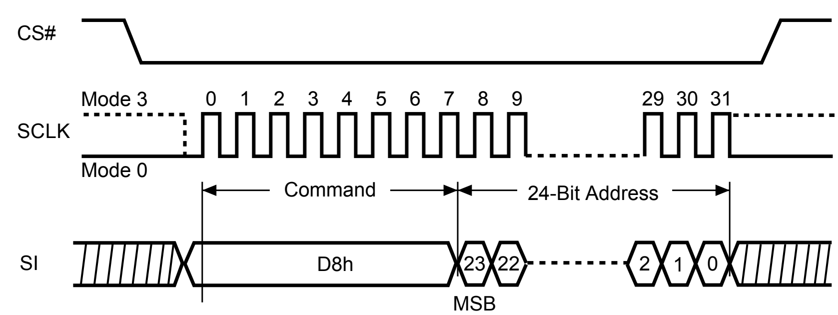
The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 24. Block Erase (BE) Sequence



10-17. Chip Erase (CE)

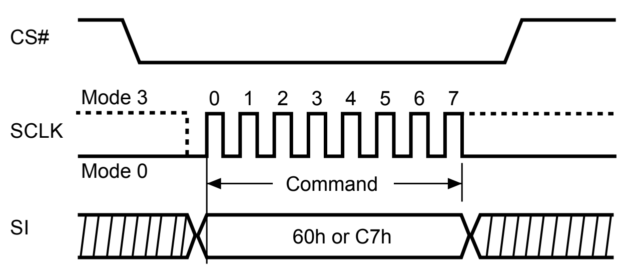
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→send CE instruction code→CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP1, BP0 all set to "0". BP2 is a "Don't Care" and can be "1" or "0".

Figure 25. Chip Erase (CE) Sequence



10-18. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

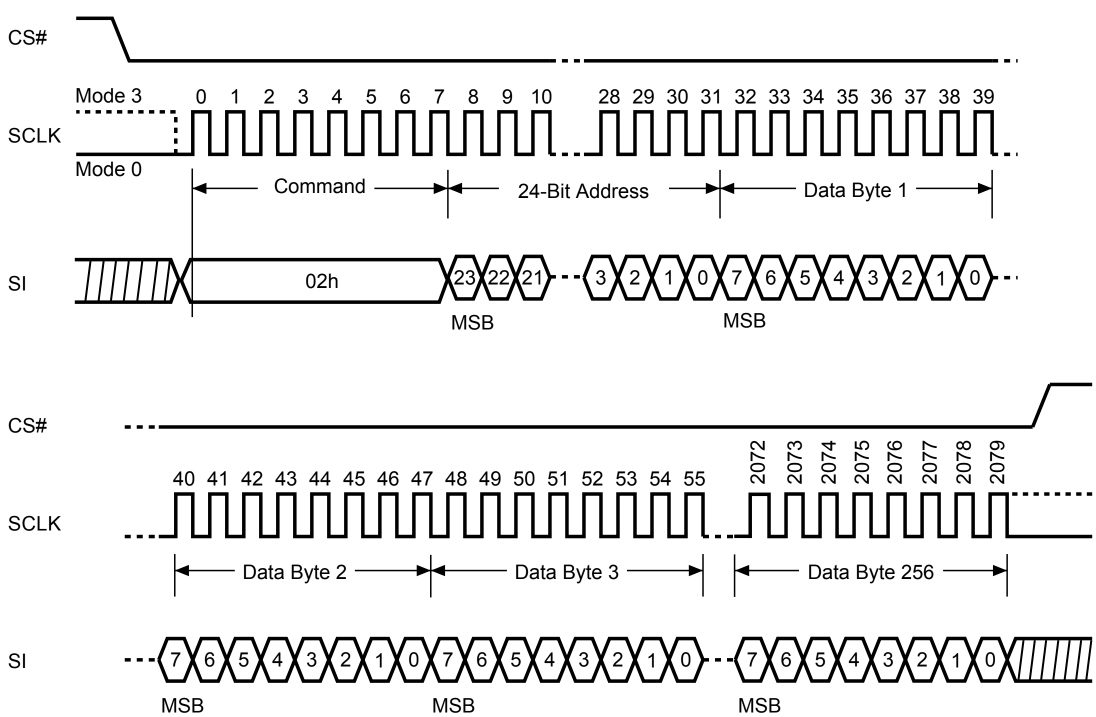
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

The SIO[3:1] are "don't care".

Figure 26. Page Program (PP) Sequence

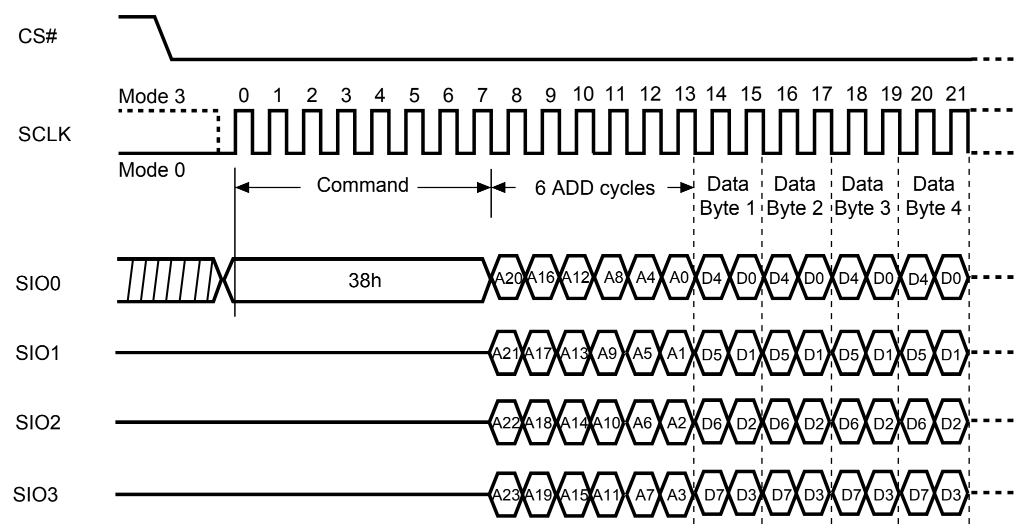


10-19. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The 4PP operation frequency supports as fast as f4PP. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

Figure 27. 4 x I/O Page Program (4PP) Sequence



10-20. Deep Power-down (DP)

The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power-down mode, in which the quiescent current is reduced from ISB1 to ISB2.

The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must go high at the byte boundary (after exactly eighth bits of the instruction code have been latched-in); otherwise the instruction will not be executed. SIO[3:1] are "don't care".

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Powerdown mode and before the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored except Release from Deep Power-down (RDP).

The device exits Deep Power-down mode and returns to Stand-by mode if it receives a Release from Deep Power-down (RDP) instruction, power-cycle, or reset. Please refer to *"Figure 29. Release from Deep Power-down (RDP) Sequence"*.

Figure 28. Deep Power-down (DP) Sequence (Command B9h)

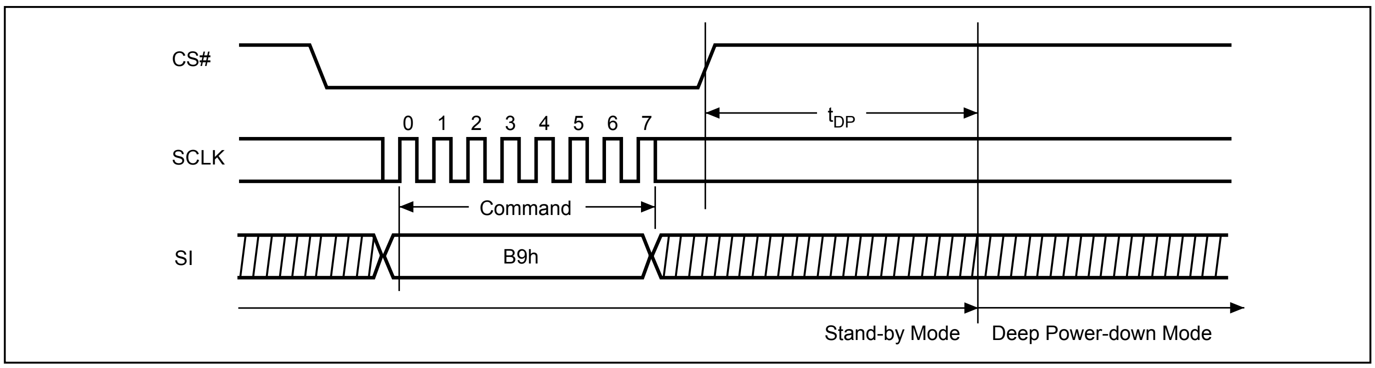
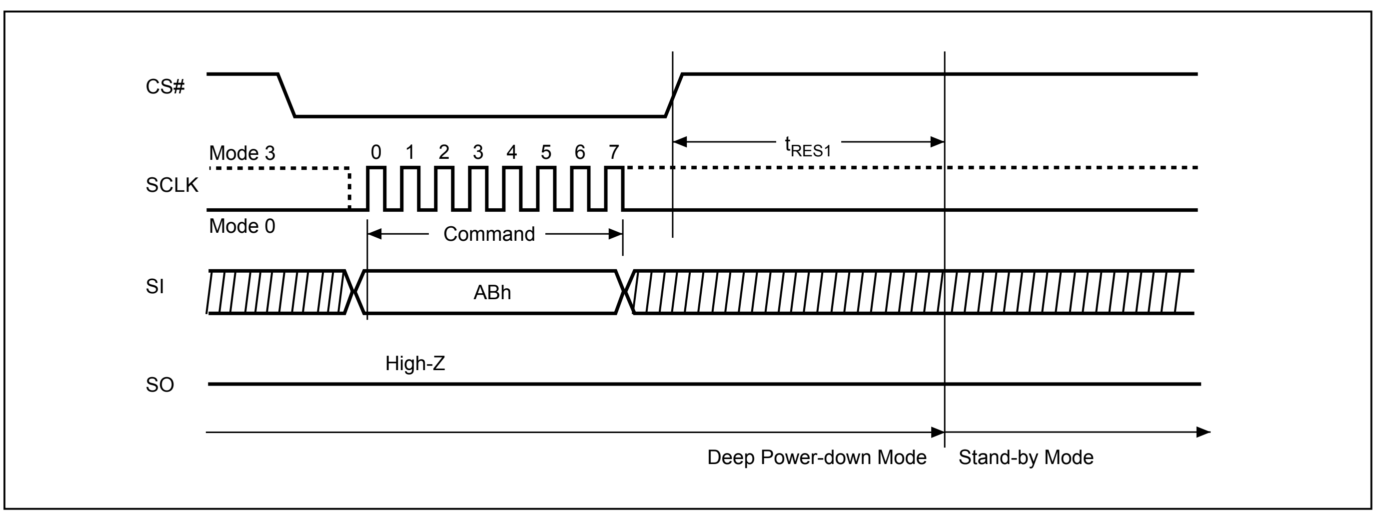


Figure 29. Release from Deep Power-down (RDP) Sequence



10-21. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the standby Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 15. AC Characteristics (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.3V - 3.6V)"*. Once in the standby mode, the device waits to be selected, so that it can receive, decode and execute instructions.

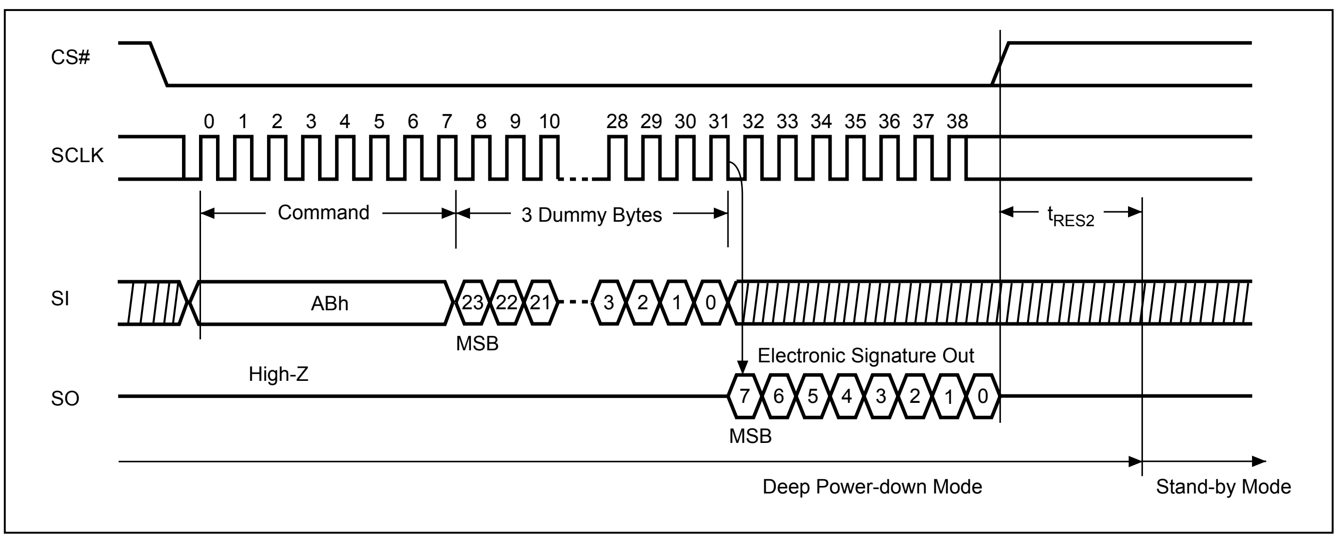
RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 5. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycles; there's no effect on the current program/erase/write cycles in progress.

The SIO[3:1] are don't care when during this mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-down Mode.

Figure 30. Read Electronic Signature (RES) Sequence (Command ABh)



10-22. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit Secured OTP mode. While the device is in 4K-bit Secured OTP mode, array access is not available. The additional 4K-bit Secured OTP is independent from main array, and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

The SIO[3:1] are "don't care".

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

10-23. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit Secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

The SIO[3:1] are "don't care".

10-24. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

The SIO[3:1] are "don't care".

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the Secured OTP area is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more.

Program Suspend Status bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Erase Suspend Status bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Fail Flag bit. The Program Fail bit shows the status of the last Program operation. The bit will be set to "1" if the program operation failed or the program region was protected. It will be automatically cleared to "0" if the next program operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Fail Flag bit. The Erase Fail bit shows the status of last Erase operation. The bit will be set to "1" if the erase operation failed or the erase region was protected. It will be automatically cleared to "0" if the next erase operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

Table 8. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend status)	PSB (Program Suspend status)	LDSO (lock-down 4K-bit Secured OTP)	Secured OTP Indicator bit (4K-bit Secured OTP)
Reserved	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	Reserved	0=Erase is not suspended 1=Erase is suspended (default=0)	0=Program is not suspended 1=Program is suspended (default=0)	0 = not lockdown 1 = lock-down (cannot program/ erase OTP)	0 = nonfactory lock 1 = factory lock
non-volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit
Reserved	Read Only	Read Only		Read Only	Read Only	OTP	Read Only

10-25. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 1st 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the 1st 4K-bit Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The SIO[3:1] are "don't care".

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

10-26. Program/Erase Suspend/Resume

The Suspend instruction interrupts a Page Program, Sector Erase, or Block Erase operation to allow access to the memory array. After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the sector or block being erased (*"Table 9. Readable Area of Memory While a Program or Erase Operation is Suspended"*).

Table 9. Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Sector Erase (4KB)	All but the 4KB Sector being erased
Block Erase (32KB)	All but the 32KB Block being erased
Block Erase (64KB)	All but the 64KB Block being erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL (*"Figure 32. Suspend to Read/Program Latency"*) before the Write Enable Latch (WEL) bit clears to “0” and the PSB or ESB sets to “1”, after which the device is ready to accept one of the commands listed in *"Table 10. Acceptable Commands During Program/Erase Suspend after tPSL/tESL"* (e.g. FAST READ). *"Table 11. Acceptable Commands During Suspend (tPSL/tESL not required)"* lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status. The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

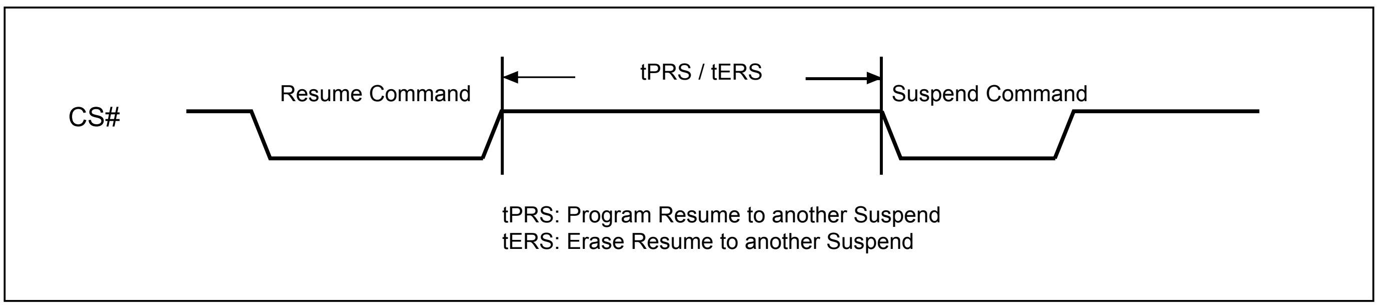
Table 10. Acceptable Commands During Program/Erase Suspend after tPSL/tESL

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03h	•	•
FAST READ	0Bh	•	•
DREAD	3Bh	•	•
QREAD	6Bh	•	•
2READ	BBh	•	•
4READ	EBh	•	•
READ UID	5Ah	•	•
RDID	9Fh	•	•
REMS	90h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
WREN	06h		•
RESUME	7Ah or 30h	•	•
PP	02h		•
4PP	38h		•

Table 11. Acceptable Commands During Suspend (tPSL/tESL not required)

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04h	•	•
RDSR	05h	•	•
RDSCUR	2Bh	•	•
RES	ABh	•	•
RSTEN	66h	•	•
RST	99h	•	•

Figure 31. Resume to Suspend Latency

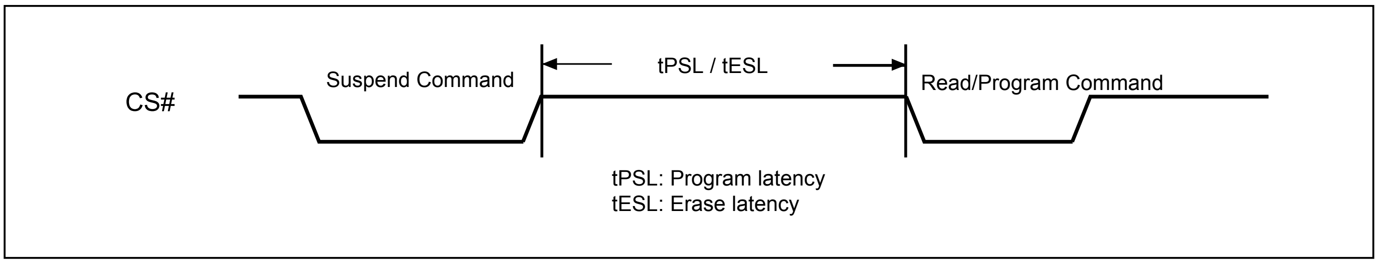


10-26-1. Erase Suspend to Program

The "Erase Suspend to Program" feature allows Page Programming while an erase operation is suspended. Page Programming is permitted in any unprotected memory except within the sector of a suspended Sector Erase operation or within the block of a suspended Block Erase operation. The Write Enable (WREN) instruction must be issued before any Page Program instruction.

A Page Program operation initiated within a suspended erase cannot itself be suspended and must be allowed to finish before the suspended erase can be resumed. The Status Register can be polled to determine the status of the Page Program operation. The WEL and WIP bits of the Status Register will remain "1" while the Page Program operation is in progress and will both clear to "0" when the Page Program operation completes.

Figure 32. Suspend to Read/Program Latency



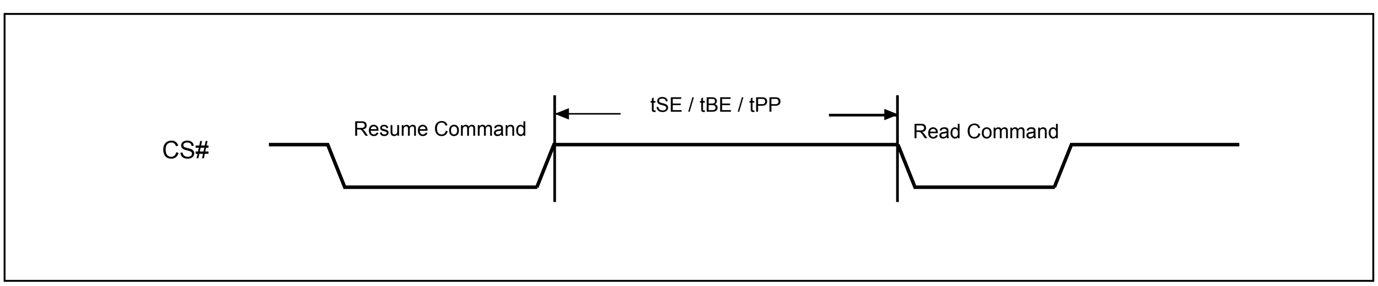
Notes:
1. Please note that Program only available after the Erase-Suspend operation
2. To check suspend ready information, please read security register bit2(PSB) and bit3(ESB)

10-27. Program Resume and Erase Resume

The Resume instruction resumes a suspended Page Program, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume instruction, the WEL and WIP bits are set to "1" and the PSB or ESB is cleared to "0". The program or erase operation will continue until finished (*"Figure 33. Resume to Read Latency"*) or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction (*"Figure 31. Resume to Suspend Latency"*).

Figure 33. Resume to Read Latency



10-28. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

The SIO[3:1] are "don't care".

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. Longer latency time is required to recover from a program operation than from other operations.

Figure 34. Software Reset Recovery

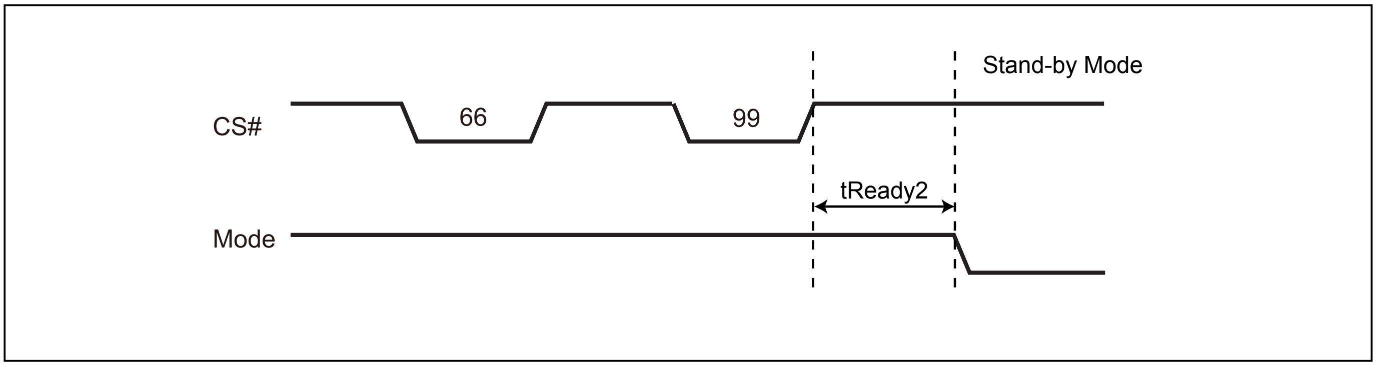
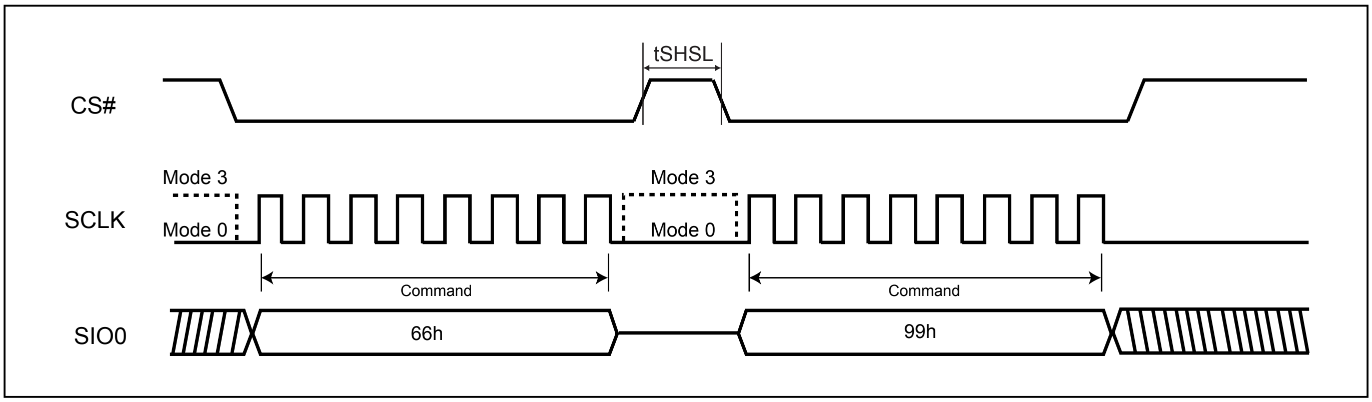


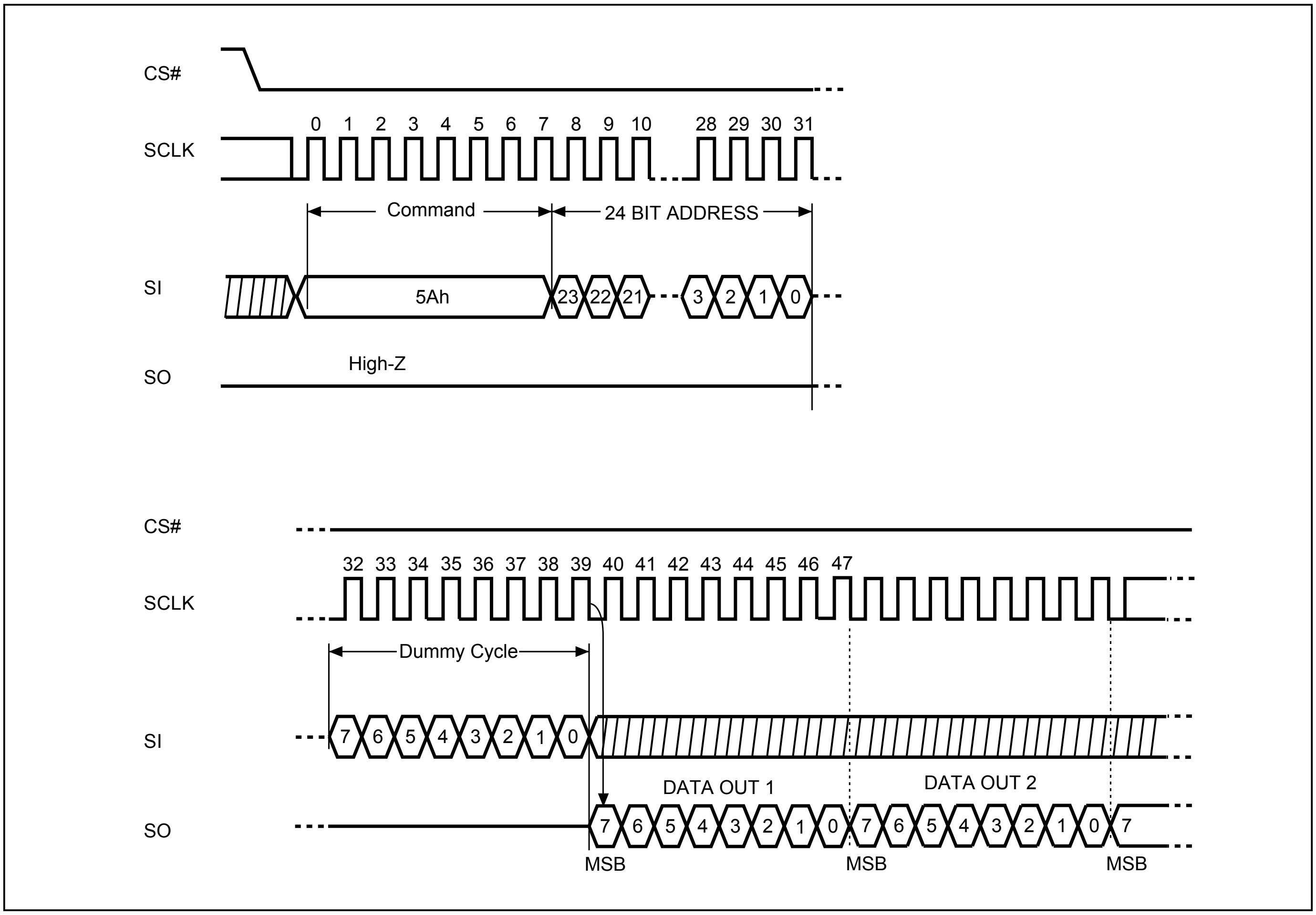
Figure 35. Reset Sequence



10-29. Read UID

MX25V2033F supports Unique ID Data (UID). Please contact local Macronix sales for details.

Figure 36. Read UID Sequence



11. POWER-ON STATE

The device is at the following states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the *"Figure 44. Power-up Timing"*.

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

12. ELECTRICAL SPECIFICATIONS

Table 12. Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to VCC+0.5V

NOTICE:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 37. Maximum Negative Overshoot Waveform

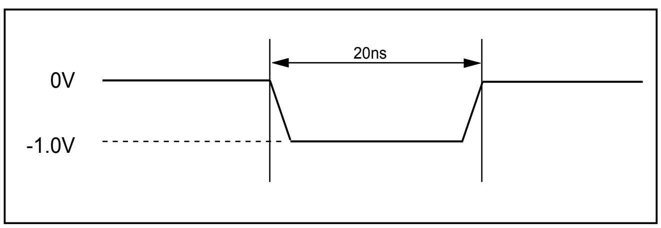


Figure 38. Maximum Positive Overshoot Waveform

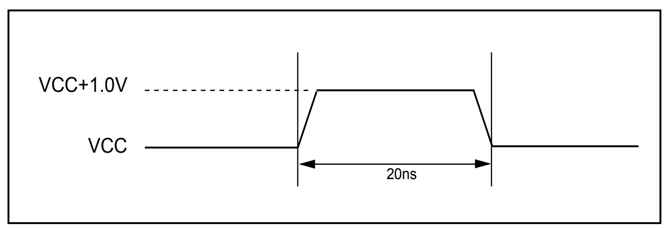


Table 13. Capacitance

TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 39. Input Test Waveforms and Measurement Level

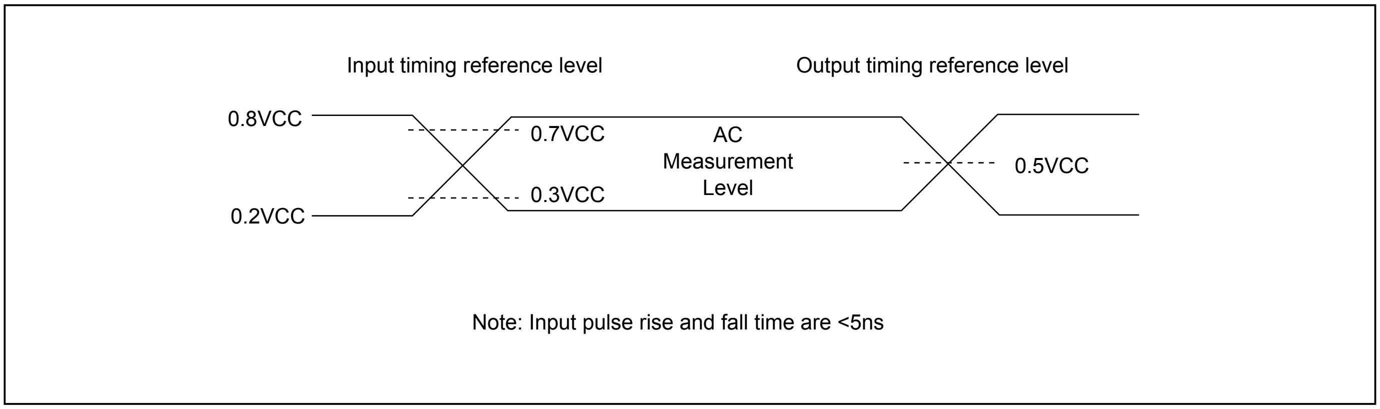


Figure 40. Output Loading

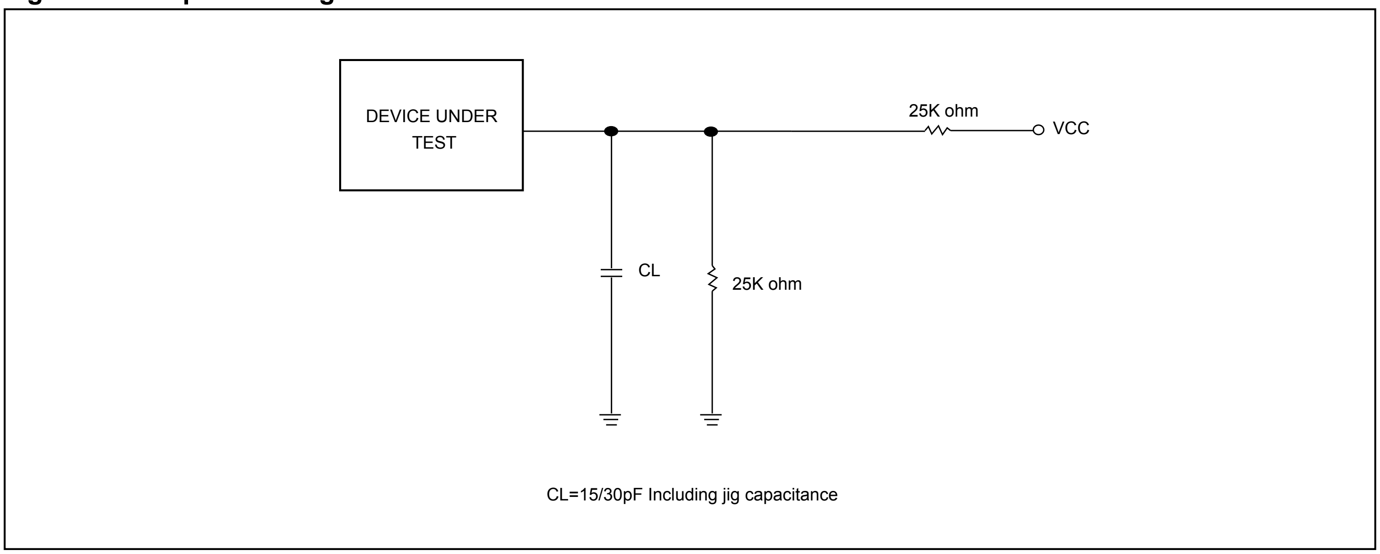


Figure 41. SCLK TIMING DEFINITION

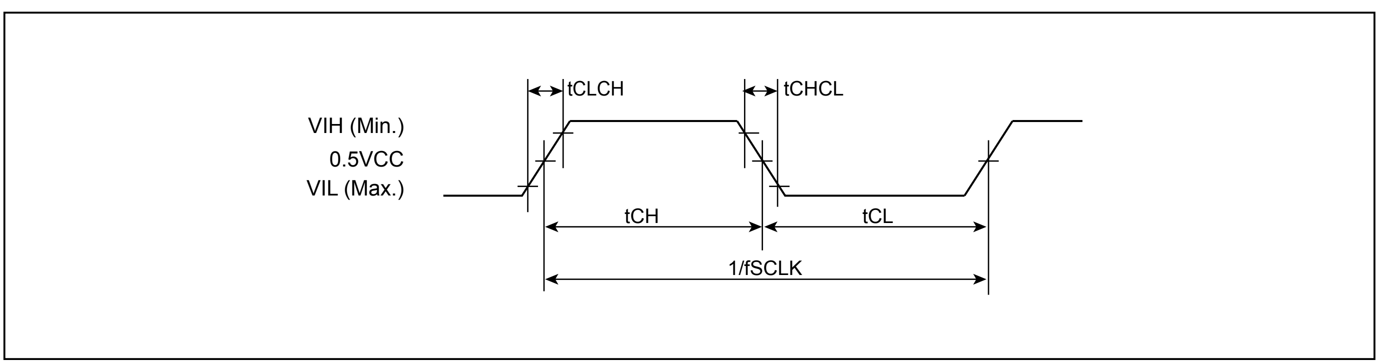


Table 14. DC Characteristics (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.3V - 3.6V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1		± 0.02	± 2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1		± 0.02	± 2	uA	VCC = VCC Max VOUT = VCC or GND
ISB1	VCC Standby Current	1		10	25	uA	VIN = VCC or GND CS#=VCC
ISB2	Deep Power-down Current			1.5	10	uA	VIN = VCC or GND CS#=VCC
ICC1	VCC Read	1		4	6	mA	f=80MHz, (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		4	20	mA	Program in Progress CS#=VCC
ICC3	VCC Write Status Register (WRSR) Current			2.1	15	mA	Program status register in progress CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		9	15	mA	Erase in Progress CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		15	20	mA	Erase in Progress CS#=VCC
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA
VWI	Low VCC Write Inhibit Voltage	3	1.5		2.1	V	

Notes :

1. *Typical values at VCC = 2.5V, T = 25°C. These currents are valid for all product versions (package and speeds).*
2. *Typical value is calculated by simulation.*
3. *Not 100% tested.*

Table 15. AC Characteristics (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.3V - 3.6V)

Symbol	Alt.	Parameter		Min.	Typ.[2]	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE32K, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR		D.C.		80 (2.7-3.6V) 50 (2.3-2.7V)	MHz
fRSCLK	fR	Clock Frequency for READ instructions				33	MHz
fTSCLK	fT	Clock Frequency for 2READ/DREAD instructions				80 (2.7-3.6V) 50 (2.3-2.7V)	MHz
	fQ	Clock Frequency for 4READ/QREAD instructions				60 (2.7-3.6V) 33 (2.3-2.7V)	MHz
f4PP		Clock Frequency for 4PP (Quad page program)				60 (2.7-3.6V) 33 (2.3-2.7V)	MHz
tCH[1]	tCLH	Clock High Time	Others (fSCLK)	45%x (1/fSCLK)			ns
			Normal Read (fRSCLK)	13			ns
tCL[1]	tCLL	Clock Low Time	Others (fSCLK)	45%x (1/fSCLK)			ns
			Normal Read (fRSCLK)	13			ns
tCLCH[8]		Clock Rise Time (peak to peak)		0.1			V/ns
tCHCL[8]		Clock Fall Time (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		7			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		7			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		7			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		7			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read	20			ns
			From Write/Erase/Program to Read Status Register	40			ns
tSHQZ[8]	tDIS	Output Disable Time				6	ns
tCLQV	tV	Clock Low to Output Valid	Loading: 30pF			8	ns
			Loading: 15pF			6	ns
tCLQX	tHO	Output Hold Time		0			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)		8			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)		8			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)		8			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)		8			ns
tHHQX	tLZ	HOLD# to Output Low-Z				10	ns
tHLQZ	tHZ	HOLD# to Output High-Z				10	ns
tWHSL[3]		Write Protect Setup Time		20			ns
tSHWL[3]		Write Protect Hold Time		100			ns
tDP		CS# High to Deep Power-down Mode				10	us
tRES1[8]		CS# High to Standby Mode without Electronic Signature Read				8.8	us
tRES2[8]		CS# High to Standby Mode with Electronic Signature Read				8.8	us
tW		Write Status Register Cycle Time			5	40	ms
tREADY2		Reset Recovery time (During instruction decoding)		30			us
		Reset Recovery time (for read operation)		30			us
		Reset Recovery time (for program operation)		80			us
		Reset Recovery time(for SE4KB operation)		12			ms
		Reset Recovery time (for BE32KB/64KB operation)		12			ms
		Reset Recovery time (for Chip Erase operation)		12			ms
		Reset Recovery time (for WRSR operation)		0.1			ms

Symbol	Alt.	Parameter	Min.	Typ.[2]	Max.	Unit
tESL[7]		Erase Suspend Latency			40	us
tPSL[7]		Program Suspend Latency			40	us
tPRS [4]		Latency between Program Resume and next Suspend	0.3			us
tERS [5]		Latency between Erase Resume and next Suspend	0.3			us
tBP		Byte-Program		30	50	us
tPP		Page Program Cycle Time		1.0	10	ms
tSE		Sector Erase Cycle Time		50	400	ms
tBE32K		Block Erase (32KB) Cycle Time		0.3	3.8	s
tBE		Block Erase (64KB) Cycle Time		0.6	4	s
tCE		Chip Erase Cycle Time		2	14	s

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Program operation may be interrupted as often as system request. The minimum timing of tPRS must be observed before issuing the next program suspend command. However, in order for an Program operation to make progress, tPRS ≥ 100us must be included in resume-to-suspend loop(s). Not 100% tested.
5. Erase operation may be interrupted as often as system request. The minimum timing of tERS must be observed before issuing the next erase suspend command. However, in order for an Erase operation to make progress, tERS ≥ 200us must be included in resume-to-suspend loop(s). The details are described in Macronix application notes. Not 100% tested.
6. Test condition is shown as *"Figure 39. Input Test Waveforms and Measurement Level"* and *"Figure 40. Output Loading"*.
7. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
8. The value guaranteed by characterization, not 100% tested in production.

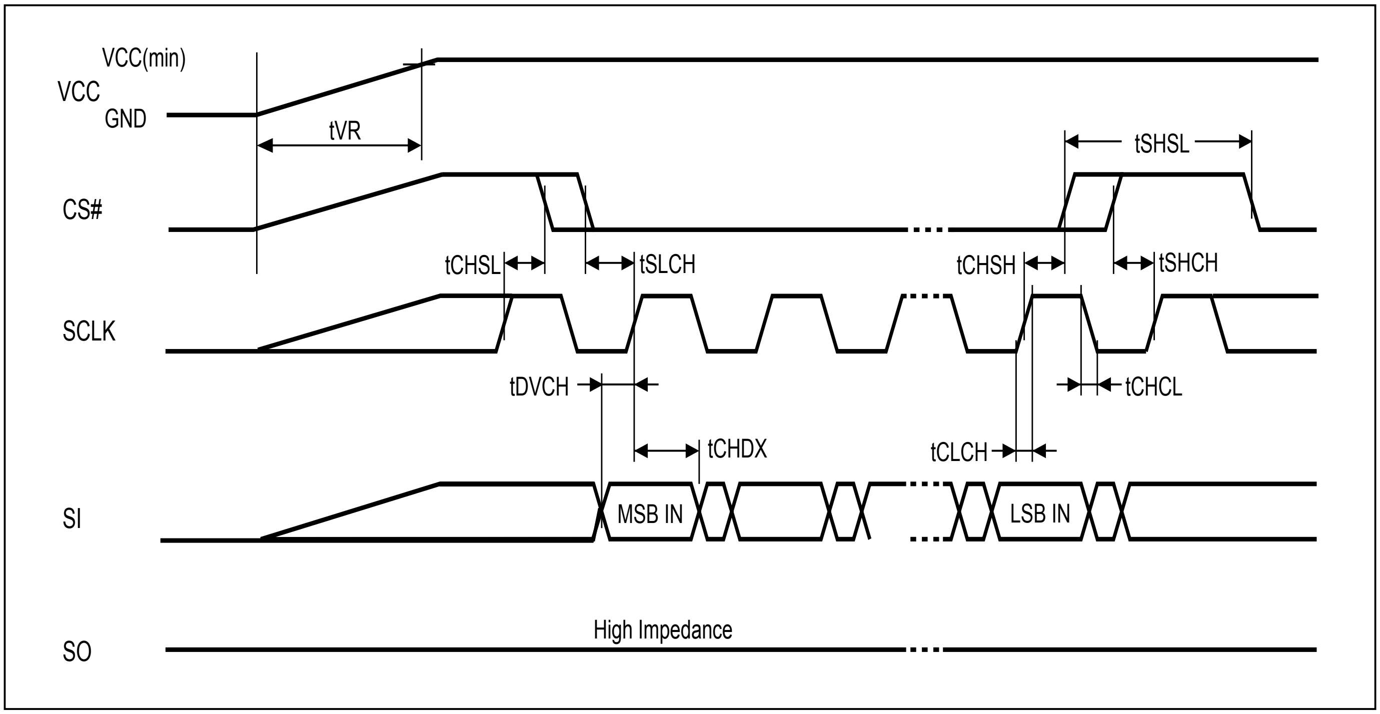
13. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 42. AC Timing at Device Power-Up"* and *"Figure 43. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 42. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes:
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 15. AC Characteristics (Temperature = -40°C to 85°C for Industrial grade, VCC = 2.3V - 3.6V)"*.

Figure 43. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

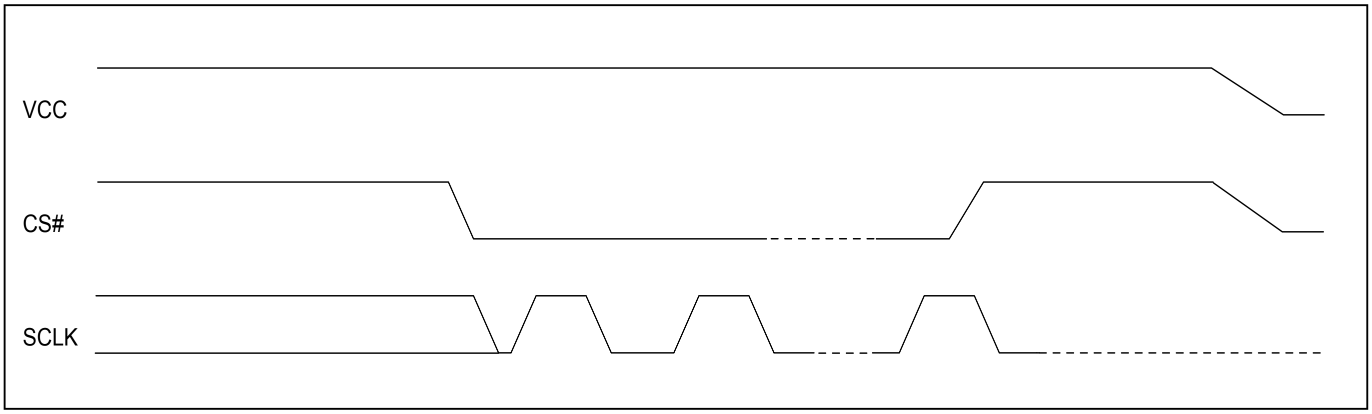


Figure 44. Power-up Timing

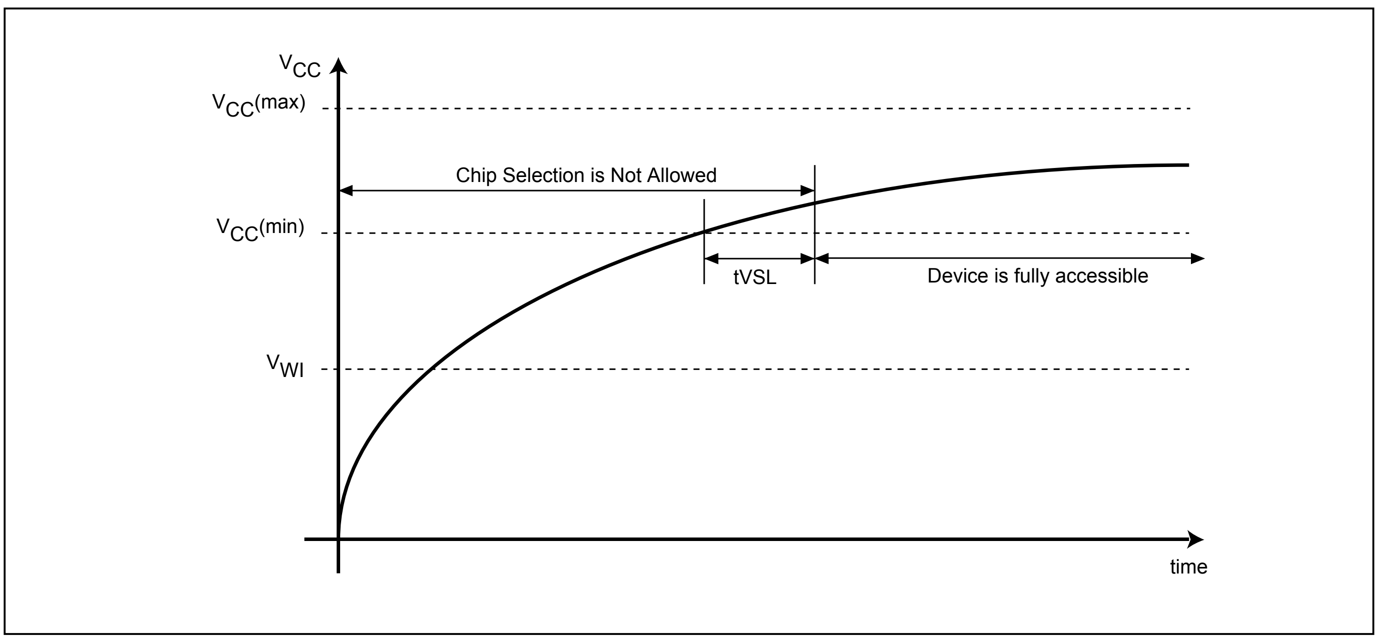


Figure 45. Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below V_{PWD} for at least tPWD timing. Please check the table below for more detail.

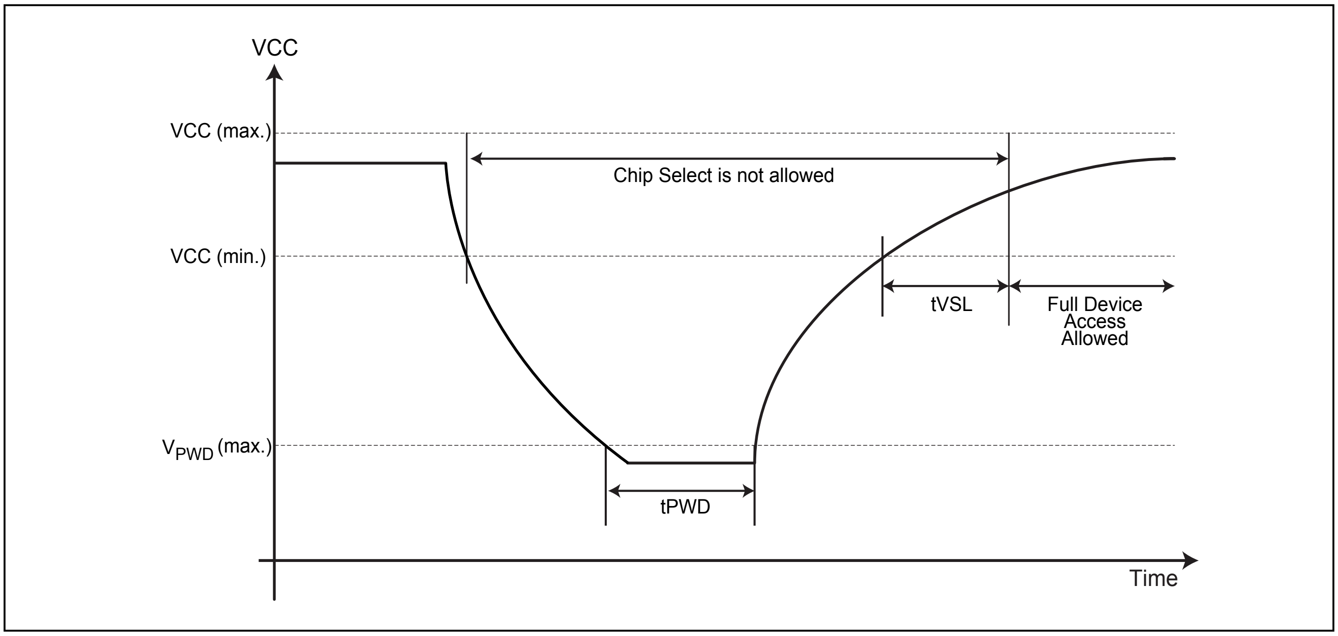


Table 16. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	800		us
VWI	Write Inhibit Voltage	1.5	2.1	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us

Note: These parameters are characterized only.

13-1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

15. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time		5	40	ms
Sector Erase Cycle Time (4KB)		50	400	ms
Block Erase Cycle Time (32KB)		0.3	3.8	s
Block Erase Cycle Time (64KB)		0.6	4	s
Chip Erase Cycle Time		2	14	s
Byte Program Time		30	50	us
Page Program Time		1.0	10	ms
Erase/Program Cycle	100,000			cycles

Notes:

1. Typical erase assumes the following conditions: 25°C, typical operation voltage and all zero pattern.
2. Under worst conditions of 85°C and minimum operation voltage.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Typical program assumes the following conditions: 25°C, typical VCC, and checkerboard pattern.

14. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = typical operation voltage, one pin at a time.		

16. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

PART NO.	Voltage	Package	Temperature	Remark
MX25V2033FM1I	2.3V-3.6V	8-SOP (150mil)	-40°C to 85°C	
MX25V2033FZUI	2.3V-3.6V	8-USON (2x3mm)	-40°C to 85°C	

17. PART NAME DESCRIPTION

MX 25V 2033F M1 I

TEMPERATURE RANGE:
I: Industrial (-40°C to 85°C)

PACKAGE:
M1: 8-SOP (150mil)
ZU: 8-USON (2x3mm)

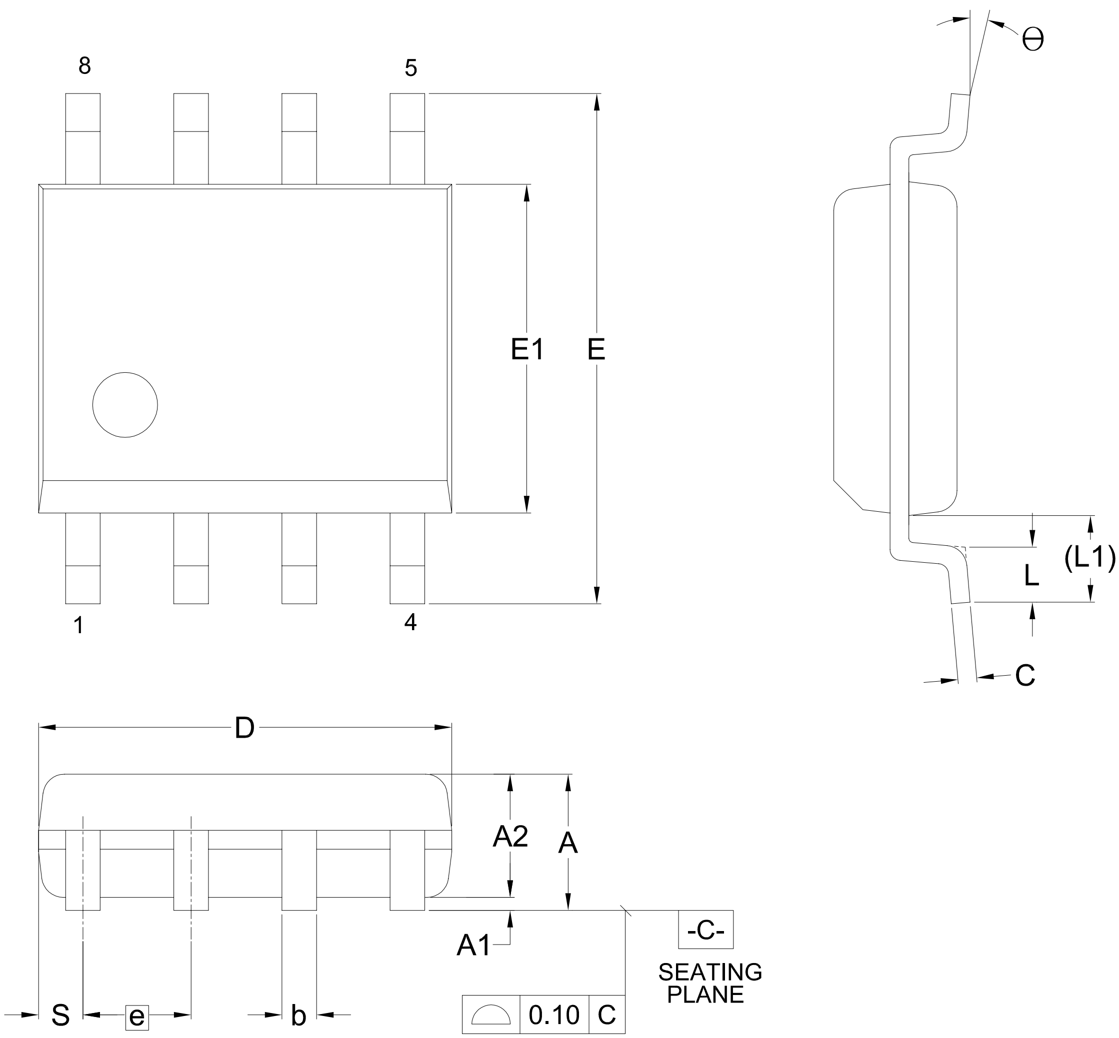
DENSITY & MODE:
2033F: 2Mb

DEVICE:
25V: Serial NOR Flash (2.3V-3.6V)

18. PACKAGE INFORMATION

18-1. 8-pin SOP (150mil)

Doe. Title: Package Outline for SOP 8L (150MIL)

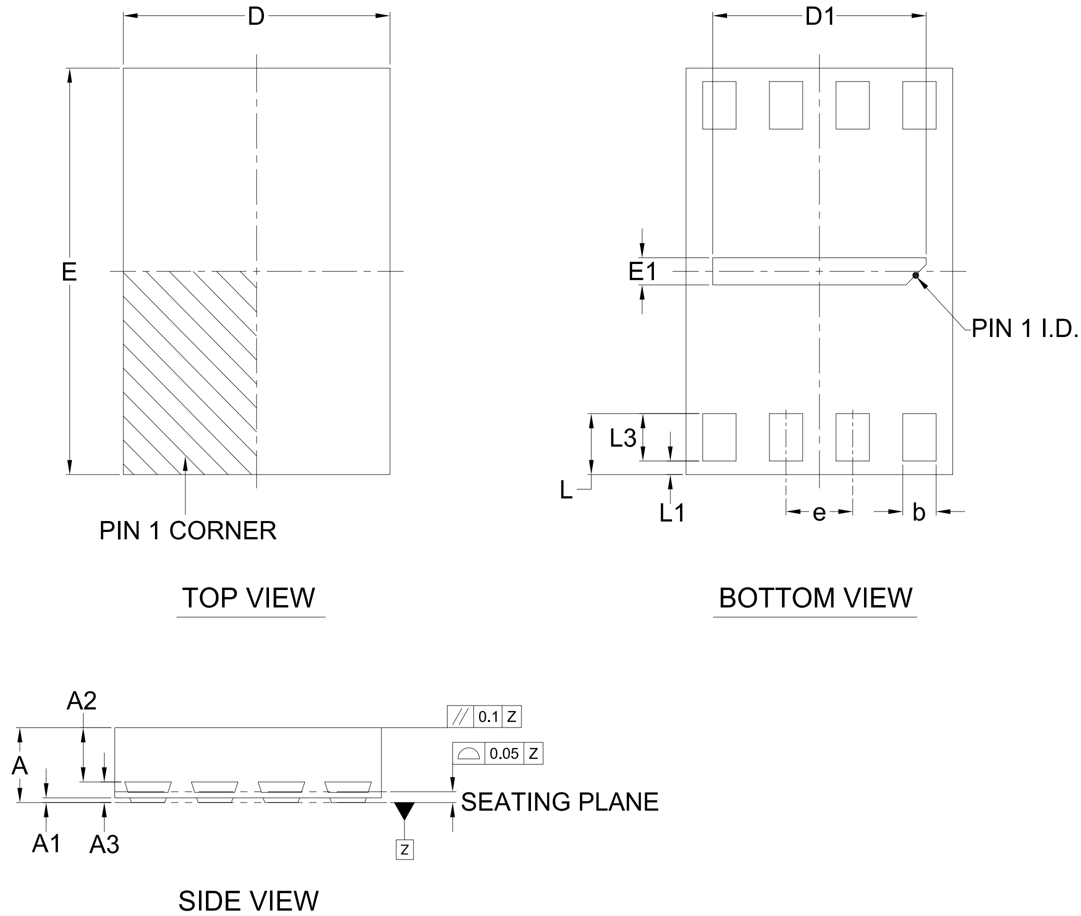


Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	1.35	0.36	0.15	4.77	5.80	3.80	---	0.46	0.85	0.41	0°
	Nom.	---	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5°
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00	---	0.86	1.25	0.67	8°
Inch	Min.	---	0.004	0.053	0.014	0.006	0.188	0.228	0.150	---	0.018	0.033	0.016	0°
	Nom.	---	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5°
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158	---	0.034	0.049	0.026	8°

18-2. 8-land USON (2x3mm)

Doc. Title: Package Outline for USON 8L (2x3x0.6MM, LEAD PITCH 0.5MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	A3	b	D	D1	E	E1	e	L	L1	L3
mm	Min.	0.50	0	---	---	0.20	1.90	1.50	2.90	0.10	---	0.40	0	0.30
	Nom.	0.55	0.035	0.40	0.152	0.25	2.00	1.60	3.00	0.20	0.50	0.45	---	0.40
	Max.	0.60	0.05	0.425	---	0.30	2.10	1.70	3.10	0.30	---	0.50	0.15	0.50
Inch	Min.	0.020	0	---	---	0.008	0.075	0.059	0.114	0.004	---	0.016	0	0.012
	Nom.	0.022	0.0014	0.016	0.0060	0.010	0.079	0.063	0.118	0.008	0.020	0.018	---	0.016
	Max.	0.024	0.002	0.0167	---	0.012	0.083	0.067	0.122	0.012	---	0.020	0.006	0.020

19. REVISION HISTORY

Revision	Descriptions	Page
March 08, 2017		
0.00	1. Initial Release.	All
August 24, 2017		
1.0	1. Removed the document status "Advanced Information" to align with the product status.	All
	2. Specification improved as: Typ. tSE: 50ms Typ. tBE32K: 0.3s Typ. tBE: 0.6s Typ. tCE: 2s	P5, 57, 61
	3. Added *"Figure 41. SCLK TIMING DEFINITION"*.	P54
	4. Content modification.	P1, 15-16, 20, 25-26, 39, 43, 56
	5. Format modification.	P64-65

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