PRM™ Regulator
MPRM28Ax360M120A00

High-Efficiency Converter

Features & Benefits

- 28V input (14.0 – 50V), non-isolated ZVS buck-boost regulator
- 26.0 – 50.0V adjustable output range
- 200W output power in 1.11in^2 footprint
- 95.5% typical efficiency, at full load
- 667W/in^3 (42W/cm^3) power density
- 4.7MHrs MTBF (MIL-HDBK-217 Plus Parts Count, 25°C)
- Full VI Chip® package
  - 32.5 x 22.0 x 6.73mm

Typical Applications

- Land/Air/Sea Unmanned Vehicles/Drones
- Communications
- Radar
- Mobile Weapons

Product Ratings	
V_{IN} = 14.0 – 50.0V	P_{OUT} = 200W
V_{OUT} = 36V (26.0 – 50.0V Trim)	I_{OUT} = 5.56A

Product Description

The VI Chip® PRM Regulator is high efficiency converter, operating from a 14.0 to 50.0V_{DC} input to generate a regulated 26.0 – 50.0V_{DC} output. The ZVS buck-boost topology enables high switching frequency operation with high conversion efficiency. High switching frequency reduces the size of reactive components enabling power density up to 667W/in^3.

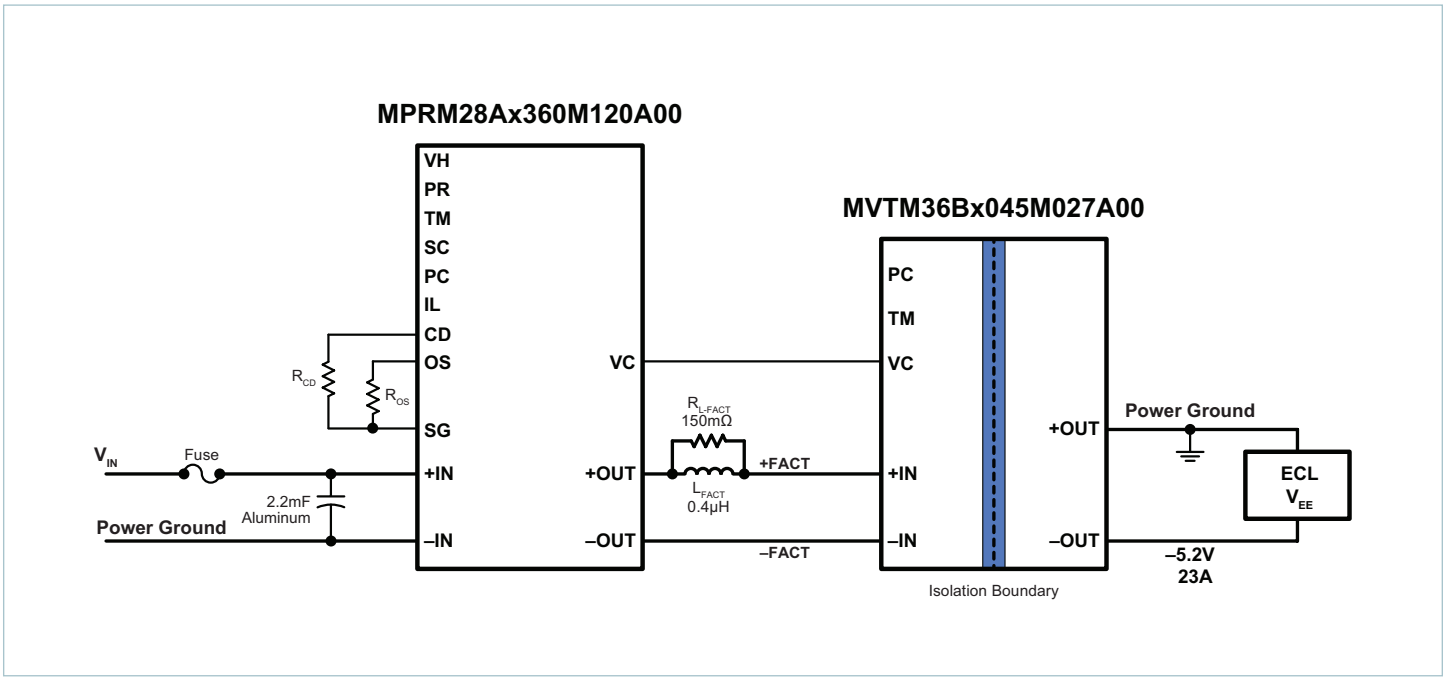
The Full VI Chip package is compatible with standard pick-and-place and surface mount assembly processes with a planar thermal interface area and superior thermal conductivity.

In a Factorized Power Architecture™ system, the PRM and downstream VTM™ current multiplier minimize distribution and conversion losses in a high-power solution, providing an isolated, regulated output voltage.

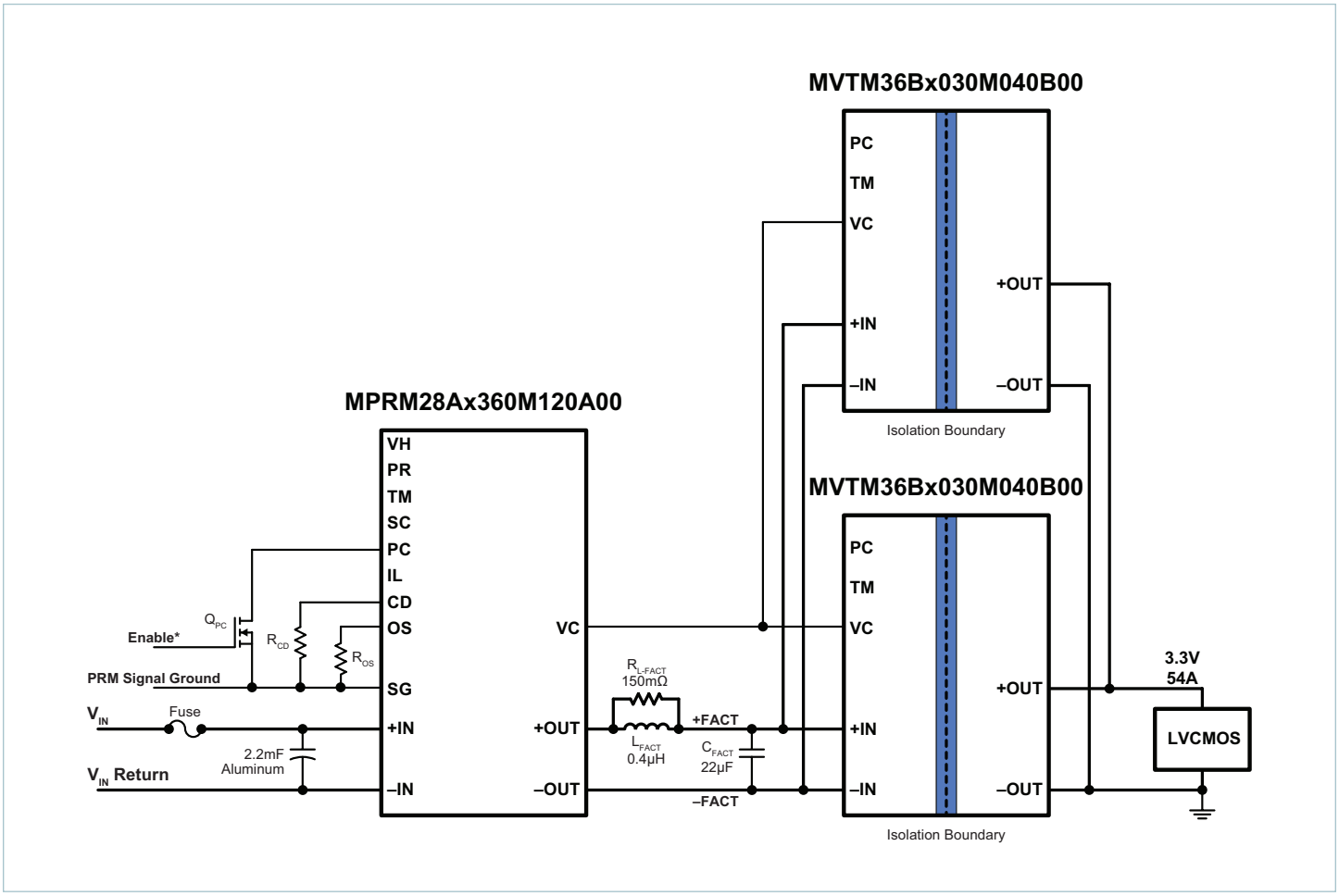
The MPRM28Ax360M120A00 can be configured for adaptive-loop output regulation, if needed. In adaptive-loop operation, the MPRM28Ax360M120A00 utilizes a unique feed-forward scheme that enables precise regulation of an isolated PoL voltage without the need for remote sensing and voltage feedback.

Note: Product images may not highlight current product markings.

Typical Applications

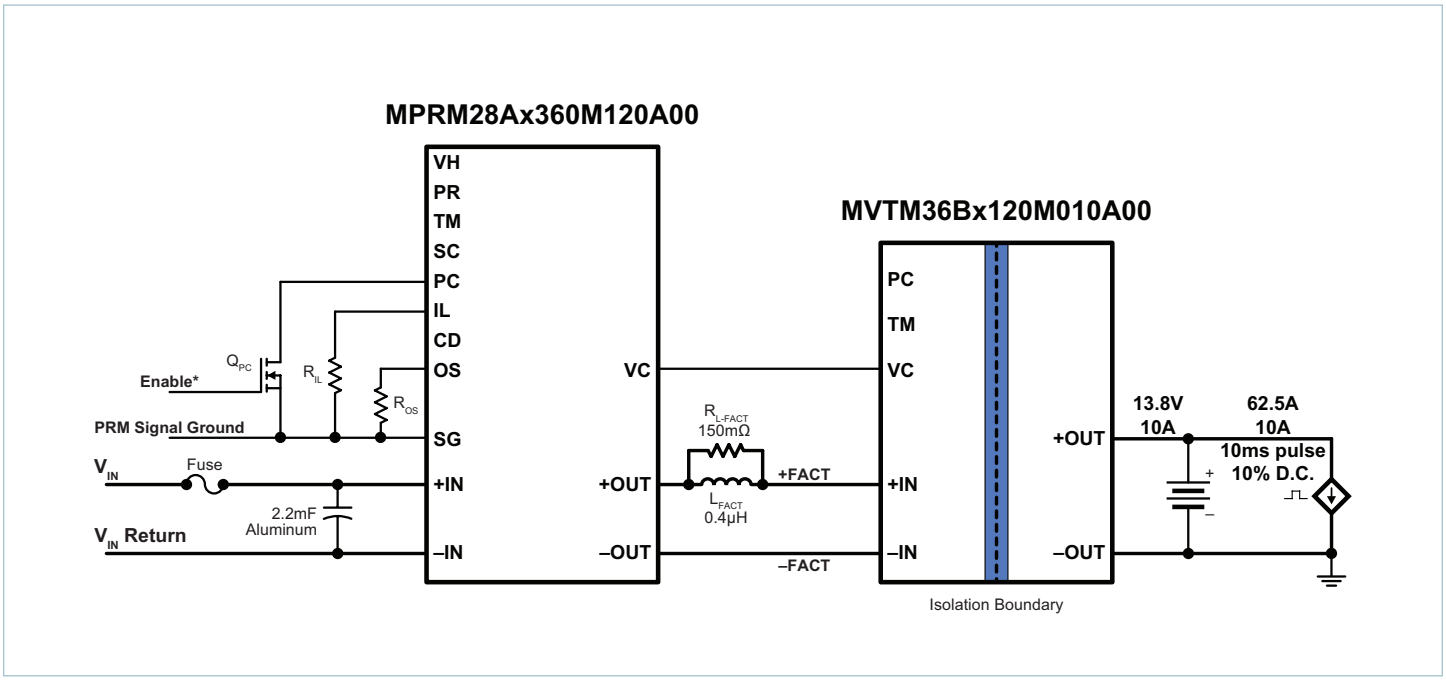


MPRM28Ax360M120A00 + MVTM36Bx045M027A00 isolated adaptive-loop configuration for negative supply



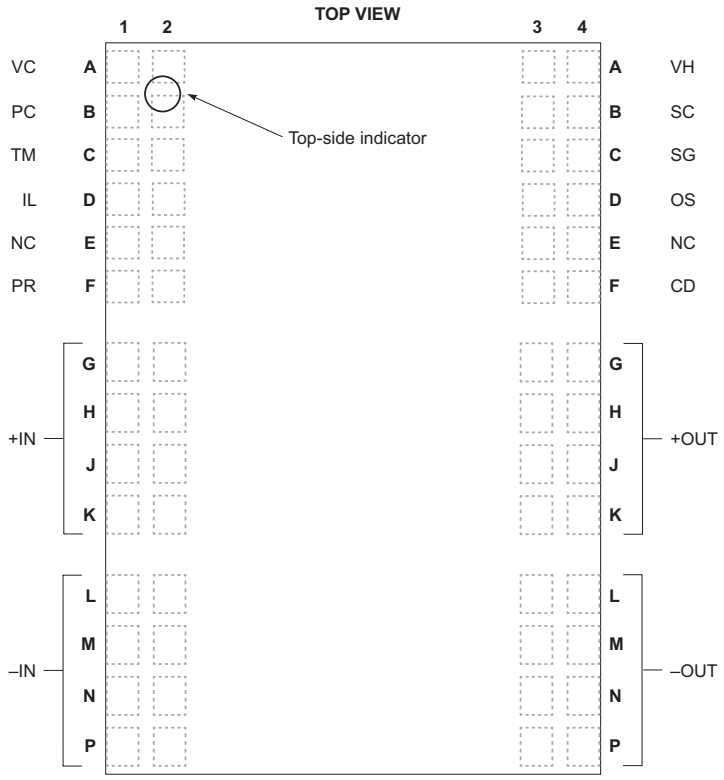
MPRM28Ax360M120A00 + two MVTM36Bx030M040B00s for isolated 180W-logic supply

Typical Applications (Cont.)



MPRM28Ax360M120A00 + MVTM36Bx120M010A00 current-limited battery charger

Pinout



Full VI Chip®

Pin Descriptions

Pin Number	Signal Name	Type	Function
A1, A2	VC	BIDIR	VTM control and temperature feedback for AL regulation
A3, A4	VH	OUTPUT	9V auxiliary voltage source
B1, B2	PC	BIDIR	Primary control; pull low to disable the PRM
B3, B4	SC	INPUT	Secondary control; regulation reference voltage
C1, C2	TM	OUTPUT	Temperature monitor
C3, C4	SG	REF	Signal ground
D1, D2	IL	INPUT	Current-limit adjust
D3, D4	OS	INPUT	Output set; output voltage divider network port
E1, E2	NC	n/a	Factory use only
E3, E4	NC	n/a	Factory use only
F1, F2	PR	BIDIR	Control node voltage
F3, F4	CD	INPUT	Compensation device for AL regulation
G1 – K1, G2 – K2	+IN	INPUT POWER	Positive input power terminal
G3 – K3, G4 – K4	+OUT	OUTPUT POWER	Positive output power terminal
L1 – P1, L2 – P2	–IN	INPUT POWER RETURN	Negative input power return; connected internally to SG
L3 – P3, L4 – P4	–OUT	OUTPUT POWER RETURN	Negative output power return

Part Ordering Information

Part Number	Package Type	Temperature Grade	Option	Tray Size
MPRM28A**F**360**M**120A**00**	**F** = Full VI Chip® SMD	**M** = –55 to 125°C	**00** = AL PRM	40 parts per tray

All products shipped in JEDEC standard high-profile (0.400in thick) trays (JEDEC Publication 95, Design Guide 4.10).

Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."

Attribute	Comments	Specification
Storage Temperature Range		–65 to 125°C
Operating Internal Temperature Range (T_{INT})		–55 to 125°C
Weight		15g
Lead Finish	Nickel	0.51 – 2.03µm
	Palladium	0.02 – 0.15µm
	Gold	0.003 – 0.050µm
MSL Rating		MSL4
ESD Rating	Method per Human Body Model Test JEDEC JS-001-2012	Class 1C, < ±2000V
	Charged Device Model JESD22-C101-E	CLASS C1, < ±500V

Reliability and Agency Approvals

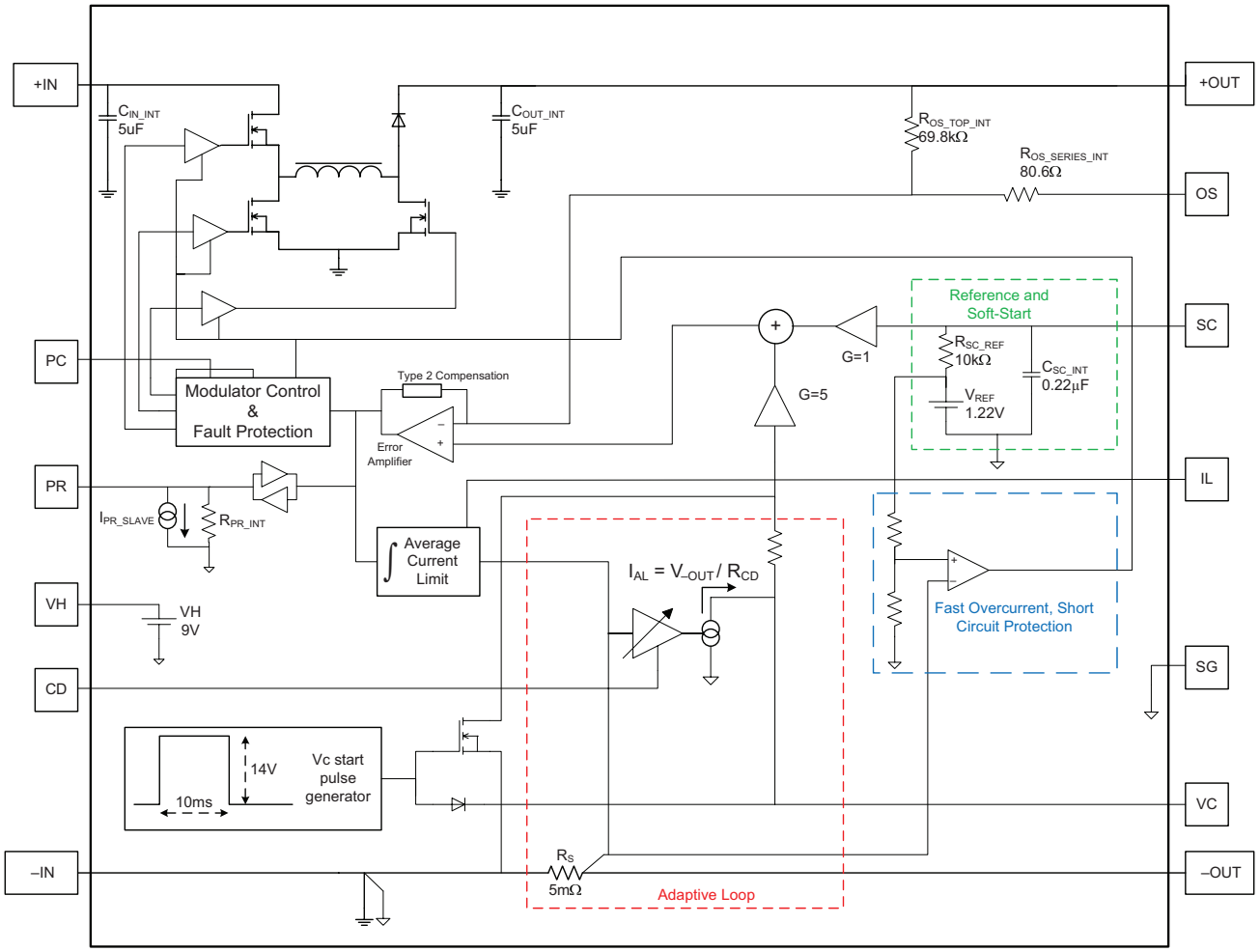
Attribute	Comments	Value	Unit
MTBF	MIL-HDBK-217 Plus Parts Count, 25°C Ground Benign, Stationary, Indoors / Computer Profile	4.7	MHrs
	MIL-HDBK-217 Plus Parts Count, 50°C Naval Sheltered, Stationary, Indoors / Computer Profile	0.85	
	MIL-HDBK-217 Plus Parts Count, 65°C Airborne Inhabited Cargo, Stationary, Indoors / Computer Profile	0.67	
Agency Approvals/Standards			
	CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable		

Absolute Maximum Ratings

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for an extended period of time may affect device reliability.

Parameter	Comments	Min	Max	Unit
+IN to –IN	Continuous, non-operating	–0.3	60	V
+OUT to –OUT	Continuous, non-operating	–0.3	60	V
VC to –OUT		–0.3	20	V
			±2000	mA
PC to SG		–0.3	7	V
TM to SG		–0.3	7	V
			±20	mA
IL, PR, SC, OS, CD	To SG	–0.3	11	V
VH to SG		–0.5	11	V
			±100	mA
SG to –IN			±100	mA
Continuous Output Current			6.6	A
Internal Operating Temperature	M-Grade	–55	125	°C
Storage Temperature	M-Grade	–65	125	°C

Functional Block Diagram



Electrical Specifications

Specifications apply over all line, load and trim voltage conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –55°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specifications						
Input Voltage Range	V_{IN}	Continuous, operating	**14.0**	28.0	**50.0**	V
Input Voltage Slew Rate	dV_{IN}/dt	0V ≤ V_{IN} ≤ 50.0V	**0.001**		**1000**	V/ms
No-Load Power Dissipation	P_{NL}	PC high, V_{IN} = 28.0V, V_{OUT} = 36.0V		1.1	**1.35**	W
Input Quiescent Current	I_{QC}	PC low, V_{IN} = 28.0V, V_{OUT} = 36.0V		21	**30**	mA
Input Current	I_{IN_DC}	I_{OUT} = 5.56A, V_{IN} = 28.0V, V_{OUT} = 36.0V		7.48	**7.6**	A
Input Capacitance (Internal)	C_{IN_INT}	Effective value, V_{IN} = 28.0V		30.0		µF
Input Capacitance (Internal) ESR	R_{C-IN}	Effective value, V_{IN} = 28.0V		2		mΩ
Power Output Specifications						
Output Voltage Set Point	V_{OUT_SET}	No connection to SC, excluding R_{OS} tolerance and burst-mode operation	**35.28**	36.0	**36.72**	V
Rated Output Voltage Trim Range	V_{OUT}		**26.0**		**50.0**	V
Output Voltage Line Regulation	$V_{OUT-REG-LINE}$			0.1	**0.2**	%
Output Voltage Load Regulation	$V_{OUT-REG-LOAD}$	At module output, AL inactive		0.1	**0.2**	%
Total Regulation Error	$V_{OUT-REG-TOTAL}$				**0.4**	%
Output Voltage Load Regulation (AL)	$V_{OUT-ALREG-LOAD}$	At module output, maximum AL compensation, excluding external resistor tolerances		1.0	**2.0**	%
Total Regulation Error (AL)	$V_{OUT-ALREG-TOTAL}$				**3.0**	%
Rated Output Power	P_{OUT}	T_{CASE} < 85°C; See Figure 2 for thermal derating T_{CASE} > 85°C			200	W
Rated Output Current	I_{OUT}				5.56	A
Switching Frequency	F_{SW_NOM}	V_{IN} = 28.0V, V_{OUT} = 36.0V, I_{OUT} = 3.33A	**1.2**	1.33	**1.45**	MHz
	F_{SW}	Over rated line, trim and temperature, up to 3.34A load and exclusive of burst mode	**0.7**		**1.45**	MHz
		Over rated line, trim and temperature, up to 5.56A load and exclusive of burst mode	**0.45**		**1.45**	MHz
Output Capacitance (internal)	C_{OUT_INT}	Effective value, V_{OUT} = 36.0V		26		µF
Output Capacitance (internal) ESR	R_{C-OUT}	Effective value, V_{OUT} = 36.0V		2		mΩ
Output Turn-On Delay	t_{OFF}	From V_{IN} first crossing $V_{IN-UVLO+}$ to soft-start ramp, PC floating		97	**144**	ms
Output Voltage Rise Time	$t_{RISE-VOUT}$	From soft-start begin to V_{OUT} settled to within 5%, no external SC capacitor	**4.0**	8.0	**12.0**	ms
Efficiency, Ambient	η_{AMB}	V_{IN} = 28.0V, V_{OUT} = 36.0V, I_{OUT} = 5.56A, T_{CASE} = 25°C	95.0	95.5		%
		V_{IN} = 28.0V, V_{OUT} = 36.0V, I_{OUT} = 3.34A, T_{CASE} = 25°C	93.8	94.2		%
Efficiency, Hot	η_{HOT}	V_{IN} = 28.0V, V_{OUT} = 36.0V, I_{OUT} = 5.56A, T_{CASE} = 100°C	94.0	95.4		%
		V_{IN} = 28.0V, V_{OUT} = 36.0V, I_{OUT} = 3.34A, T_{CASE} = 100°C	93.0	94.3		%
Output Voltage Ripple	V_{OUT_PP}	V_{IN} = 28.0V, V_{OUT} = 36.0V, I_{OUT} = 5.56A, $C_{OUT-EXT}$ = 0µF, 20MHz BW		225		mV_{P-P}
Load Capacitance (Electrolytic)	$C_{LOAD-ALEL}$	0.1Ω ≤ ESR ≤ 1Ω, effective value at PRM output	**0**		**63**	µF
Load Capacitance (Ceramic)	$C_{LOAD-CER}$	2mΩ ≤ ESR ≤ 200mΩ, effective value at PRM output	**0**		**25**	µF
Load Capacitance (Total)	$C_{LOAD-TOTAL}$	See Figure 27, effective value at PRM output	**0**		**63**	µF
Load Transient Voltage Deviation	V_{TRANS}	10% ↔ 100% load step, 10A/µs, $C_{OUT-EXT}$ = 0µF, deviation from initial set point		1.04	**1.35**	V
Load Transient Recovery Time	t_{TRANS}	10% ↔ 100% load step, 10A/µs, $C_{OUT-EXT}$ = 0µF, settled to within 10% final value (AL inactive)		150		µs

Electrical Specifications (Cont.)

Specifications apply over all line, load and trim voltage conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –55°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protections						
Input Undervoltage Turn-ON	V_{IN_UVLO+}	Powertrain recovery		13.5	**14.0**	V
Input Undervoltage Turn-OFF	$V_{IN\_UVLO–}$	Powertrain shut down	**12.0**	12.7	**13.8**	V
Input Undervoltage Hysteresis	$V_{IN\_UVLO\_HYST}$	$(V_{IN\_UVLO+}) – (V_{IN\_UVLO–})$	**0.2**	0.8	**2.0**	V
Input Overvoltage Turn-ON	$V_{IN\_OVLO–}$	Powertrain recovery	**50.2**	51.3		V
Input Overvoltage Turn-OFF	V_{IN_OVLO+}	Powertrain shut down		52.9	**56.0**	V
Input Overvoltage Hysteresis	$V_{IN\_OVLO\_HYST}$	$(V_{IN\_OVLO+}) – (V_{IN\_OVLO–})$	**0.2**	1.6	**5.8**	V
Output Overvoltage Turn-OFF	V_{OUT_OVP}		**54**	56	**60**	V
Minimum Current Limited V_{OUT}	V_{OUT_UVP}				**4.0**	V
Overtemperature Shut-Down Set Point	T_{OTP}	Controller temperature	130			°C
Fault Protection Response Time	t_{PROT}			1		µs
Fault Protection Recovery Time	$t_{PROT-RECOVERY}$			100		ms

Signal Specifications

Specifications apply over all line, load and trim voltage conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –55°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

VC: VTM™ Control								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Power Output	Start Up	VC Voltage	V_{VC_START}	I_{VC} = 400mA	**12**	13	**16**	V
		VC Available Current	I_{VC_START}	V_{VC} = 12V	**200**			mA
		VC Pulse Duration	t_{VC}		**7**	10	**16**	ms
		PC to VC Delay	t_{PC_VC}			18	**50**	µs
Analog Input/Output	AL Operation	CD to VC Transfer Function	I_{VC} / I_{CD}		**7.76**	8.00	**8.24**	A/A
		VC Rated Current	I_{VC_ALCOMP}		**0**		**2**	mA
		VC Voltage Range for AL Compensation	V_{VC_ALCOMP}		**0**		**2**	V
		VC to V_{REF} Transfer Function	V_{REF} / V_{VC_ALCOMP}		**59**	62.5	**66**	V/V
		Rated V_{REF} AL Comp. Range	V_{REF_AL+}		**0**		**125**	mV

VH: Auxiliary Voltage								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Output	Normal Operation	VH Voltage	V_{VH}	Over rated VH load current	**8.7**	9.0	**9.3**	V
		VH Rated Current	I_{VH}				**5**	mA
	Any	VH Rated External Bypass Capacitor	C_{VH-EXT}	If required, bypass to SG only			**30**	nF
	Standby	VH Fault Voltage	V_{VH_FLT}			0		V
	Transition	PC to VH Delay	t_{PC_VH}			1.0	**5.0**	ms
		VH Fault Response Time	t_{FR_VH}	To VH < 1.5V		290	**500**	µs

PC: Primary Control								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Output	Normal Operation	PC Voltage	V_{PC}	No external load	**4.7**	5.0	**5.3**	V
		PC Current	I_{PC}				**1.8**	mA
Digital Input/Output	Standby	PC Voltage	$V_{PC\_DISABLE}$		**1.85**	2.35		V
		PC Bias Current	$I_{PC\_DISABLE}$	After t_{OFF}, V_{PC} = 0V. Start up is assured with >100kΩ load on PC	**60**	90		µA
	Transition	PC Enable Hysteresis	V_{PC_HYSTER}			150		mV
	Start Up	PC Voltage	V_{PC_ENABLE}			2.5	**3.0**	V
		PC Delay Time	t_{ON}	V_{IN} pre-applied	**0.6**	1.0	**5.0**	ms

Signal Specifications (Cont.)

Specifications apply over all line, load and trim voltage conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –55°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

SC: Secondary Control								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Input	Normal Operation	SC Voltage	V_{SC}	No external connection to SC	**1.182**	1.222	**1.262**	V
		SC Voltage Trim Range	V_{SC_TRIM}		**0.25**		**V_{SC}**	V
	Any	SC series R to VREF	R_{SC_INT}		**9.9**	10.0	**10.1**	kΩ
		SC Bypassing to SG	C_{SC_INT}			0.22		µF
		SC Bypassing to SG, External	C_{SC_EXT}		**0**		**1.0**	µF
	Transition	PC to SC Delay	t_{PC_SC}			1.0	**5.0**	ms
		SC Fault Response Time	t_{FR_SC}			19.5	**50**	µs

TM: Temperature Monitor								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Output	Normal Operation	TM Voltage	V_{TM_AMB}	Controller temperature = 27°C	**2.95**	3.00	**3.05**	V
		TM Voltage Range	V_{TM}		**2.14**		**4.20**	V
		TM Gain	A_{TM}			10		mV/°C
		TM Rated Current	I_{TM_NORMAL}				**100**	µA
		TM Ripple	V_{TM-PP}	Powertrain in burst mode		75		mV_{P-P}
	Standby	TM Fault Current	I_{TM_FAULT}	High-impedance state		0		mA
	Transition	PC to TM Delay	t_{PC_TM}			18.0	**50**	µs
		TM Fault Response Time	t_{FR_TM}			1.0	**2.0**	µs

SG: Signal Ground								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Reference	Any	Rated SG Current	I_{SG}		**–100**		**100**	mA

Signal Specifications (Cont.)

Specifications apply over all line, load and trim voltage conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –55°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

IL: Current Limit Adjust								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Input	Normal Operation	IL Voltage Setpoint	V_{IL_SET}			1.00		V
		IL Resistance to V_{IL_SET}	R_{IL}			5		kΩ
		IL Voltage range	V_{IL}		**0.10**			V
		IL external resistor range	$R_{IL\text{-}RNG}$		**440**		**open**	Ω

OS: Output Set								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Input	Any	OS Internal Series Resistor	$R_{OS\_SERIES\_INT}$		**79.8**	80.6	**81.4**	Ω
		OS Internal Top Resistor	$R_{OS\_TOP\_INT}$		**69.1**	69.8	**70.5**	kΩ
		OS External Resistor Range	R_{OS_SG}	With SC at nominal	1.67	2.37	3.36	kΩ

PR: Control Node Port								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Output	Normal Operation	PR Active Range	V_{PR}		**0.79**		**7.4**	V
		PR Available Current	I_{PR}		**2.0**			mA

CD: Compensation Device								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Input/Output	AL Operation	CD Voltage Range	V_{CD}	0 – 5.56A range	**0**		**0.29**	V
		CD Rated Current	I_{CD}				**250**	µA
		CD Resistor Range	R_{CD}		**1.16**			kΩ

Specified Operating Area

The following figures present typical performance at T_{CASE} = 25ºC, unless otherwise noted. See associated figures for general trend data.

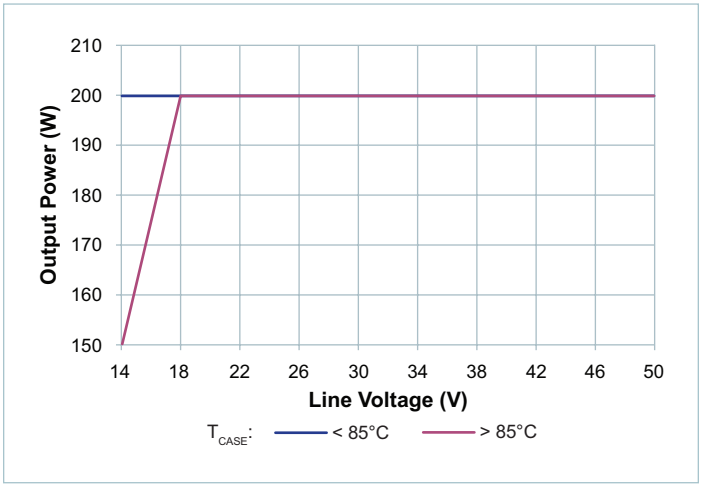


Figure 1 — *Rated output power vs line voltage, nominal trim and above*

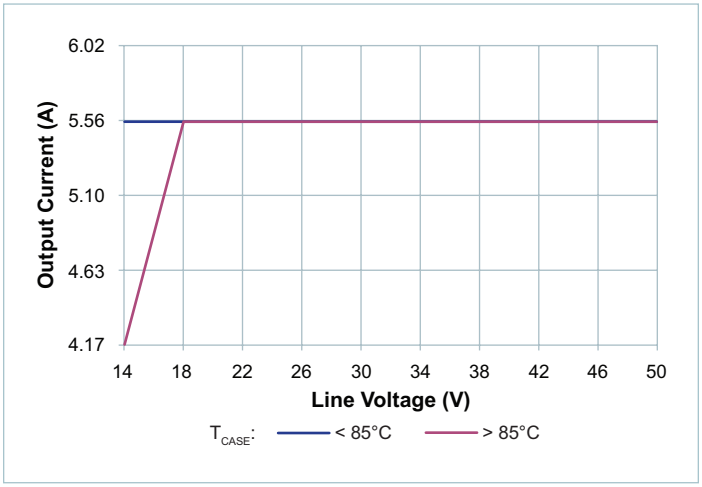


Figure 2 — *Rated output current vs. line voltage, nominal trim and below*

Typical Performance Characteristics

The following figures present typical performance at T_{CASE} = 25ºC, unless otherwise noted. See associated figures for general trend data.

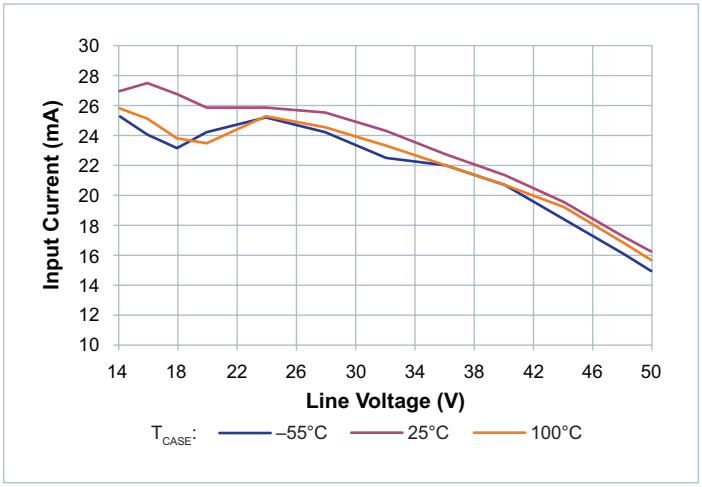


Figure 3 — *Disabled input current vs. line voltage*

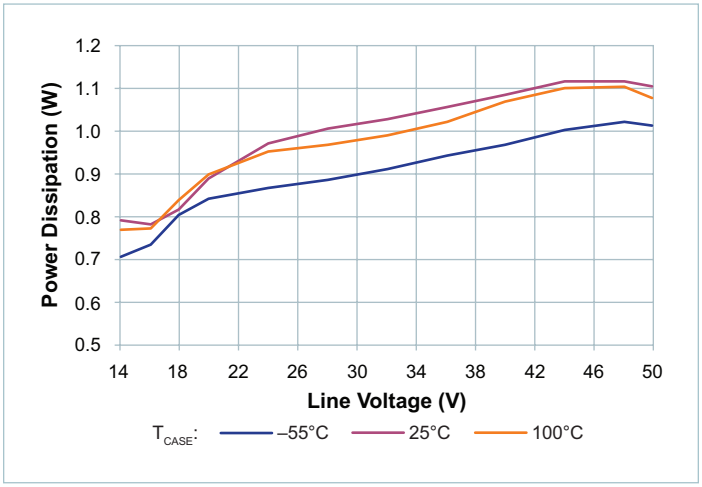


Figure 4 — *No-load power dissipation vs. V_{IN} at nominal trim*

Typical Performance Characteristics (Cont.)

The following figures present typical performance at T_{CASE} = 25°C, unless otherwise noted. See associated figures for general trend data.

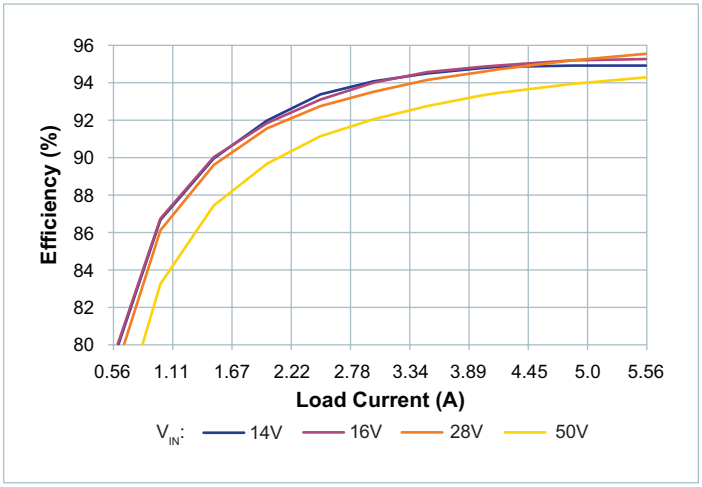


Figure 5 — *Efficiency at 25°C case temperature, V_{OUT} = 26V*

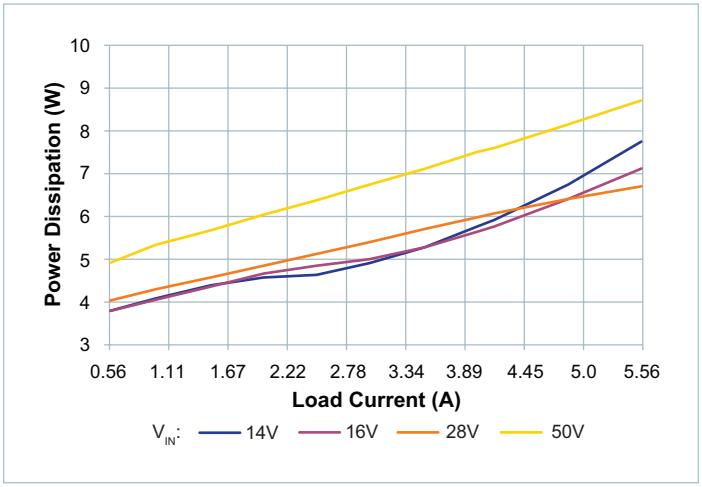


Figure 6 — *Power dissipation at 25°C case temperature, V_{OUT} = 26V*

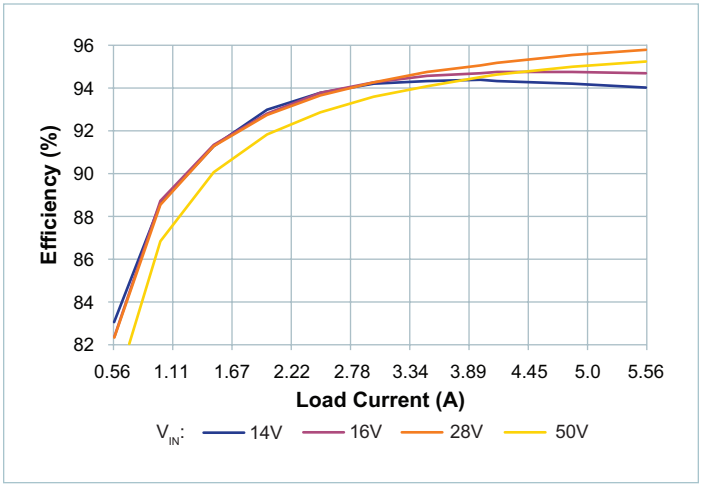


Figure 7 — *Efficiency at 25°C case temperature, V_{OUT} = 36V*

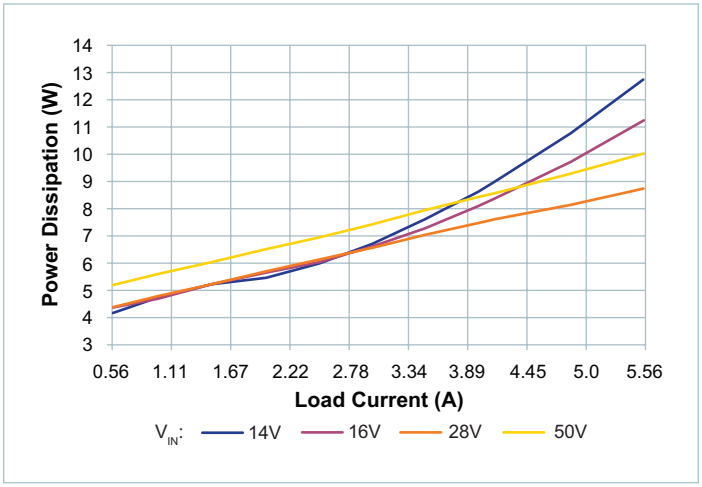


Figure 8 — *Power dissipation at 25°C case temperature, V_{OUT} = 36V*

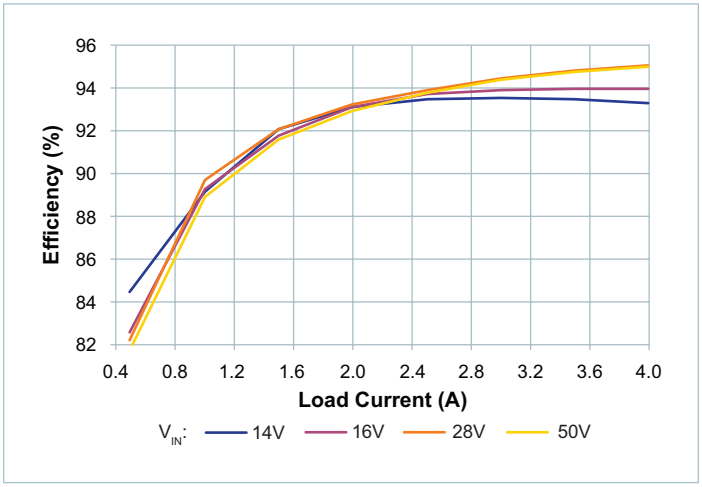


Figure 9 — *Efficiency at 25°C case temperature, V_{OUT} = 50V*

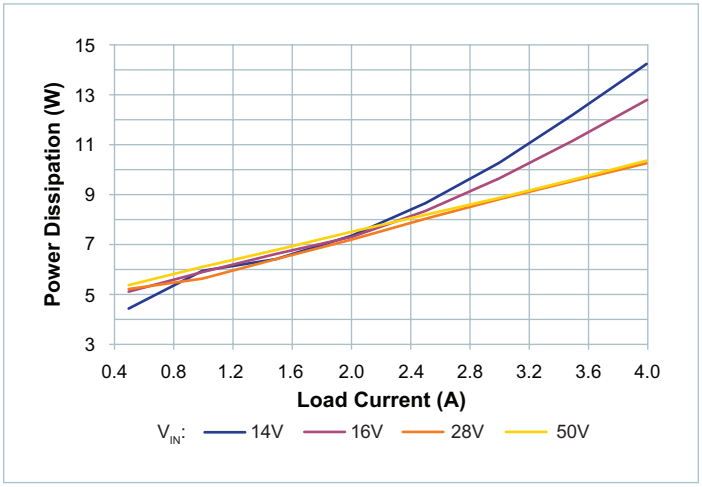


Figure 10 — *Power dissipation at 25°C case temperature, V_{OUT} = 50V*

Typical Performance Characteristics (Cont.)

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

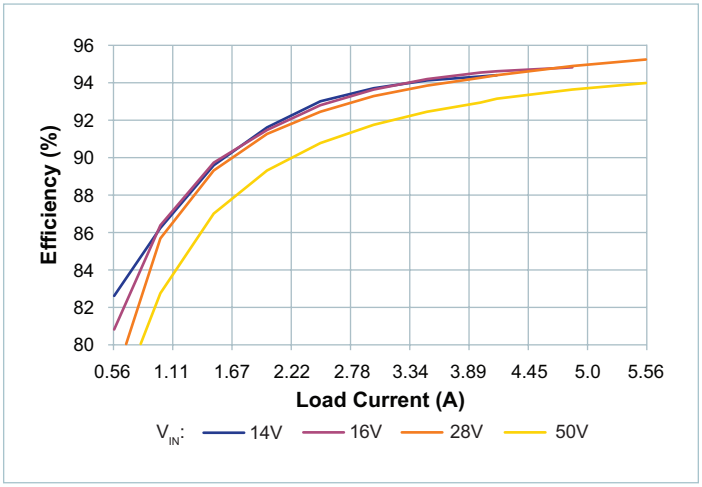


Figure 11 — *Efficiency at 100°C case temperature, V_{OUT} = 26V*

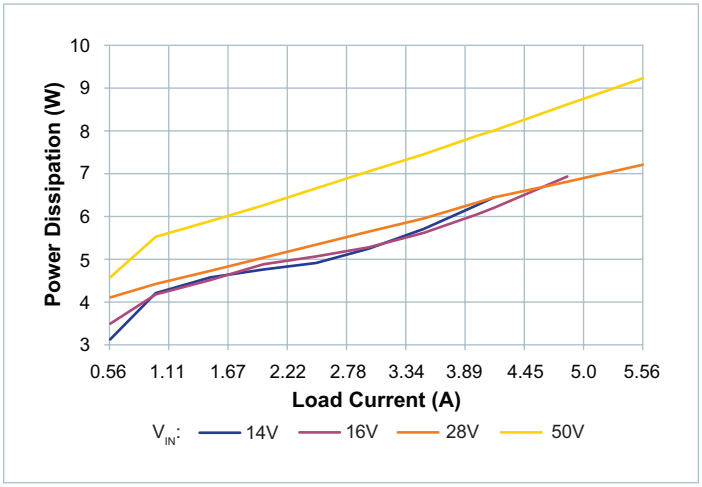


Figure 12 — *Power dissipation at 100°C case temperature, V_{OUT} = 26V*

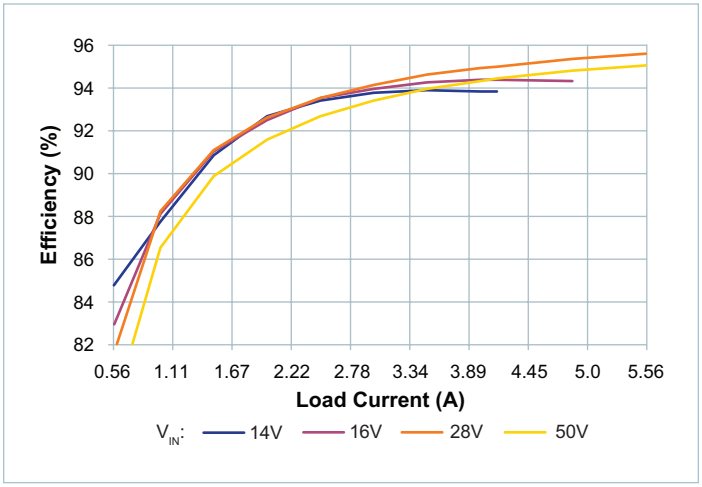


Figure 13 — *Efficiency at 100°C case temperature, V_{OUT} = 36V*

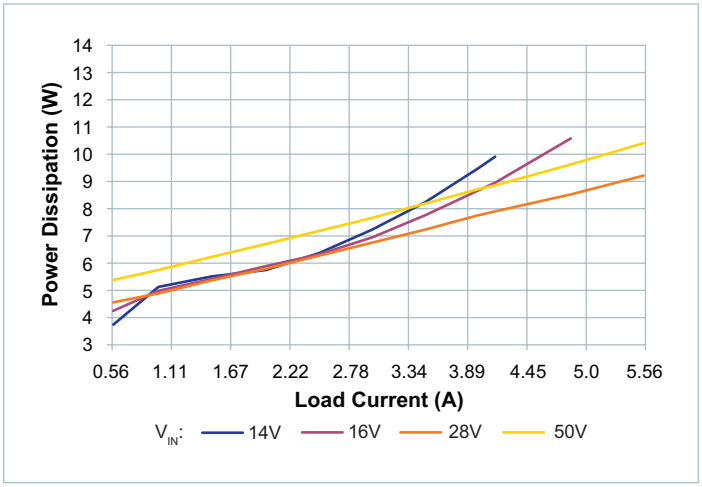


Figure 14 — *Power dissipation at 100°C case temperature, V_{OUT} = 36V*

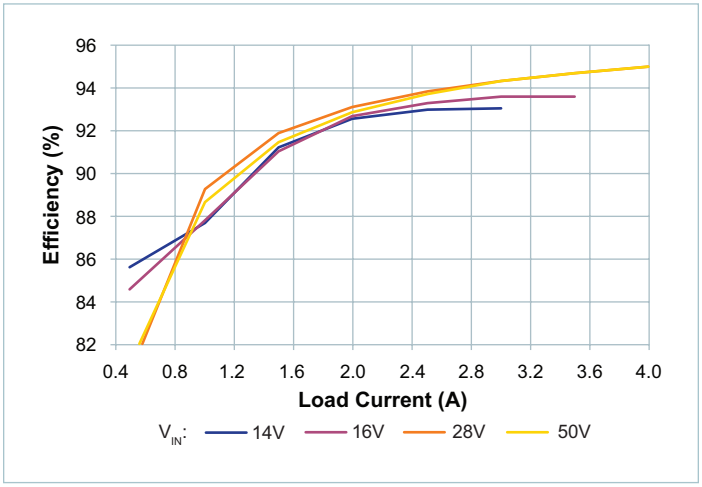


Figure 15 — *Efficiency at 100°C case temperature, V_{OUT} = 50V*

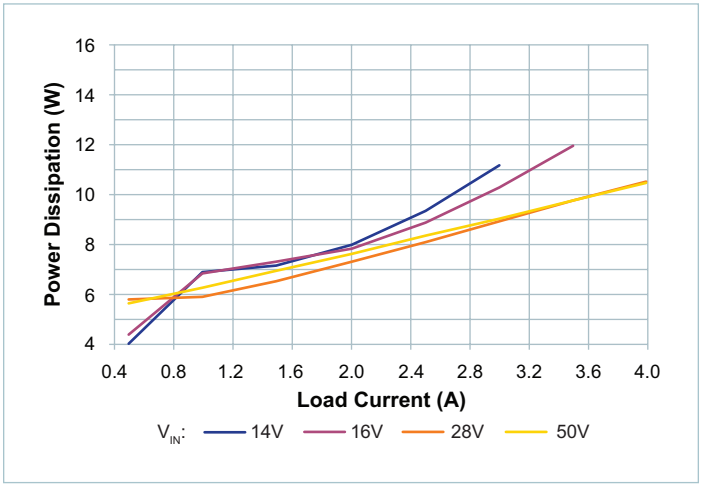


Figure 16 — *Power dissipation at 100°C case temperature, V_{OUT} = 50V*

Typical Performance Characteristics (Cont.)

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

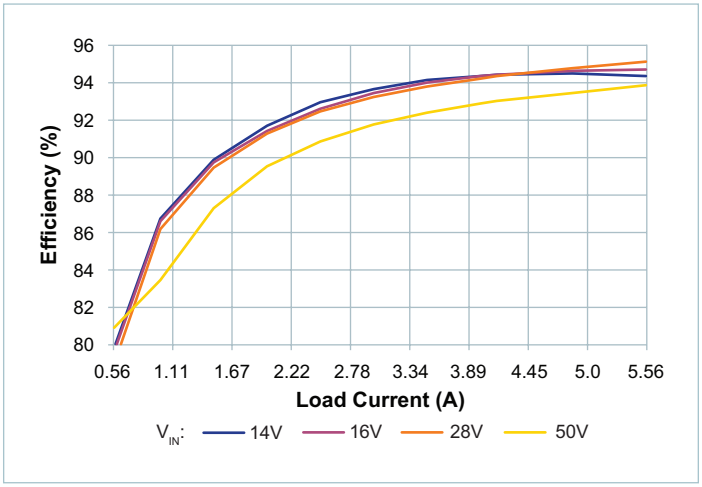


Figure 17 — *Efficiency at –55°C case temperature, V_{OUT} = 26V*

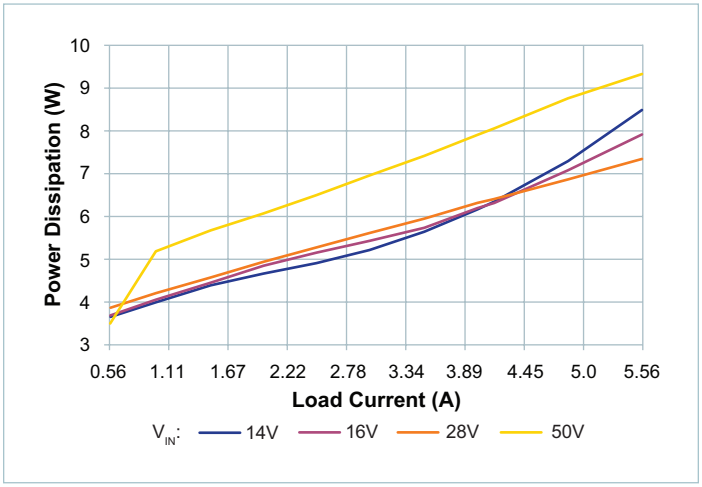


Figure 18 — *Power dissipation at –55°C case temperature, V_{OUT} = 26V*

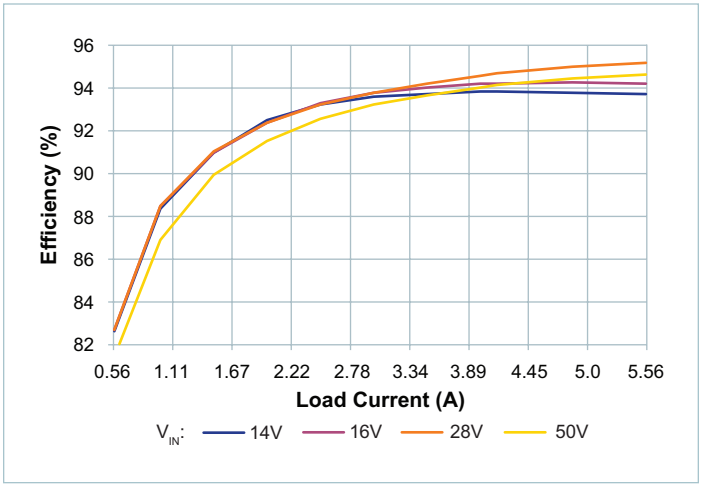


Figure 19 — *Efficiency at –55°C case temperature, V_{OUT} = 36V*

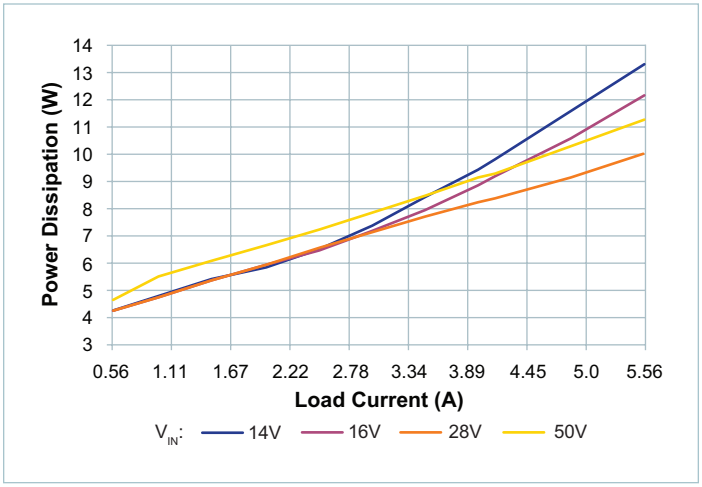


Figure 20 — *Power dissipation at –55°C case temperature, V_{OUT} = 36V*

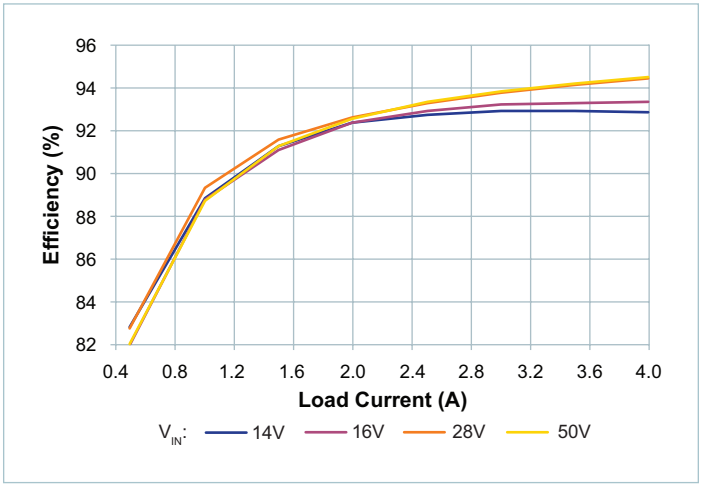


Figure 21 — *Efficiency at –55°C case temperature, V_{OUT} = 50V*

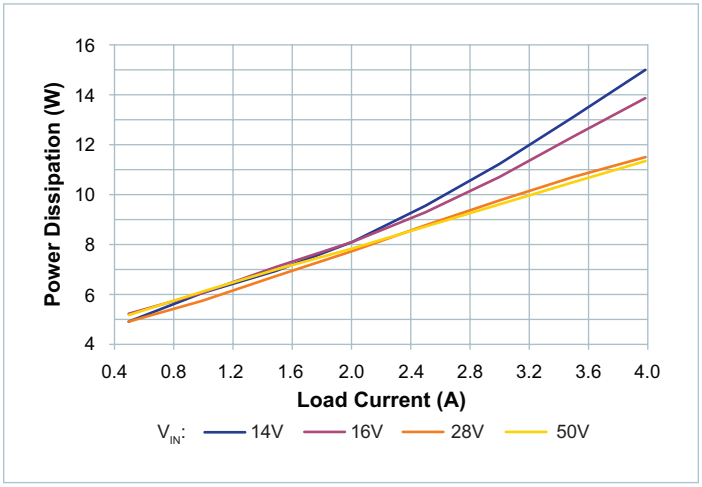


Figure 22 — *Power dissipation at –55°C case temperature, V_{OUT} = 50V*

Pin Functions

+IN, –IN

Input power pins.

+OUT, –OUT

Output power pins. –OUT uses a low-side current shunt to sense the PRM output return current, therefore do not connect –OUT to –IN since this would defeat this current measurement and could lead to loss of output overcurrent protection or anomalous adaptive-loop and constant current-limiting behavior.

VC: VTM™ Control

VC supplies power to one or two downstream VTMs during start up. When the PRM is not connected to any VTM and the AL function is unused, no VC connection is required, but a 1kΩ resistor from VC to –OUT is permitted for backward compatibility.

When AL compensation is used, after the start-up pulse, VC is a small current source proportional to module I_{OUT} and R_{CD}. A resistor inside the downstream VTM from VC to –OUT sets the dynamic voltage on VC, which is scaled and summed into the error amplifier reference.

VH: Auxiliary Voltage Source

VH is an auxiliary supply voltage referred to SG. It is active when the PRM is operating. VH can be used as a supply for low-power external control circuitry. To avoid electrical overstress to the module, do not overload VH or exceed its maximum bypass capacitor rating.

PC: Primary Control

PC turns the PRM on and off. PC has an internal current source to pull it to the enabled state if no external connection is made. External control of PC should be implemented using an open collector opto-coupler or transistor configuration that cannot drive the pin to a high state. Attempting to drive PC high with an external voltage source could cause electrical overstress to the PRM.

SC: Secondary Control

SC is driven by the internal voltage reference through $R_{SC\text{-}INT}$. It is summed with the output of the AL Compensation system to provide the voltage reference for the error amplifier. An external programming DAC or fixed resistor to SG can be used to set SC to voltages lower than V_{SC} for dynamic trimming or output margining. Trimming with this method will preserve the AL compensation scaling as well as the control loop compensation factors. A capacitor from SC to SG can be used to slow down the soft-start output voltage slew rate.

TM: Temperature Monitor

Once the PRM has started, TM outputs a voltage proportional to the internal controller temperature. The voltage is A_{TM}* temperature (°C), and so at room temperature of 27°C the nominal TM voltage will be 3.00V. TM can be used as a "power good" flag to indicate PRM operation, provided that it is not loaded in excess of its current rating.

SG: Signal Ground

This is a low-current pin which provides a Kelvin connection to the PRMs internal signal ground. Use this pin as the ground reference for external circuitry and signals to avoid voltage drops caused by high currents on input power return. SC is the ground reference for PC, OS, CD, SC, VH and IL ports. Note that VC current should return to –OUT and not SG.

IL: Current Limit Adjust

During operation, the PRM features constant-current-style output current limiting, where IL sets the constant current threshold. By adding a resistor R_{IL} from IL to SG, the current limit threshold can be reduced and the module will operate in constant-current when the load current exceeds the programmed value. If full rated current is needed or if constant current limiting is not needed, then this pin should be left open. Note that this functionality is enhanced compared to the MP028x036M12AL product fault protection response to a slow current limit.

PR: Control Node Port

PR is the error amplifier output and is proportional to PRM output power. No external connection to PR is needed.

OS: Output Set

OS provides access to the error amplifier inverting input through an internal low-value resistor. An external resistor from OS to SG is required to set the scale factor of the feedback from the PRM output voltage to the control loop.

CD: Compensation Device

CD is used to set the adaptive-loop scale factor. CD is a voltage source proportional to I_{OUT}, and an external resistor to SG programs the resulting CD current. This current then acts on the VC port to develop the added voltage to the control loop to increase V_{OUT}. When adaptive-loop compensation is not needed, CD should be left open with no external connection.

Functional Description

The MPRM28Ax360M120A00 is a non-isolated ZVS buck-boost regulator. It is specifically designed to provide a controlled factorized-bus distribution voltage for powering a downstream VTM transformer.

The PRM can be configured for two operating modes depending on the application need. In applications with a downstream VTM, the adaptive-loop regulation circuitry within the PRM can be configured with a negative load line to compensate for the effective output resistance of the VTM, without the need for a direct remote sense connection. This permits the resultant system to preserve the isolation offered by the VTM transformer stage.

In applications without a VTM, the adaptive-loop circuitry can be deactivated, allowing the PRM to serve as a general-purpose regulator, with tight regulation provided at the module output.

PRM Start Up

Any time the PRM input voltage is within UVLO and OVLO and the module is not disabled via the PC pin, it will attempt to start.

At start up, VH goes active and the VC pulse starts. The PRM internal reference rises to generate the soft-start ramp of module output voltage. The soft-start time can be increased by the addition of a capacitor on SC. When a VTM is used, care must be taken not to increase the soft-start time so much that the VTM faults at the end of the VC pulse due to undervoltage lockout.

Burst Mode

The PRM features a hysteretic pulse-skipping mode. At light-load conditions, switching cycles can be skipped in order to significantly reduce gate-drive power and improve efficiency. The regulator will automatically enter and exit burst mode based on load. Depending on line and trim operating conditions, occasional skipping of one or many switching cycles. When the input voltage is 16V or higher, a minimum load of 20W will generally cause the PRM to exit burst mode for all output voltage trim levels.

Variable-Frequency Operation

The PRM is pre-programmed to a fixed, maximum base operating frequency. The maximum processed power determines the base frequency and associated power inductor with respect to other constraints to achieve peak efficiency at nominal operation. The operating frequency can be reduced from the base frequency as needed to maintain rated power capability at certain line voltage, trim voltage and load conditions. By reducing the operating frequency, or stretching the period of each switching cycle, the ZVS operation is preserved throughout the input line voltage range maintaining optimum efficiency.

Excluding burst mode, the MPRM28Ax360M120A00 operates at fixed frequency across the output voltage trim range for loads up to 3.3A, for line voltages down to 21V.

PRM Fault Response

The PRM includes several fault protection mechanisms to help prevent damage or overstress to the module. When a fault is detected, the PRM will shut down and restart after $t_{PROT\text{-}RECOVERY}$, and once the fault condition is no longer detected.

Design Guidelines

Input Filter Stability

Regulating switch-mode power supplies like the PRM present a negative impedance to the voltage source that is powering them. To ensure stability of the regulation loop, the source impedance and the parasitic resistance and inductance of the interconnect lines must be considered. The high performance ceramic decoupling capacitors placed locally to the input to the PRM are effective in controlling reflected ripple current at the switching frequency. However their low ESR means they will not significantly damp an excessively high impedance of an upstream voltage source.

The regulator dynamic input impedance magnitude r_{EQ_IN} can be calculated by dividing the lowest line voltage by the full load input current. To ensure stability, two cases must be considered.

Input Filter case 1; inductive source and local, external, input decoupling capacitance with negligible ESR (i.e., ceramic type)

The voltage source impedance can be modeled as a series R_{LINE} L_{LINE} circuit. In order to guarantee stability the following conditions must be verified:

$$R_{LINE} > \frac{L_{LINE}}{(C_{IN} + C_{IN\_EXT}) \bullet \left| r_{EQ\_IN} \right|} \qquad (1)$$

$$R_{LINE} << \left| r_{EQ\_IN} \right| \qquad (2)$$

Notice that the local high-performance ceramic input capacitors should be included for this purpose. Equation 2 means that the line source impedance should be <10% of the regulator dynamic input resistance r_{EQ_IN}. for best performance, but the line source impedance must <50% of r_{EQ_IN}. However, R_{LINE} cannot be made arbitrarily low otherwise Equation 1 is violated and the system will show instability, due to under-damped RLC input network.

Input Filter case 2; inductive source and internal, external input decoupling capacitance with significant $R_{C_{IN\_EXT}}$ ESR (i.e., electrolytic type)

In order to simplify the analysis in this case, the input source impedance can be modeled as a simple inductor L_{LINE}. Notice that, the internal high-performance ceramic capacitors C_{IN} directly at the input of the PRM should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$\left| r_{EQ\_IN} \right| > R_{C_{IN\_EXT}} \qquad (3)$$

$$\frac{L_{LINE}}{(C_{IN\_EXT} \bullet R_{C_{IN\_EXT}})} < \left| r_{EQ\_IN} \right| \qquad (4)$$

Equation 4 shows that if the aggregate ESR is too small – for example by using only high-Q ceramic input capacitors (C_{IN_EXT}) – the system will be under-damped and may not be stable. As with Equation 2 above, a decade of margin in satisfying Equation 3 is preferred, but an octave of margin is considered the minimum.

Additional information can be found in the filter design application note AN:023. Also, refer to the Vicor online input filter design tool to ensure input stability. Lastly, consider the PRM maximum input voltage slew rate dV_{IN}/dt, which is needed to prevent overstress to input stage components in the module. Additional circuitry may be required at the PRM input if the filter solution can exceed that slew rate.

Input Fuse Recommendations

A fuse should be incorporated at the input to the PRM, in series with the +IN pin. A 20A or smaller input fuse (Littelfuse® NANO²® 451, 453 or 456 Series) is required to safety agency conditions of acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

Output Voltage Set Point

Output voltage trim is programmed with R_{OS}. R_{OS} is a resistor placed from the OS pin to SG and forms the bottom of the resistive divider that provides feedback to the voltage control loop. R_{OS} is required, and if it is not present, the PRM will regulate to 1.222V, or may not start at all.

For a desired output voltage $V_{OUT-PRM}$, R_{OS} is calculated as follows:

$$R_{OS}(\Omega) = \frac{V_{SC}}{V_{OUT} - V_{SC}} \bullet 69{,}800 - 80.6$$

Or in the typical case where SC is not used for margining, the equation is simply:

$$R_{OS}(\Omega) = \frac{1.222}{V_{OUT} - 1.222} \bullet 69{,}800 - 80.6$$

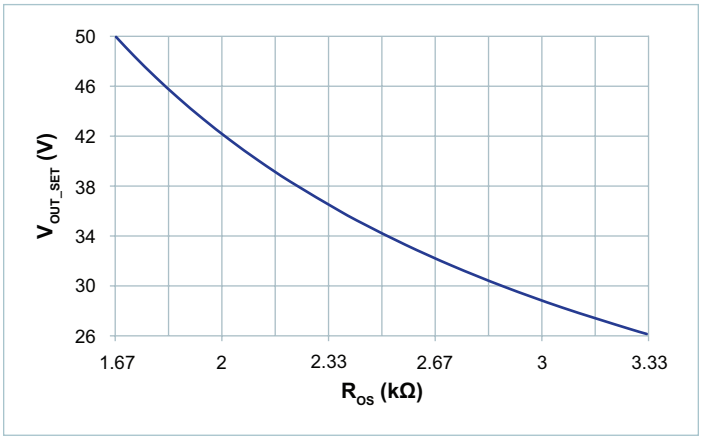


Figure 23 — *PRM output voltage set point determined by value of R_{OS}*

Output Voltage Margining

A PRM system configured for adaptive-loop compensation has values for R_{VC} and R_{CD} which are established based on R_{OS}. In cases where the output needs to temporarily be margined down to a lower value, it is simpler to leave the values of R_{OS}, and R_{CD} intact, and instead lower the internal reference voltage. R_{SC} is an optional resistor placed from the SC pin to SG, and is used to reduce the input voltage reference.

For a system with output voltage programmed to V_{NORMAL} using R_{OS}, the output voltage can be reduced to V_{MARGIN} with R_{SC} according to:

$$R_{SC}(k\Omega) = \frac{V_{MARGIN}}{V_{NORMAL} - V_{MARGIN}} \bullet 10$$

SC should not be programmed lower than the minimum SC voltage V_{SC_TRIM}, which occurs with an R_{SC} of approximately 2.57kΩ.

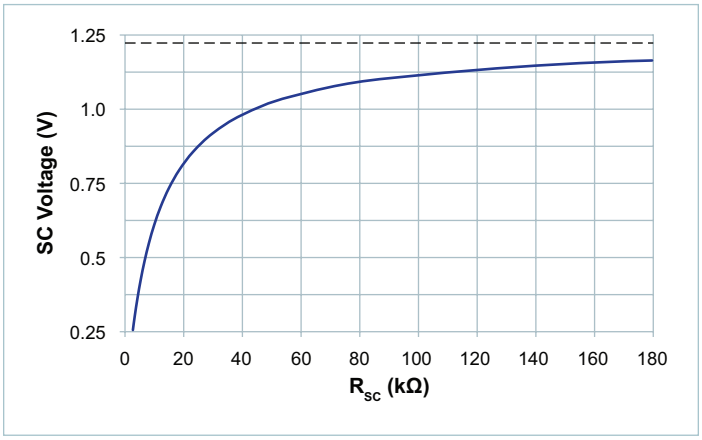


Figure 24 — *Temporary margining to a lower value using optional resistor R_{SC}*

Output Voltage Start-Up Rise Time Setting

The voltage control loop reference V_{SC} has a series resistance R_{SC_INT} and shunt capacitance C_{SC_INT}. The output voltage rise time is exponential, with a default time constant of 2.2ms. The module output voltage will settle to within 5% of the final value after approximately 6.5ms.

C_{SC_EXT} is an optional external capacitor placed from the SC pin to SG. Electrically it appears in parallel with C_{SC_INT}, and can therefore be used to increase the time constant and slow down the rise time at startup. In general the time constant of the reference is given by:

$$\tau = R_{SC\_INT} \bullet \left(C_{SC\_INT} + C_{SC\_EXT}\right)$$

With the maximum rated C_{SC_EXT} value, the module time constant will be ~12.2ms. In cases where a VTM follows the PRM, care must be taken that the PRM module output voltage achieves the UVLO threshold of the VTM before the end of the PRM's VC pulse.

Adaptive-Loop Compensation Setting

A factorized power system naturally has a DC load line associated with it since the regulator stage (PRM) is regulating before the isolation and voltage transformation stage (VTM™), and there are finite resistances in the system including the factorized bus resistance, the VTM stage effective output resistance, and round trip bus resistance between the VTM and the point of load.

Consider a factorized power system with the following parameters:

- $V_{LOAD\_DESIRED}$ = 3.3V
- R_{LOAD_BUS} = 1.0mΩ at 25°C
- VTM model MVTM36BF045M027B00:
  - K_{VTM} = 1/8
  - $R_{OUT\_VTM\_INT}$ = 6mΩ at 25°C
- $R_{FACTORIZED\_BUS}$ = 17mΩ
- V_F = 26.4V

The effective system output resistance is:

$$R_{OUT\_SYSTEM}(\Omega) = R_{LOAD\_BUS} + R_{OUT-VTM\_INT} + \frac{R_{FACTORIZED\_BUS}}{K_{VTM}^{\,2}}$$

At no load the output voltage at the load will be equal to the factorized bus voltage V_F, multiplied by the VTM K factor, K_{VTM}, or 3.3V. Because the PRM regulates against the factorized-bus voltage, the voltage at the load will sag at a rate directly proportional to the effective resistance between that point and the load. At the full rated 27A current for this VTM, the load voltage will drop by 196mV to ~3.1V due to the load line of this resistance. If the presence of this load line is acceptable for an application, then the PRM should be trimmed by way of R_{OS} alone, and further compensation is not necessary.

If tighter output voltage regulation is desired, then the load line can be effectively canceled by way of the PRM's adaptive-loop (AL) engine. The AL engine measures the output current of the PRM and increases the PRM's output voltage in response, emulating a fixed negative resistance.

Setting the Adaptive-Loop Load Line

To determine an appropriate value for the PRM's adaptive-loop compensation slope, R_{LL_AL} it helps to reflect the VTM's output resistance and round-trip load bus resistances to the input side of the VTM. The VTM's internal effective output resistance and the round-trip resistance between the load and the VTM output are reflected to the VTM's input scaled by the square of its transformation ratio K_{VTM}. For the factorized-power system above, the output resistance would reflect to the VTM's input as 448mΩ. The factorized-bus wiring and any filtering components is then be directly added to that. In the example power system we consider, this total is 465mΩ. This becomes R_{LL_AL}, the amount of resistance we would like the PRM AL engine to cancel.

Programming the PRM's adaptive-loop compensation is done with R_{CD}, a resistor connected between the CD pin and the SG pin. The value of R_{CD} depends on the resistance we want the AL engine to cancel, and also R_{VC} (the resistance seen by the PRM at its VC pin) and R_{OS}, according to the following general formula:

$$R_{CD}(\Omega) = \frac{R_{VC}}{R_{LL\_AL}} \bullet 20.458 \bullet 10^{-3}\left(\frac{85296}{R_{OS} + 80.6} + 1.222\right)$$

R_{CD} can alternately be expressed in terms of the PRM output voltage set point instead of R_{OS} according to:

$$R_{CD}(\Omega) = \frac{R_{VC}}{R_{LL\_AL}} \bullet \frac{V_{OUT\_PRM}}{48.88}$$

Note the lack of an R_{SC} term, which indicates that AL compensation is unchanged with subsequent voltage margining.

A system with a VTM includes R_{VC} internal to the VTM, and the VTM data sheet will list the value. If the adaptive-loop compensation is to be used when a VTM is not present, an external 1kΩ resistor should be added between the PRM's VC pin and the PRM's –OUT terminal. Any use of the CD pin for AL compensation requires the PRM VC pin have finite terminating resistance to SG.

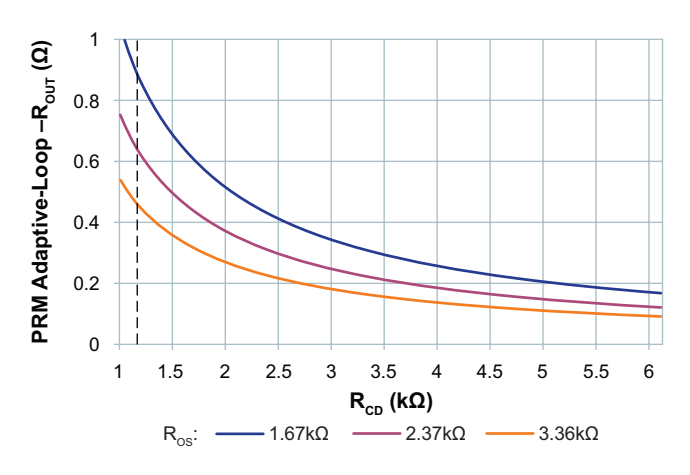


Figure 25 — *Programming the adaptive-loop compensation with R_{VC} = 1kΩ*

Returning to the example factorized-power system which uses the MVTM36BF045M027B00, the value for R_{VC_INT} is given as R_{VC} = 1kΩ from the data sheet, and the R_{OS} needed to trim the PRM to 26.4V is R_{OS} = 3.31kΩ. To cancel the R_{LL_AL} of 465mΩ, the equations show we need an R_{CD} of 1.16kΩ.

Current Limit

In some applications, a constant current limiting type response is valuable, where the module will automatically transition between regulating constant voltage and regulating constant current, in response to the load. The MPRM28Ax360M120A00 includes a programmable constant-current limit threshold which can be used for this purpose.

By default, the PRM will regulate output voltage across the full range of rated current or power. In cases where the load exceeds the capability of the PRM, the module will shut down due to overcurrent or short-circuit protection, and no constant-current operation will occur. R_{IL} is an optional resistor placed from the IL pin to SG and is used to program the constant-current threshold. When the threshold is set lower than the module rated current I_{OUT}, the module will enter constant-current regulation when the load exceeds the threshold, instead of shutting down. The nominal constant-current threshold can be programmed with $R_{(IL)}$ according to:

$$R_{IL}\,(k\Omega) = \frac{I_{CL}}{6.66 - I_{CL}} \bullet 4$$

The minimum value $R_{IL\text{-}RNG}$ will set the output current limit to 0.67A.

Note that once in current limit, the PRM output voltage will drop below the programmed voltage regulation point in order to regulate current. If the load is high impedance or is itself a constant current type load, the output voltage of the PRM will drop without bound. The VTM™ will shut down if its input voltage falls below its rated V_{IN} range, and the PRM will shut down if its V_{OUT} falls below V_{OUT_UVP}.

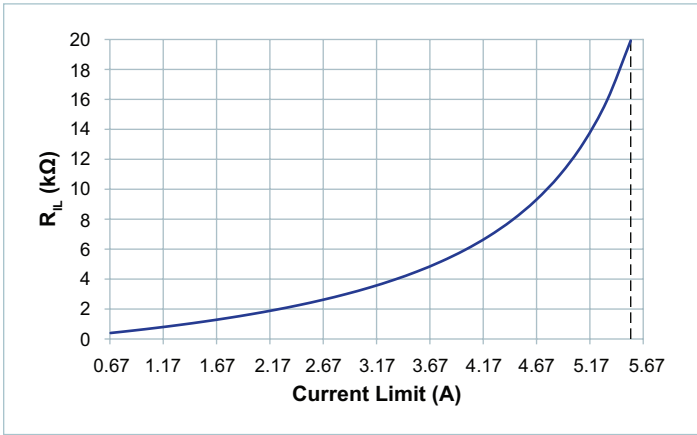


Figure 26 — *Programming the constant-current limit threshold with R_{IL}*

The constant-current limit also allows the PRM to be used to charge and maintain a battery, with automatic transition between CC and CV regulation schemes.

Note that for loads that are higher impedance than a battery with fast current rise times, the PRM may exhibit multiple instances of fast current limit before the current-regulation loop has settled. During fast current limit, the powertrain will stop processing power for approximately 50µs, and then automatically resume switching. This behavior is by design, but during this time the output is not regulated.

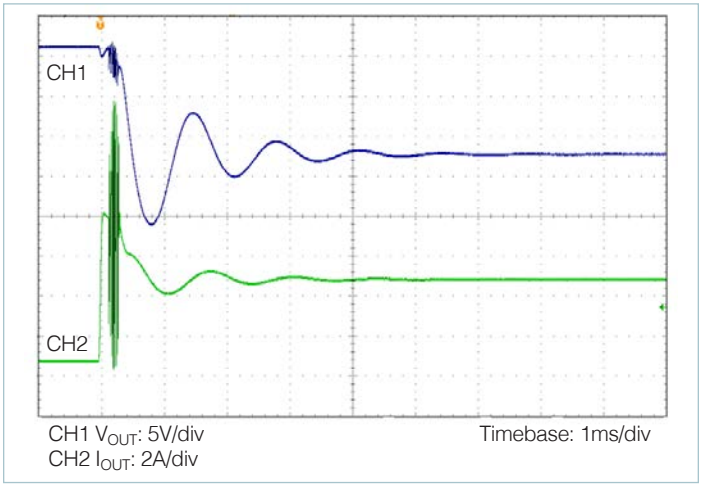


Figure 27 — *Example CV to CC transition with fast load slew rate*

Including some capacitance at either the load or on the factorized bus will reduce instances of fast current limit.

Layout Considerations

Application Note AN:005 provides detailed recommendations on layout for Factorized Power Architecture systems using PRMs and VTMs for minimizing losses and EMI. Particular attention should be paid to recommendations on routing control signals (OS, CD, VC etc.) to avoid noise pickup that could occur if these were routed directly beneath the PRM. It is critical that all control signals (except VC) are referenced to SGND, both for routing and for pull-down and bypassing purposes. VC provides control and feedback from the VTM during AL operation, and should instead be referenced to the PRM's –OUT.

The PRM –OUT pin is a distinct node from –IN, and the two must never be shorted together; all PRM output current must return to the –OUT terminal. SGND is connected to –IN inside the PRM, and it should not be tied to any other established ground in the system.

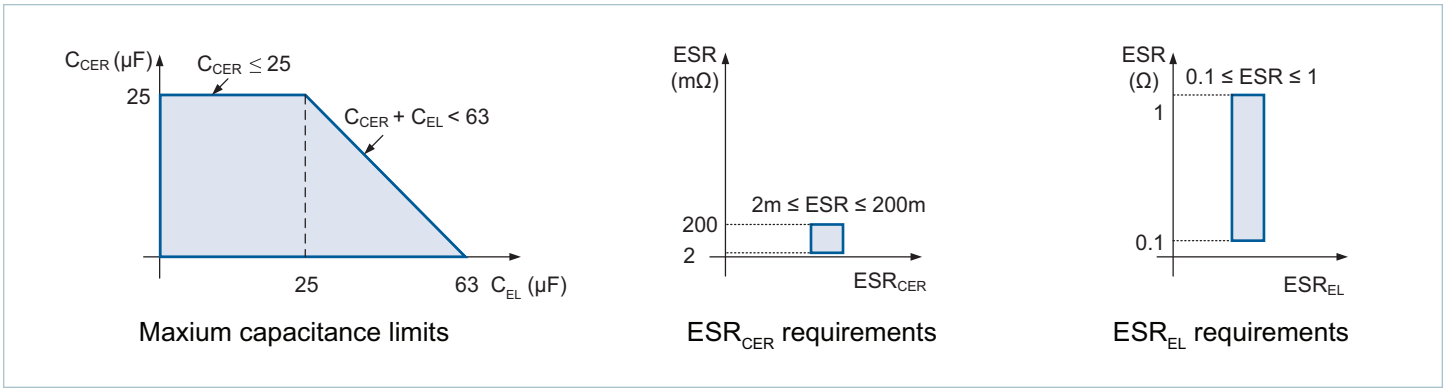


Figure 28 — *Output capacitance limits*

FPA System Considerations

There are a few system-level design considerations that should be carefully considered when using a PRM and VTM to implement a Factorized Power Architecture (FPA™) system.

The VC pin of the PRM should be directly connected to the VC pin of the VTM. The PRM and VTM coordinate the soft-start sequence of the FPA system through this connection. If the VC pins are not connected the VTM will not start up. When the PRM is ready to start up, it applies a voltage on VC, which enables and powers the VTM's powertrain. The PRM then proceeds to ramp up its output voltage. After approximately 10ms, VC returns to 0V and the VTM must then derive internal bias power from the factorized bus. Any VTM fault protection will latch the VTM powertrain off. In order to restart the system, input power to the system as a whole must be recycled or the PRM disabled and enabled with PC.

The PRM +OUT should have a damped inductor connected to it before any bypass capacitators on the factorized bus or the VTM input, in order to isolate switching ripple currents of the two modules. The inductor impedance should be much greater than the PRM internal output capacitance, $C_{OUT-INT}$, at the switching frequency of the PRM, F_{SW}. A resistor should be placed in parallel to this inductor to damp the resultant LC tank. In most cases 400nH is sufficient to isolate the switching ripple currents, with a 150mΩ damping resistor placed in parallel. Finally the low side of the factorized bus (the connection from the PRM –OUT pin to the VTM –IN pin) should have as low resistance as possible whenever adaptive-loop compensation is used in order to preserve optimal accuracy of the AL compensation.

Stability Considerations and Load Capacitance

The internal voltage-regulation loop has a fixed compensation network, designed to be stable over a wide range of operating and load conditions including load capacitance. External output capacitors influence the closed-loop frequency response, including capacitors on the output of any downstream VTM (if used) reflected to its input, as well as capacitors placed directly on the PRM output. In total these capacitors must lower than $C_{LOAD-ALEL}$, $C_{LOAD-CER}$, and C_{LOAD_TOTAL}, in order to maintain stability of the control loop and ensure reliable start up.

Figure 28 graphically illustrates the combined electrolytic and ceramic output capacitor limits for the PRM.

Thermal Design

Figure 29 shows a thermal impedance model that can predict the temperature of the hottest internal components for a given line operating condition at nominal trim. The circuit model identifies groups of heat flow paths through the package and pins, and assumes each group is isothermal. In order to exclude a group of thermal resistances from a given cooling solution, set the heat current through that group of paths to zero.

It is not recommended to use the MPRM28Ax360M120A00 without proper heat sinking.

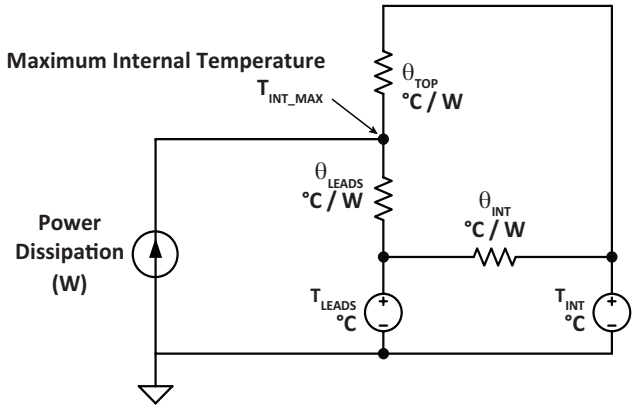


Figure 29 — *Thermal model*

Symbol	Thermal Impedance at Nominal Trim (°C / W)	Definition of Estimated Thermal Resistance
θ_{LEADS}	6.9	from the hottest component junction inside the PRM to the circuit board it is mounted on, at the leads
θ_{TOP}	2.6	from the hottest component junction inside the PRM to the case top
θ_{INT}	5.2	between the case top and the leads

Table 1 — *Thermal impedance*

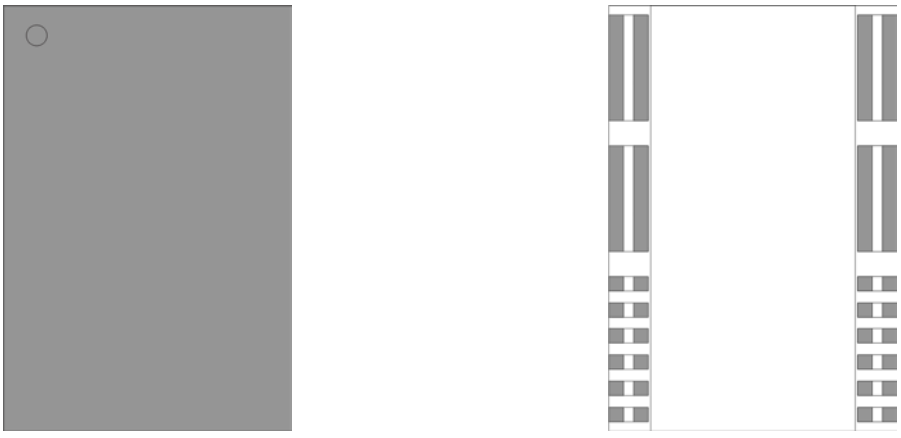
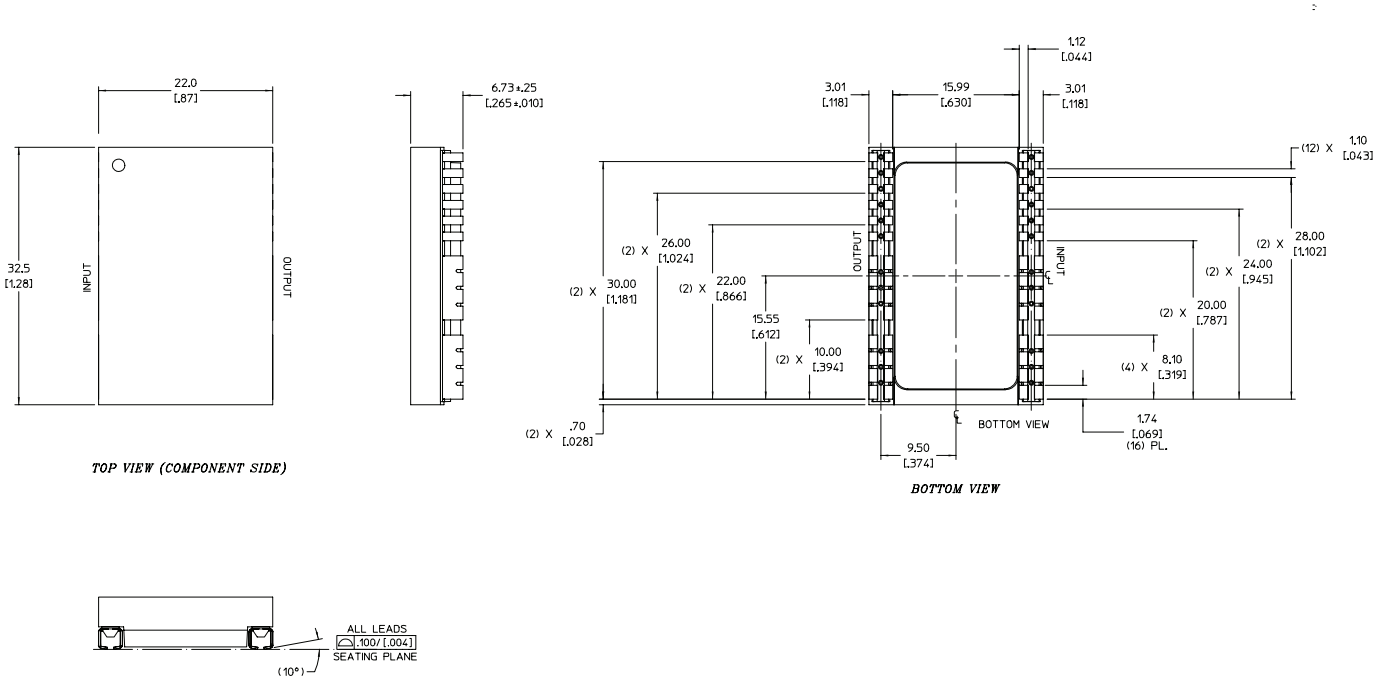
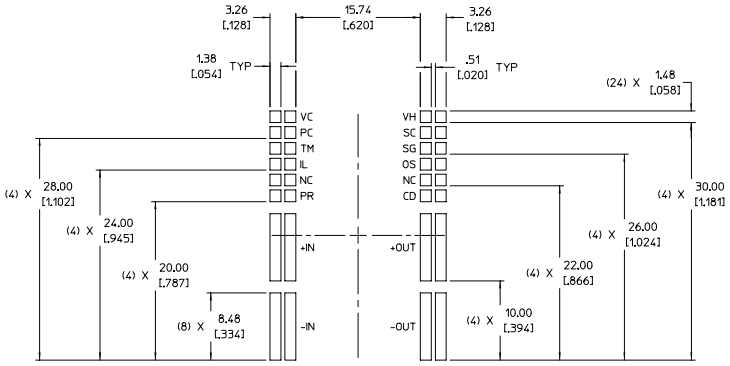


Figure 30 — *Thermal model boundary conditions; area defined as shaded*

Product Outline Drawing and Recommended Land Pattern - SMD (F)





RECOMMENDED LAND PATTERN

(COMPONENT SIDE SHOWN)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]

Revision History

Revision	Date	Description	Page Number(s)
1.0	06/04/20	Initial release	n/a

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