ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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Offices: 310-530-9400 / Fax: 310-530-9402
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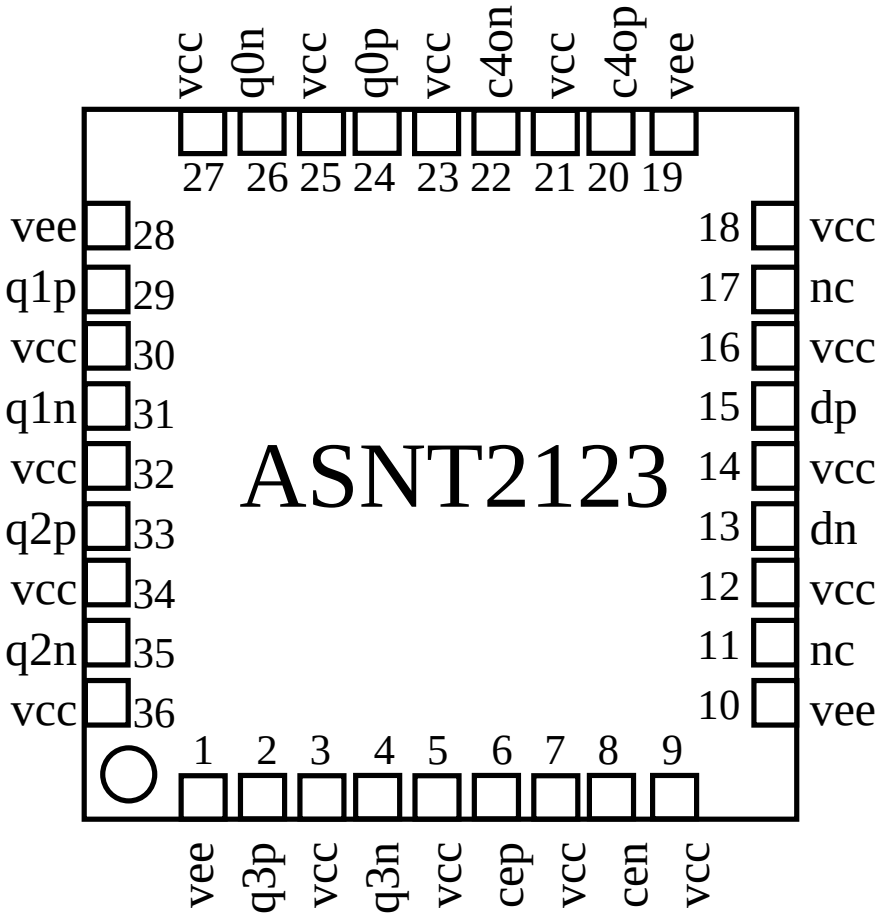
ASNT2123-PQP
DC-32*Gbps* Broadband Digital DDR 1:4 Demultiplexer

- High speed broadband 1:4 Demultiplexer (DMUX)
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Differential CML I/O data and clock buffers
- Half-rate clock input (DDR mode)
- Quarter-rate clock output
- Single +3.3*V* or -3.3*V* power supply
- Power consumption: 1.16*W*
- Fabricated in SiGe for high performance, yield, and reliability
- Standard QFN 36-pin package



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DESCRIPTION

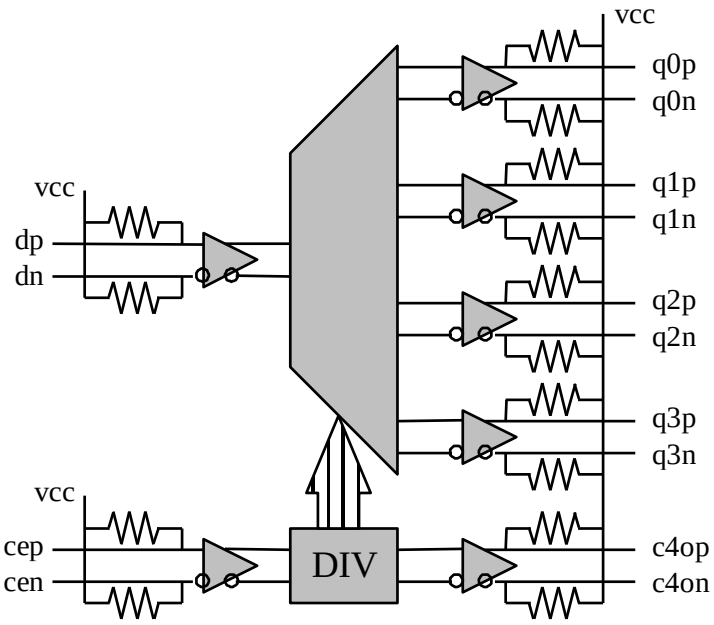

Fig. 1. Functional Block Diagram

ASNT2123-PQP is a low power and high-speed digital 1-to-4 deserializer-demultiplexer (DMUX) that functions seamlessly over data rates (f_{bit}) ranging from DC to its maximum speed.

The main function of the part shown in Fig. 1 is to demultiplex an incoming high speed serial differential CML data bit stream dp/dn running at a bit rate of f_{bit} into 4 parallel data channels q0p/q0n, q1p/q1n, q2p/q2n, q3p/q3n running at a bit rate of $f_{bit}/4$. Differential or single-ended half-rate clock cep/cen must be provided by an external source for the part to function properly.

The parallel words and clock divided-by-4 c4op/c4on are transmitted through CML output interfaces. The clock and data outputs are phase-matched to each other resulting in a very little relative skew over the operating temperature range of the device.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (vcc = 0.0*V* = ground and vee = −3.3*V*), or positive supply (vcc = +3.3*V* and vee = 0.0*V* = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

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All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.3	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+100	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
Low-Speed I/Os			
q0p	24	CML output	Differential quarter-rate data outputs. Require external SE 50*Ohm* termination to vcc
q0n	26		
q1p	29	CML output	
q1n	31		
q2p	33	CML output	
q2n	35		
q3p	2	CML output	
q3n	4		
c4op	20	CML output	Differential quarter-rate clock outputs. Require external SE 50*Ohm* termination to vcc
c4on	22		
High-Speed I/Os			
cep	6	CML input	Differential half-rate clock input signals with internal 50*Ohm* termination to vcc
cen	8		
dp	15	CML input	Differential full-rate data input signals with internal 50*Ohm* termination to vcc
dn	13		

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	3, 5, 7, 9, 12, 14, 16, 18, 21, 23, 25, 27, 30, 32, 34, 36
vee	Negative power supply (0*V* or -3.3*V*)	1, 10, 19, 28
nc	Not connected pins	11, 17

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		350		*mA*	
Power consumption		1160		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (dp/dn)					
Data Rate	DC	20	32	*Gb/s*	
Swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Half-Rate Input Clock (cep/cen)					
Frequency	DC	10	16	*GHz*	
Differential swing	0.2		0.8	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
Duty Cycle	40	50	60	*%*	
LS Output Data (q0p/q0n, q1p/q1n, q2p/q2n, q3p/q3n)					
Data Rate	DC	5	8	*Gb/s*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.44		*V*	With external 50*Ohm* DC termination
Output Jitter		2		*ps*	Peak-to-peak at 10*Gb/s*
LS Output Clock (c4op/c4on)					
Frequency	DC	5	8	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.4		*V*	With external 50*Ohm* DC termination
Duty Cycle		50		*%*	
Output Jitter		1		*ps*	Peak-to-peak at 10*GHz*

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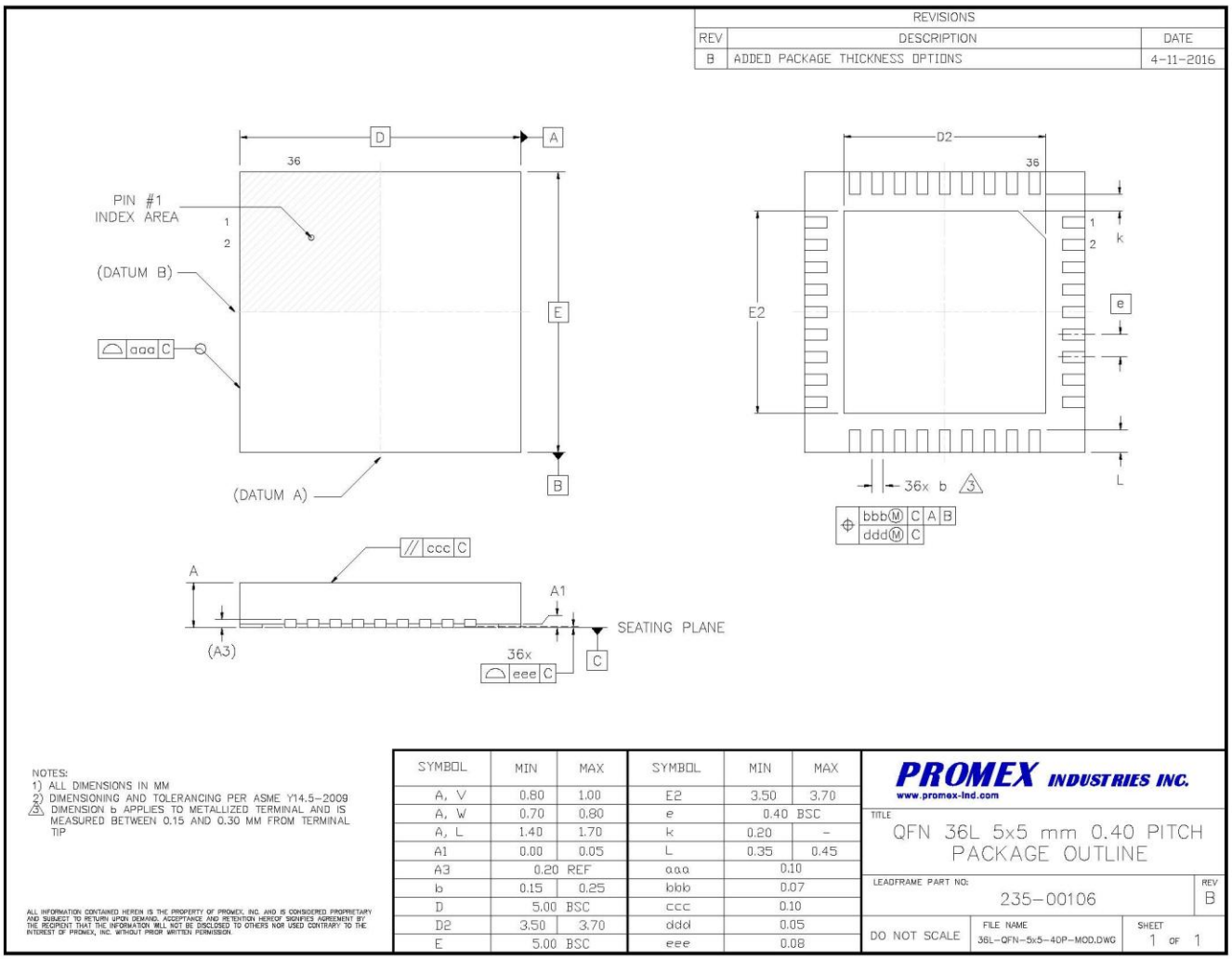
PACKAGE INFORMATION

The chip die is housed in standard 36-pin QFN package with a footprint shown in Fig. 2. It is recommended that the center heat slug located on the back side of the package is soldered to the vee plain that is ground for the positive supply or power for the negative supply.

The part's identification label is ASNT2123-PQP The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.



SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	3.50	3.70
A, W	0.70	0.80	e	0.40 BSC	
A, L	1.40	1.70	k	0.20	–
A1	0.00	0.05	L	0.35	0.45
A3	0.20 REF		aaa	0.10	
b	0.15	0.25	bbb	0.07	
D	5.00 BSC		ccc	0.10	
D2	3.50	3.70	ddd	0.05	
E	5.00 BSC		eee	0.08	

Fig. 2. QFN 36-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.1.2	01-2020	Updated Package Information
1.0.2	07-2019	Updated Letterhead
1.0.1	11-2017	Initial release
0.0.1	10-2017	Preliminary release