



# Low Capacitance, +12 V / +5 V / +3 V, Triple SPDT (Triple 2:1) Analog Switch / Multiplexer

## DESCRIPTION

The DG9454E is a high precision triple SPDT (triple 2:1) analog switch / multiplexer with enhanced performance on low power consumption. The part features low parasitic capacitance, low leakage, and low charge injection over the full signal range which make it an ideal switch for healthcare, data acquisition, and instrument products. Its compact size, light weight, low power consumption, and low voltage control capability are of advantages in portable consumer applications such as goggles.

The DG9454E is designed to operate from a 3 V to 16 V supply at V+, and 2.5 V to 5.5 V at VL, while guarantees 1.8 V logic compatible over the full operation voltage range.

Processed with advanced CMOS technology, the DG9454E conducts equally well in both directions, offers rail to rail analog signal handling and can be used both as a multiplexer as well as a de-multiplexer.

The DG9454E operating temperature is specified from -40 °C to +125 °C. It is available in ultra-compact 1.8 mm x 2.6 mm miniQFN16 package of lead (Pb)-free nickel-palladium-gold device termination. It is represented by the lead (Pb)-free “-E4” suffix. The nickel-palladium-gold device terminations meet all JEDEC® standards for reflow and MSL ratings.

## FEATURES

- Operates with V+ = 3 V to 16 V, VL = 2.5 V to 5.5 V
- Guaranteed 1.8 V logic control at full V+ range
- Low power consumption, both I+ and IL < 1 µA
- Low parasitic capacitance:
  - CD(ON): 8.8 pF
  - CD(OFF): 4 pF
  - CS(OFF): 3.1 pF
- High bandwidth: 356 MHz
- Low charge injection over the full signal range
- Compact miniQFN16 package (1.8 mm x 2.6 mm x 0.55 mm)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



RoHS COMPLIANT HALOGEN FREE

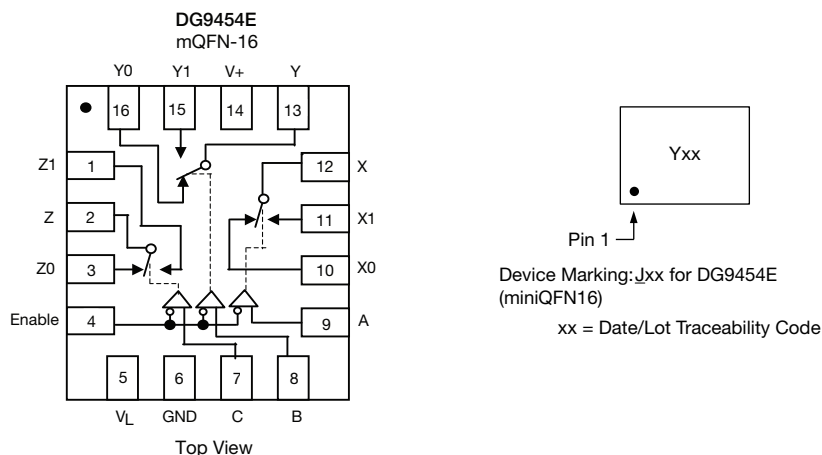
## APPLICATIONS

- Medical and healthcare systems
- Data acquisition systems
- Meters and instruments
- Games and Goggles
- Automatic test equipment
- Process control and automation
- Communication systems
- Battery powered systems

## BENEFITS

- Low power consumption
- Precision switching
- Low voltage logic interface
- Bi-directional rail to rail signal switching
- Compact package option
- Extended operation temperature range

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





TRUTH TABLE				
ENABLE INPUT	SELECT INPUTS			ON SWITCHES
	C	B	A	DG9454E
H	X	X	X	All Switches Open
L	L	L	L	X to X0, Y to Y0, Z to Z0
L	L	L	H	X to X1, Y to Y0, Z to Z0
L	L	H	L	X to X0, Y to Y1, Z to Z0
L	L	H	H	X to X1, Y to Y1, Z to Z0
L	H	L	L	X to X0, Y to Y0, Z to Z1
L	H	L	H	X to X1, Y to Y0, Z to Z1
L	H	H	L	X to X0, Y to Y1, Z to Z1
L	H	H	H	X to X1, Y to Y1, Z to Z1

ORDERING INFORMATION			
TEMP. RANGE	PACKAGE	PART NUMBER	MIN. ORDER / PACK. QUANTITY
-40 °C to +85 °C lead (Pb)-free	16-Pin miniQFN	DG9454EEN-T1-GE4	Tape and reel, 3000 units

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)		
PARAMETER	LIMIT	UNIT
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub> , V <sub>L</sub>	GND - 0.3 to (V <sub>+</sub> ) + 0.3 or 30 mA, whichever occurs first	V
V <sub>+</sub> to GND	-0.3 to +18	
Continuous Current (any terminal)	30	mA
Peak Current, S or D (pulsed 1 ms, 10 % duty cycle)	100	
Storage Temperature	-65 to +150	°C
Power Dissipation <sup>b</sup>	16-Pin miniQFN <sup>c, d</sup>	mW
Thermal Resistance <sup>b</sup>	16-Pin miniQFN <sup>d</sup>	°C/W
Latch-Up (per JEDEC78)	100	mA
ESD Human Body Model (HBM); per ANSI / ESDA / JEDEC JS-001	2500	V

**Notes**

- Signals on SX, DX, V<sub>L</sub> or INX exceeding V<sub>+</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC board.
- Derate 6.6 mW/°C above 70 °C.
- Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



SPECIFICATIONS FOR UNIPOLAR SUPPLIES											
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V <sub>+</sub> = 12 V, V <sub>L</sub> = 2.7 V V <sub>IN(A, B, C and enable)</sub> = 1.8 V, 0.5 V <sup>a</sup>	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	-40 °C to +125 °C		-40 °C to +85 °C		UNIT		
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	MIN. <sup>d</sup>	MAX. <sup>d</sup>			
<b>Analog Switch</b>											
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full	-	0	12	0	12	V		
On-Resistance	R <sub>ON</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 0.7 V, 6 V, 11.3 V	Room	85	-	103	-	103	Ω		
			Full	-	-	133	-	125			
On-Resistance Match	ΔR <sub>ON</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 0.7 V, 11.3 V	Room	1.24	-	8	-	8	Ω		
			Full	-	-	8	-	8			
On-Resistance Flatness	R <sub>FLATNESS</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 0.7 V, 6 V, 11.3 V	Room	27	-	37	-	37	Ω		
			Full	-	-	44	-	43			
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 13.2 V, V <sub>L</sub> = 2.7 V V <sub>D</sub> = 1 V / 12.2 V, V <sub>S</sub> = 12.2 V / 1 V	Room	± 0.05	-1	1	-1	1	nA		
			Full	-	-50	50	-5	5			
	I <sub>D(off)</sub>		Room	± 0.07	-1	1	-1	1			
			Full	-	-50	50	-5	5			
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>+</sub> = 13.2 V, V <sub>L</sub> = 2.7 V V <sub>D</sub> = V <sub>S</sub> = 1 V / 12.2 V	Room	± 0.07	-1	1	-1	1	nA		
			Full	-	-50	50	-5	5			
<b>Digital Control</b>											
Logic Low Input Voltage	V <sub>INL</sub>	V <sub>L</sub> = 2.7 V	Full	-	-	0.5	-	0.5	V		
Logic High Input Voltage	V <sub>INH</sub>		Full	-	1.8	-	1.8	-			
Logic Low Input Current	I <sub>L</sub>	V <sub>IN(A0, A1, A2 and enable)</sub> under test = 0.5 V	Full	0.02	-1	1	-1	1	μA		
Logic High Input current	I <sub>H</sub>	V <sub>IN(A0, A1, A2 and enable)</sub> under test = 1.8 V	Full	0.02	-1	1	-1	1			
<b>Dynamic Characteristics</b>											
Transition Time	t <sub>TRANS</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF see Fig. 1, 2, 3	Room	79	-	119	-	119	ns		
			Full	-	-	134	-	126			
Enable Turn-On Time	t <sub>ON(EN)</sub>		Room	70	-	110	-	110			
			Full	-	-	130	-	116			
Enable Turn-Off Time	t <sub>OFF(EN)</sub>		Room	51	-	91	-	91			
			Full	-	-	95	-	94			
Break-Before-Make Time Delay	t <sub>D</sub>		Room	17	-	-	-	-			
			Full	-	1	-	1	-			
Charge Injection <sup>e</sup>	Q		C <sub>L</sub> = 1 nF, R <sub>GEN</sub> = 0 Ω, V <sub>GEN</sub> = 0 V	Full	5.84	-	-	-		-	pC
Off Isolation <sup>e</sup>	OIRR		f = 1 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF	100 kHz	Room	-95	-	-		-	-
		1 MHz		Room	-85	-	-	-	-		
		10 MHz		Room	-65	-	-	-	-		
Crosstalk <sup>e</sup>	X <sub>TALK</sub>	100 kHz		Room	-92	-	-	-	-		
		1 MHz		Room	-73	-	-	-	-		
		10 MHz		Room	-53	-	-	-	-		
Bandwidth, -3 dB <sup>e</sup>	BW	R <sub>L</sub> = 50 Ω		Room	356	-	-	-	-	MHz	
Source Off Capacitance <sup>e</sup>	C <sub>S(off)</sub>	f = 1 MHz		Room	3.1	-	-	-	-	pF	
Drain Off Capacitance <sup>e</sup>	C <sub>D(off)</sub>			Room	4	-	-	-	-		
Channel On Capacitance <sup>e</sup>	C <sub>D(on)</sub>			Room	8.8	-	-	-	-		
Total Harmonic Distortion <sup>e</sup>	THD	Signal = 1 V <sub>RMS</sub> , 20 Hz to 20 kHz, R <sub>L</sub> = 600 Ω	Room	0.075	-	-	-	-	%		



SPECIFICATIONS FOR UNIPOLAR SUPPLIES									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V <sub>+</sub> = 12 V, V <sub>L</sub> = 2.7 V V <sub>IN(A, B, C and enable)</sub> = 1.8 V, 0.5 V <sup>a</sup>	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	MIN. <sup>d</sup>	MAX. <sup>d</sup>	
<b>Power Supply</b>									
Power Supply Range	I <sub>+</sub>	V <sub>IN(A, B, C and enable)</sub> = 0 V or 12 V	Room	0.05	-	1	-	1	μA
			Full	-	-	10	-	10	
Ground Current	I <sub>GND</sub>	V <sub>L</sub> = 2.7 V	Room	0.05	-1	-	-1	-	
			Full	-	-10	-	-10	-	
Logic Supply Current	I <sub>L</sub>		Room	0.05	-	1	-	1	
			Full	-	-	10	-	10	

**Notes**

- a. V<sub>IN</sub> = input voltage to perform proper function.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.



SPECIFICATIONS FOR UNIPOLAR SUPPLIES											
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V <sub>+</sub> = 5 V, V <sub>L</sub> = 2.7 V V <sub>IN(A, B, C and enable)</sub> = 1.8 V, 0.5 V <sup>a</sup>	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	-40 °C to +125 °C		-40 °C to +85 °C		UNIT		
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	MIN. <sup>d</sup>	MAX. <sup>d</sup>			
<b>Analog Switch</b>											
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full	-	0	5	0	5	V		
On-Resistance	R <sub>ON</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 0 V, 3.5 V	Room	125	-	147	-	147	Ω		
			Full	-	-	176	-	168			
On-Resistance Match	ΔR <sub>ON</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 3.5 V	Room	1.33	-	8	-	8	Ω		
			Full	-	-	8	-	8			
On-Resistance Flatness	R <sub>FLATNESS</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 0 V, 3 V	Room	21	-	31	-	31	Ω		
			Full	-	-	25	-	29			
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = 0 V V <sub>D</sub> = 1 V / 4.5 V, V <sub>S</sub> = 4.5 V / 1 V	Room	± 0.03	-1	1	-1	1	nA		
			Full	-	-50	50	-5	5			
	Room		± 0.03	-1	1	-1	1				
	Full		-	-50	50	-5	5				
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = 0 V V <sub>D</sub> = V <sub>S</sub> = 1 V / 4.5 V	Room	± 0.03	-1	1	-1	1	nA		
			Full	-	-50	50	-5	5			
<b>Digital Control</b>											
V <sub>IN(A, B, C and enable)</sub> LOW	V <sub>IL</sub>	V <sub>L</sub> = 2.7 V	Full	-	-	0.6	-	0.6	V		
V <sub>IN(A, B, C and enable)</sub> High	V <sub>IH</sub>	V <sub>L</sub> = 2.7 V	Full	-	1.8	-	1.8	-	V		
Input Current, V <sub>IN</sub> Low	I <sub>L</sub>	V <sub>IN(A, B, C and enable)</sub> under test = 0.6 V	Full	0.02	-1	1	-1	1	μA		
Input Current, V <sub>IN</sub> High	I <sub>H</sub>	V <sub>IN(A, B, C and enable)</sub> under test = 1.8 V	Full	0.02	-1	1	-1	1	μA		
<b>Dynamic Characteristics</b>											
Transition Time	t <sub>TRANS</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF see Fig. 1, 2, 3	Room	95	-	135	-	135	ns		
			Full	-	-	164	-	152			
Enable Turn-On Time	t <sub>ON</sub>		Room	80	-	120	-	120			
			Full	-	-	138	-	129			
Enable Turn-Off Time	t <sub>OFF</sub>		Room	58	-	98	-	98			
			Full	-	-	106	-	103			
Break-Before-Make Time Delay	t <sub>D</sub>		Room	45	-	-	-	-			
			Full	-	24	-	15	-			
Charge Injection <sup>e</sup>	Q		V <sub>g</sub> = 0 V, R <sub>g</sub> = 0 Ω, C <sub>L</sub> = 1 nF	Full	1.44	-	-	-		-	pC
Off Isolation <sup>e</sup>	OIRR		R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF f = 100 kHz	Room	-95	-	-	-		-	dB
Channel-to-Channel Crosstalk <sup>e</sup>	X <sub>TALK</sub>	Room		-92	-	-	-	-			
Source Off Capacitance <sup>e</sup>	C <sub>S(off)</sub>	f = 1 MHz	Room	3.5	-	-	-	-	pF		
Drain Off Capacitance <sup>e</sup>	C <sub>D(off)</sub>		Room	4.5	-	-	-	-			
Channel On Capacitance <sup>e</sup>	C <sub>D(on)</sub>		Room	10.2	-	-	-	-			
<b>Power Supply</b>											
Power Supply Current	I <sub>+</sub>	V <sub>IN(A, B, C and enable)</sub> = 0 V or 5 V	Room	0.05	-	1	-	1	μA		
			Full	-	-	10	-	10			
Ground Current	I <sub>GND</sub>		Room	-0.05	-1	-	-1	-			
			Full	-	-10	-	-10	-			
Logic Supply Current	I <sub>L</sub>		Room	0.05	-	1	-	1			
			Full	-	-	10	-	10			

**Notes**

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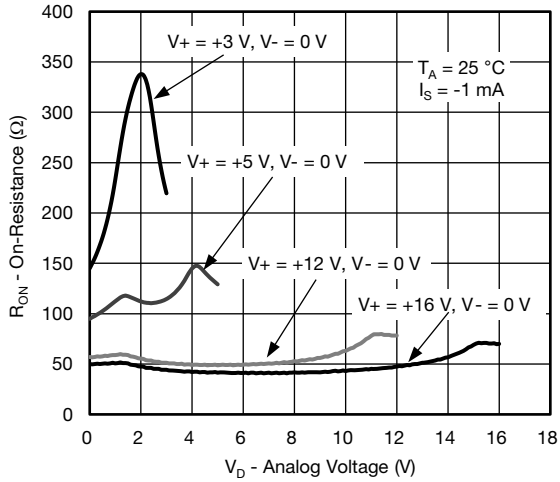
SPECIFICATIONS FOR UNIPOLAR SUPPLIES									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V <sub>+</sub> = 3 V, V <sub>L</sub> = 2.7 V V <sub>IN(A, B, C AND ENABLE)</sub> = 1.5 V, 0.6 V <sup>a</sup>	TEMP. <sup>b</sup>	TYP. <sup>c</sup>	-40 °C to +125 °C		-40 °C to +85 °C		UNIT
					MIN. <sup>d</sup>	MAX. <sup>d</sup>	MIN. <sup>d</sup>	MAX. <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full	-	0	3	0	3	V
On-Resistance	R <sub>ON</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 1.5 V	Room	221	-	-	-	-	Ω
			Full	-	-	-	-		
Switch Off Leakage Current	I <sub>S(off)</sub>	V <sub>+</sub> = 3.3 V, V <sub>L</sub> = 2.7 V V <sub>D</sub> = 0.3 V / 3 V, V <sub>S</sub> = 3 V / 0.3 V	Room	± 0.02	-1	1	-1	1	nA
			Full	-	-50	50	-5	5	
	I <sub>D(off)</sub>		Room	± 0.02	-1	1	-1	1	
			Full	-	-50	50	-5	5	
Channel On Leakage Current	I <sub>D(on)</sub>	V <sub>+</sub> = 3.3 V, V <sub>L</sub> = 2.7 V V <sub>S</sub> = V <sub>D</sub> = 0.3 V / 3 V	Room	± 0.02	-1	1	-1	1	
			Full	-	-50	50	-5	5	
<b>Digital Control</b>									
Logic Low Input Voltage	V <sub>INL</sub>	V <sub>L</sub> = 2.7 V	Full	-	-	0.6	-	0.6	V
Logic High Input Voltage	V <sub>INH</sub>		Full	-	1.8	-	1.8	-	
Logic Low Input Current	I <sub>L</sub>	V <sub>IN(A0, A1, A2 and enable)</sub> under test = 0.6 V	Full	0.02	-1	1	-1	1	μA
Logic High Input Current	I <sub>H</sub>	V <sub>IN(A0, A1, A2 and enable)</sub> under test = 1.8 V	Full	0.02	-1	1	-1	1	
<b>Dynamic Characteristics</b>									
Transition Time	t <sub>TRANS</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF see Fig. 1, 2, 3	Room	161	-	-	-	-	ns
			Full	-	-	-	-	-	
Enable Turn-On Time	t <sub>ON(EN)</sub>		Room	120	-	-	-	-	
			Full	-	-	-	-	-	
Enable Turn-Off Time	t <sub>OFF(EN)</sub>		Room	79	-	-	-	-	
			Full	-	-	-	-	-	
Break-Before-Make Time Delay	t <sub>D</sub>		Room	98	-	-	-	-	
			Full	-	-	-	-	-	
Charge Injection <sup>e</sup>	Q		C <sub>L</sub> = 1 nF, R <sub>GEN</sub> = 0 Ω, V <sub>GEN</sub> = 0 V	Full	0.58	-	-	-	pC
Off Isolation <sup>e</sup>	OIRR		f = 1 MHz, R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF	Room	-95	-	-	-	dB
Crosstalk <sup>e</sup>	X <sub>TALK</sub>	Room		-92	-	-	-		
Source Off Capacitance <sup>e</sup>	C <sub>S(off)</sub>	f = 1 MHz	Room	3.7	-	-	-	pF	
Drain Off Capacitance <sup>e</sup>	C <sub>D(off)</sub>		Room	4.7	-	-	-		
Channel On Capacitance <sup>e</sup>	C <sub>D(on)</sub>		Room	10.4	-	-	-		
<b>Power Supply</b>									
Power Supply Range	I <sub>+</sub>	V <sub>IN (A, B, C and enable)</sub> = 0 V or 3 V	Room	0.05	-	1	-	1	μA
			Full	-	-	10	-	10	
Ground Current	I <sub>GND</sub>		Room	0.05	-1	-	-1	-	
			Full	-	-10	-	-10	-	
Logic Supply Current	I <sub>L</sub>		Room	0.05	-	1	-	1	
			Full	-	-	10	-	10	

**Notes**

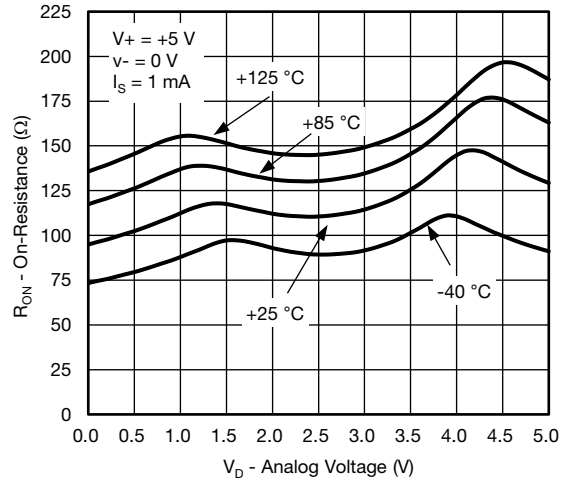
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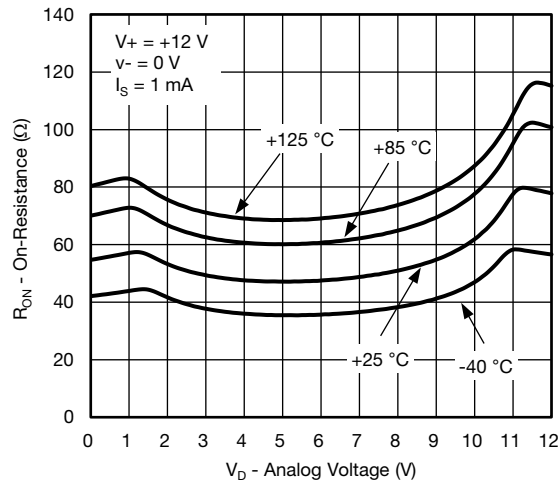
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



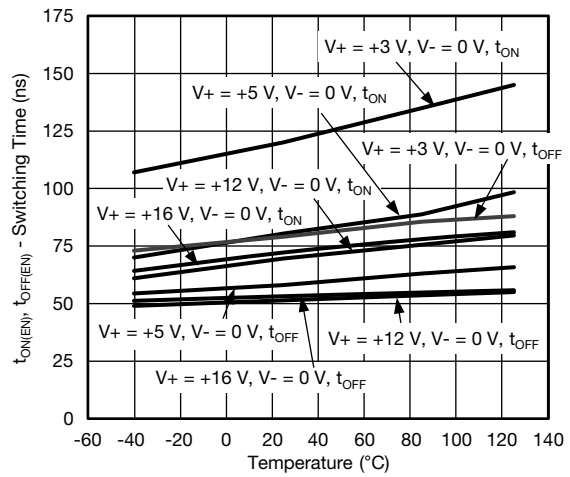
On-Resistance vs. V<sub>D</sub> and Signal Supply Voltage



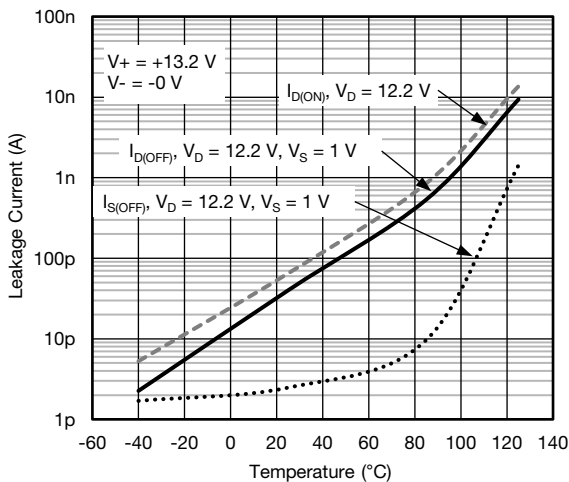
On-Resistance vs. Analog Voltage and Temperature



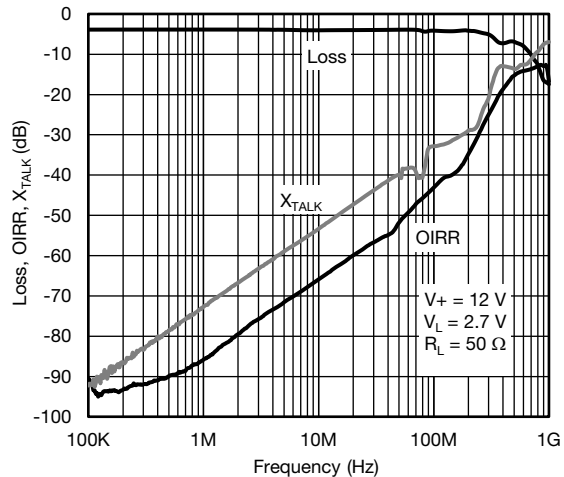
On-Resistance vs. Analog Voltage and Temperature



Switching Time vs. Temperature

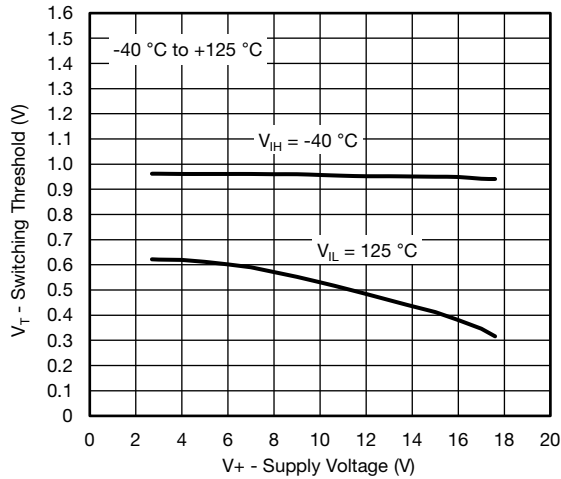


Leakage Current vs. Temperature

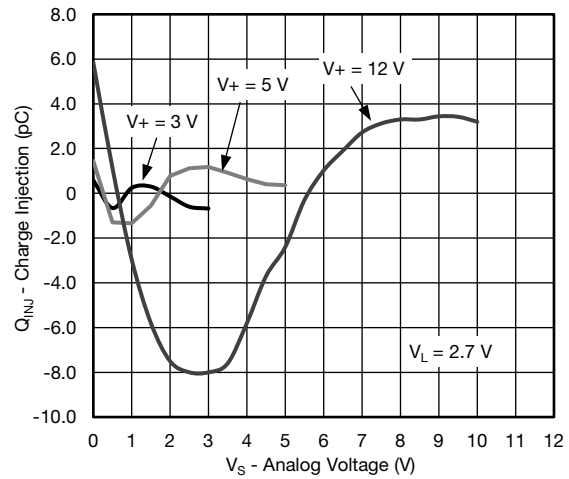


Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

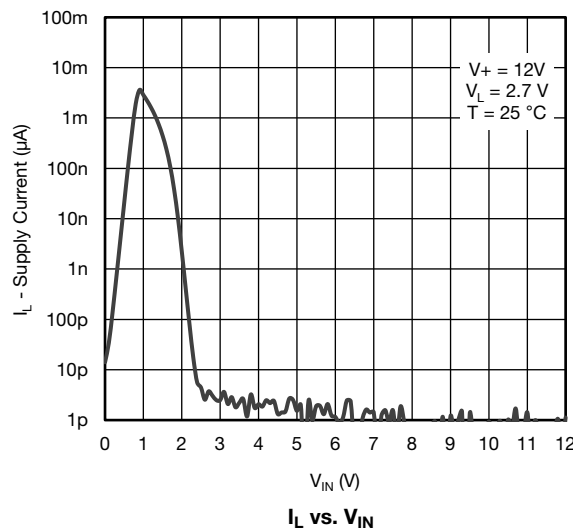
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



Switching Threshold vs. Logic Supply Voltage

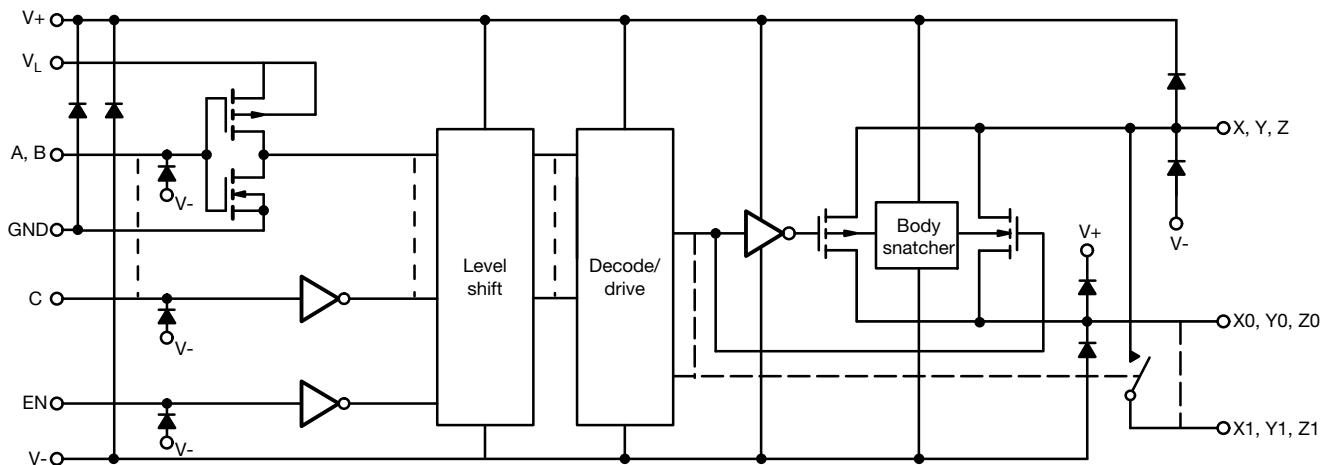


Charge Injection vs. Analog Voltage



I<sub>L</sub> vs. V<sub>IN</sub>

**SCHEMATIC DIAGRAM** (typical channel)





TEST CIRCUITS

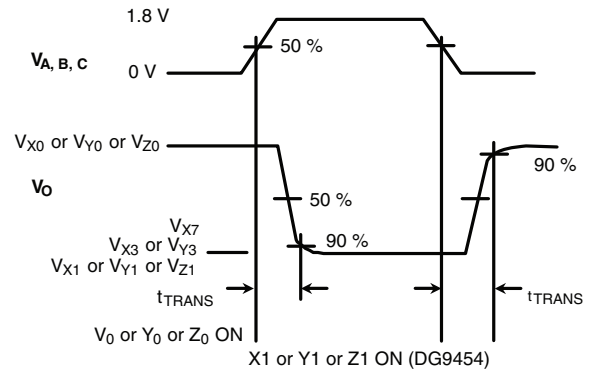
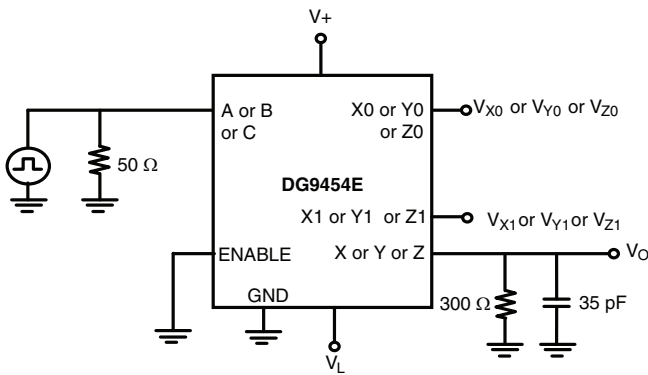


Fig. 1 - Transition Time

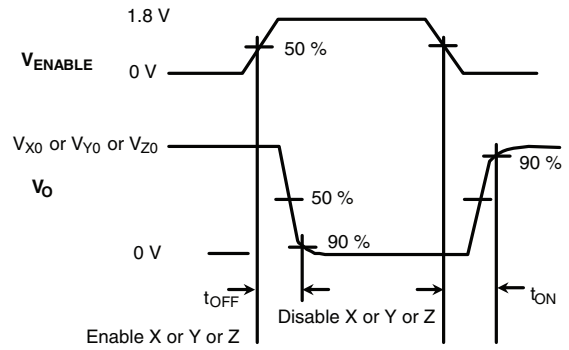
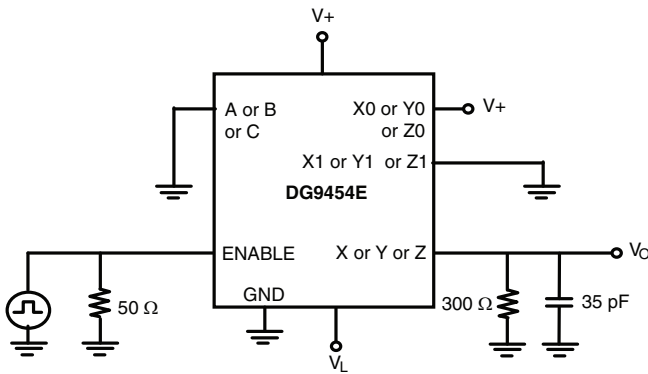


Fig. 2 - Enable Switching Time

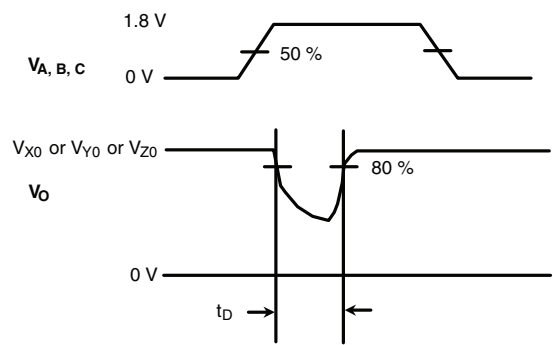
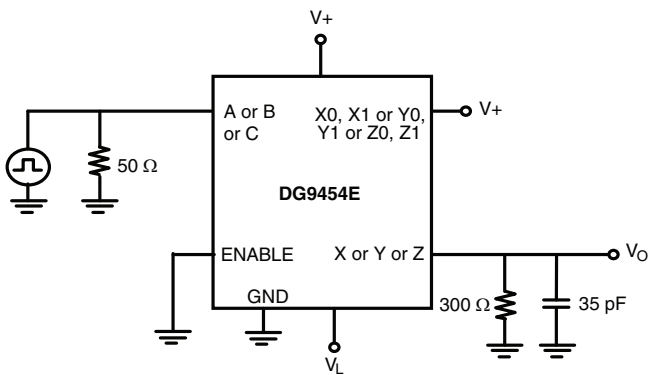


Fig. 3 - Break-Before-Make

TEST CIRCUITS

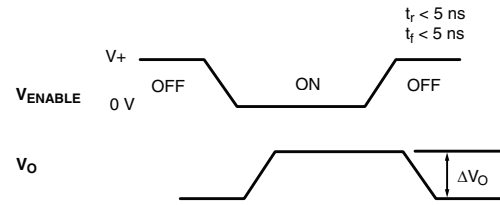
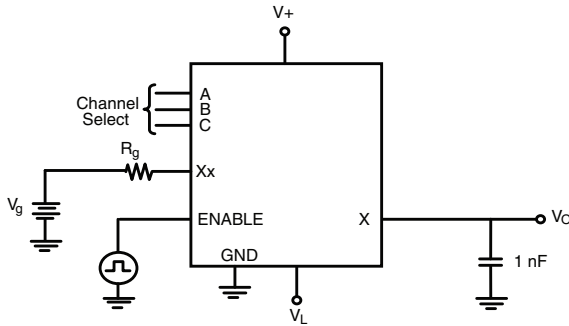
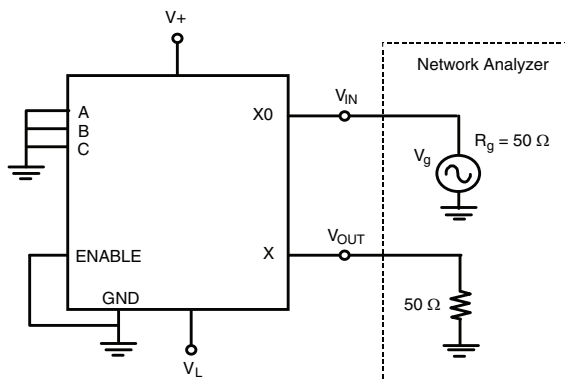
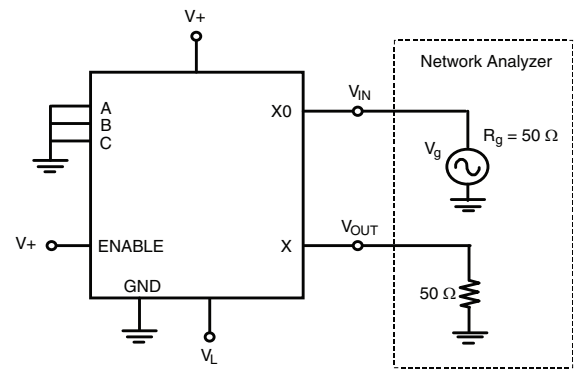


Fig. 4 - Charge Injection



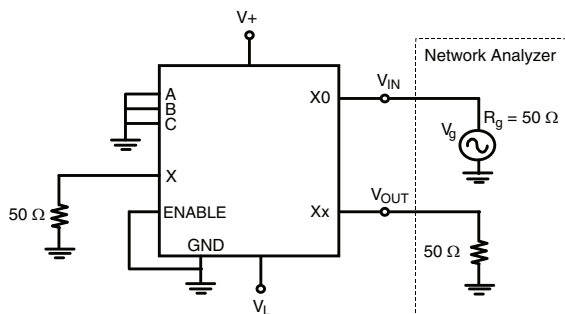
$$\text{Insertion Loss} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Fig. 5 - Insertion Loss



$$\text{Off Isolation} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Fig. 7 - Off Isolation



$$\text{Crosstalk} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Fig. 6 - Crosstalk

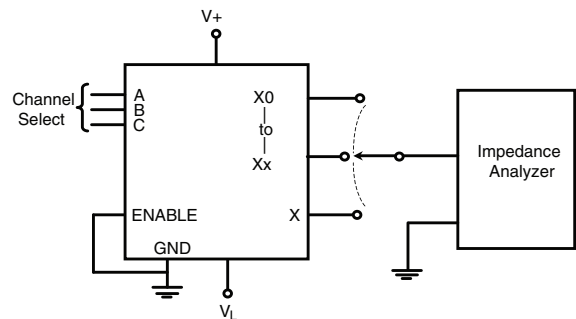
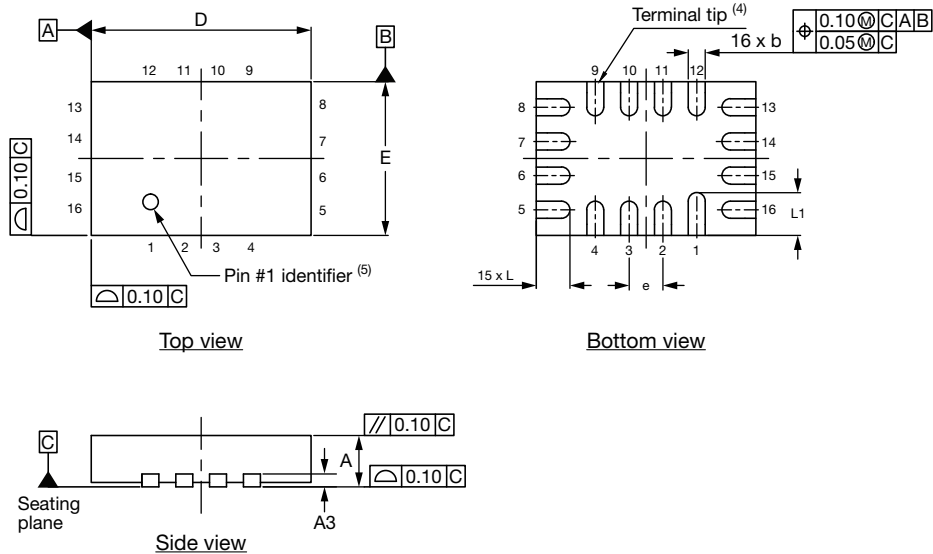


Fig. 8 - Source, Drain Capacitance

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## Thin miniQFN16 Case Outline



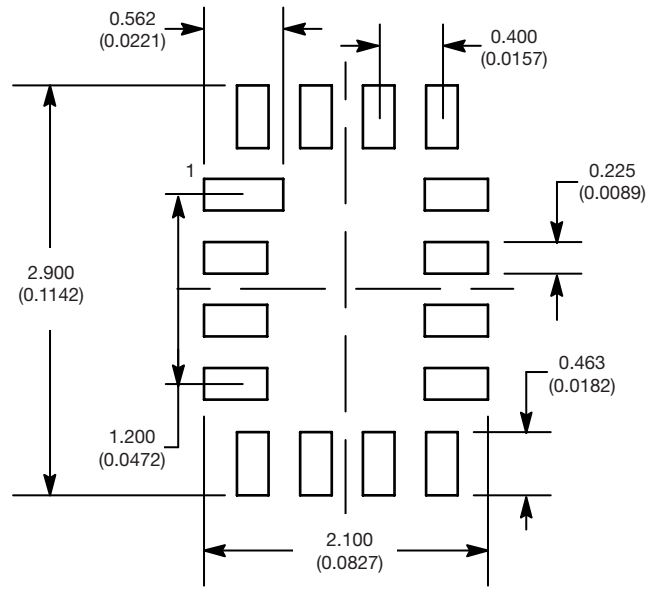
DIMENSIONS	MILLIMETERS <sup>(1)</sup>			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N <sup>(3)</sup>	16			16		
Nd <sup>(3)</sup>	4			4		
Ne <sup>(3)</sup>	4			4		

**Notes**

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

ECN: T16-0226-Rev. B, 09-May-16  
DWG: 6023

**RECOMMENDED MINIMUM PADS FOR MINI QFN 16L**



Mounting Footprint  
Dimensions in mm (inch)



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