AN_8014BN_062 January 2010

Replacing the 73S8024RN with the 73S8014BN

1 Introduction

This document describes how to replace the Teridian 73S8024RN smart card interface IC with the Teridian 73S8014BN. The 73S8014BN is a cost-optimized derivative of the 73S8024RN smart card interface device. This is achieved by removing non-essential functions of the 73S8024RN. These differences are discussed and various precautions are examined to insure the proper transition to the 73S8014BN. In addition, a dual footprint implementation is described using the 73S8024RN and 73S8014BN.

This document is intended for both the hardware and software application developer that currently uses the Teridian 73S8024RN smart card interface device. Knowledge of the ISO-7816 is required.

2 Feature Modifications and Removals

Several features available in the 73S8024RN have been removed or redefined to achieve the lowest cost interface device possible while adding support for 1.8 V smart card operation, card switch debounce and power down. The reason for removal of some of these features is to enable the use of a package that has the smallest possible pin count and therefore the lowest possible cost. This combination of redefinition and removal of these features allows the removal of 8 pins. The 28-pin 73S8024RN can now be replaced by the 20-pin 73S8014BN. If the auxiliary data signals C4 and C8 are not used, then the 14-pin version of the 73S8014BN can be used. This is the 73S8014BL.

2.1 Removal of the Activation Sequencer

The 73S8024RN has an activation sequencer to insure that the activation sequence is both ISO-7816 and NDS compatible. NDS has a requirement that states that a minimum of 40000 clock cycles are required before RST can be deasserted during the card activation. The 73S8024RN holds the RST output active for 42000 clock cycles so that the status of the RSTIN pin is ignored and held active during this time. After 42000 cycles, the RST output will track the RSTIN input. The 73S8014BN removes this delay circuitry so control of the RSTIN input timing now must be handled by the host interface. The possible software impacts will be detailed later in the software migration section.

2.2 Removal of the Adjustable VDD Fault

The 73S8024RN has a pin named VDDF_ADJ. This pin allows the threshold for the VDD fault circuit to be adjusted to a desired voltage. In order to reduce the number of pins, this feature has been removed in the 73S8014BN. The fault circuit is still implemented, but the adjustability has been removed. The VDD default threshold is set internally at 2.3 V.

2.3 Redefinition of the Clock Divider

The 73S8024RN uses two input pins, CLKDIV1 and CLKDIV2, to select among the four clock divider rates of divide by 1, 2, 4 and 8. Table 1 shows the clock divider rates for the CLKIN1 and CLKIN2 input pins.

Table 1: 73S8024RN CLKDIV1 and CLKDIV2 Configuration

CLKDIV1	CLKDIV2	CLK
0	0	⅛ XTALIN
0	1	¼ XTALIN
1	0	XTALIN
1	1	½ XTALIN

In order to remove one input pin from the two input clock divider selector on the 73S8024RN, the clock divider circuit on the 73S8014BN has been modified to allow a single pin to be used to select the four clock divider rates. This is accomplished by creating a single input with multiple voltage level thresholds to select the four divisor rates. The voltage levels used to select the desired divider ratio in the 73S8014BN is shown in Table 1.

Table 1: 73S8014BN CLKDIV Configuration

CLKDIV Voltage	CLK Frequency	Max XTALIN/CLKIN
Ground	¼ XTALIN	27MHz
V_{DD} / 3	XTALIN	20MHz
V_{DD} * 2 / 3	⅛ XTALIN	27MHz
V_{DD}	½ XTALIN	27MHz

Usage of an external resistor divider network can allow for conversion of some of the clock divider rates between the 73S8024RN and 73S8014BN, however direct full conversion to support all four divisor rates is not possible without some external logic circuits. Table 2 shows the clock divider selection for both the 73S8024RN and the 73S8014BN. The reason the direct full conversion is not possible without external logic is due to the fact that a resistor divider can't create a voltage of VDD * 2/3 from a logic 0 on both CLKDIV1 and CLKDIV2 for the divide by 8 selection.

Table 2: 73S8024RN and 73S8014BN Clock Divider Configuration Comparison

	73S8024RN		73S8014BN
CLK	CLKDIV1	CLKDIV2	
⅛ XTALIN	0	0	V_{DD} * 2 / 3
¼ XTALIN	0	1	Ground
XTALIN	1	0	V_{DD} / 3
½ XTALIN	1	1	V_{DD}

This was a deliberate decision made by Teridian as it was determined that a majority of users do not use all the divisor rates in a given application. In most cases, it has been found that the divisor rates of divide by 2 and divide by 4 are most commonly used. As a result, it was decided to use these rates as the 0 V and VDD logic levels to reduce the possibility of requiring the use on an external resistor divider to convert the divider rate selection when using the 73S8014BN. The divide by 1 and divide by 8 ratios will require the use of an external resistor network to select these rates.

For example, those applications where only divisor rates of divide by 2 and 4 are used, the CLKDIV1 pin used on the 73S8024RN can be used to connect directly to the CLKDIV pin of the 73S8014BN and maintain the same ratios.

2.4 Removal of CLKSTOP, CLKLVL and $\overline{\text{PRES}}$ Pins

The pins CLKSTOP and CLKLVL were found to be used very rarely on the 73S8024RN and these functions were removed from the 73S8014BN. The $\overline{\text{PRES}}$ pin was removed as it is very simple to configure the external card detect for logic high (card inserted) by changing the external resistor configuration.

3 Feature Enhancements

The 73S8014BN includes some feature enhancements not found on the 73S8024RN.

3.1 Addition of 1.8 V Support

The 73S8014BN adds support for 1.8 V smart cards while maintaining compatibility with the 73S8024RN control logic. The 73S8024RN supports 3 V and 5 V smart cards using a combination of the $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ control inputs. The 73S8014BN maintains the use and logic of these signals with the 73S8024RN, but adds support for 1.8 V control by taking both $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ low at the same time (within 400 ns of each other). The precautions involved around transitioning the software control from the 73S8024RN to the 73S8014BN will be discussed in the firmware precautions section.

3.2 PRES Input Debounce

The 73S8024RN has no debounce on the PRES/$\overline{\text{PRES}}$ inputs. As a result, it is possible to see bounce on the $\overline{\text{OFF}}$ output when a card is inserted or removed. The 73S8014BN has added a debounce circuit. The operation of the debounce is different depending on whether the card is inserted or removed. The reason for the difference on the card event is due to action required upon a card removal when the card was activated before removal. A debounce period is not desired in this case as the emergency deactivation must be handled immediately to insure that no data corruption on the card is allowed to occur while the card is being removed. The $\overline{\text{OFF}}$ output will immediately go low on the falling edge of PRES and stay low until the PRES input is solidly high for 5 ms. In the case for a card insertion, the debounce period is approximately 5 ms meaning that the PRES input is solidly high for this amount of time. After 5 ms of having PRES solidly high has elapsed, the $\overline{\text{OFF}}$ output will go high.

3.3 Power Down

The 73S8024RN has no low power operation mode available. The analog circuitry and oscillators are always powered and running therefore drawing power whether the card is activated or not. The 73S8014BN adds low power capability without the addition of a separate power down pin. The power down mode is only available outside a card session and is initiated by setting the RSTIN pin high when both $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ are high. Power down is not immediately entered upon this condition, but if it is held for 2 ms, then the 73S8014BN will enter the power down mode. The power down mode will draw about 1 µA on VPC and VDD.

To exit from power down, the RSTIN input must be taken low. The $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ have no effect when exiting from power down. When RSTIN is taken low, the $\overline{\text{OFF}}$ output will immediately go low for about 5 to 7 ms to indicate to the host that the 73S8014BN is exiting from power down. This is necessary to allow all the circuits and oscillators to restart and stabilize. After this time has elapsed, the $\overline{\text{OFF}}$ output will reflect the card status. If the card is inserted, then activation can begin.

The card detection logic is available when the 73S8014BN is in power down mode. The debounce circuit will operate the same whether in or out of power down.

4 Firmware Precautions

When transitioning from the 73S8024RN to the 73S8014BN, the control signal timing is nearly identical between the two devices, however the feature differences between the parts forces some of the control signals and timing to change. The following sections detail these differences and indicate where they may cause operational difficulties.

4.1 Holding RSTIN high outside a Card Session

When using the 73S8024RN, the RSTIN input is a don't care when a card is deactivated or removed. This is not true for the 73S8014BN. The 73S8014BN uses RSTIN to control the power down mode under these conditions. If the RSTIN is set high while $\overline{\text{CMDVCC}}$ and 5V/$\overline{\text{3V}}$ are high and held for at least 2 ms, then the 73S8014BN will enter power down mode. The 73S8014BN will not be able to activate an inserted card when $\overline{\text{CMDVCC}}$ is set low if in power down mode. The RSTIN input must be taken low prior to activating a card to exit the power down mode and then wait until the device is ready before attempting to activate the card. See the 73S8014BN datasheet for details on how to exit power down and determine when the 73S8014BN is ready to activate a card.

4.2 Activation with CLK Delay

Like the 73S8024RN, the 73S8014BN can delay the start of the CLK output if the RSTIN is high at $\overline{\text{CMDVCC}}$ going low or at time t1 as described in the *73S8014BN Data Sheet*. Time t1 indicates a stable and valid VCC output as part of the activation sequence. If this CLK delay is used and the RSTIN input is high before the $\overline{\text{CMDVCC}}$ is taken low, then the time between RSTIN being set high and the time between $\overline{\text{CMDVCC}}$ being set low must not exceed 2 ms or the power down mode can be initiated if the 5V/$\overline{\text{3V}}$ input is set for 5 V operation (set high). If this time period is longer than 2 ms, then the 73S8014BN will go into power down and any falling edge of $\overline{\text{CMDVCC}}$ will be ignored.

4.3 RST Sequencer Delay Removal

As mentioned above, the 73S8024RN has a 42000 CLK cycle delay before the RST output follows the RSTIN input. This means that the RSTIN input will be ignored and RST is held low from the time the CLK output starts upon activation until 42000 CLK cycles have elapsed. The 73S8014BN does not implement this delay and forces the host interface to manage any required minimum delay between the CLK output start and the deassertion of RST. As a result, the ATR mute error timeout configured for the 73S8024RN may have to be changed when using the 73S8014BN. However, in most cases, the host software used for the 73S8024RN will hold the falling edge of RSTIN at least 42000 clock cycles to insure that the edge of RST is controlled by the RSTIN input and not by the sequencer. With the correlation of these edges, the ATR timeouts are insured of being in sync with the host. As a result, this shouldn't have any impact on the 73S8014BN as the host should hold RSTIN low until the sequencer delay expires and maintain the same timing.

4.4 3 V VCC Activation

When the 73S8024RN is being configured for 3 V operation, the 5V/$\overline{\text{3V}}$ should be low upon the falling edge of $\overline{\text{CMDVCC}}$ to generate 3 V on VCC. When activating the 73S8024RN, the host software should have some setup time between the 5V/$\overline{\text{3V}}$ being set low and the falling edge of $\overline{\text{CMDVCC}}$ to start activation. However, the 73S8024RN can actually power VCC at 3 V if the 5V/$\overline{\text{3V}}$ and $\overline{\text{CMDVCC}}$ fall at the same time. With the 73S8014BN, this will actually configure VCC to operate at 1.8 V. As a result, the 73S8014BN must have a setup time that must exceed 4 µs so the VCC will activate at 3.0 V.

4.5 Clock Divider

As described in section 0, the clock divider configuration is different between the 73S8024RN and the 73S8014BN. If the host can configure the CLKDIV pins on the 73S8024RN, then the control method may require the addition of resistors or external logic if divisor rates of divide by 1 or divide by 8 are required.

5 Dual Footprint Schematic and Layout

5.1 Schematic

If having a dual footprint layout able to support both the 73S8024RN and 73S8014BN is desired, then the schematic shown in Figure 1 will accomplish this. This schematic allows for either the 73S8024RN or 73S8014BN device to be used in a given application to allow for the greatest flexibility in manufacturing. Using this schematic and adhering to the firmware precautions in Section 4 allow the full interchangeability of using either the 73S8024RN or 73S8014BN.

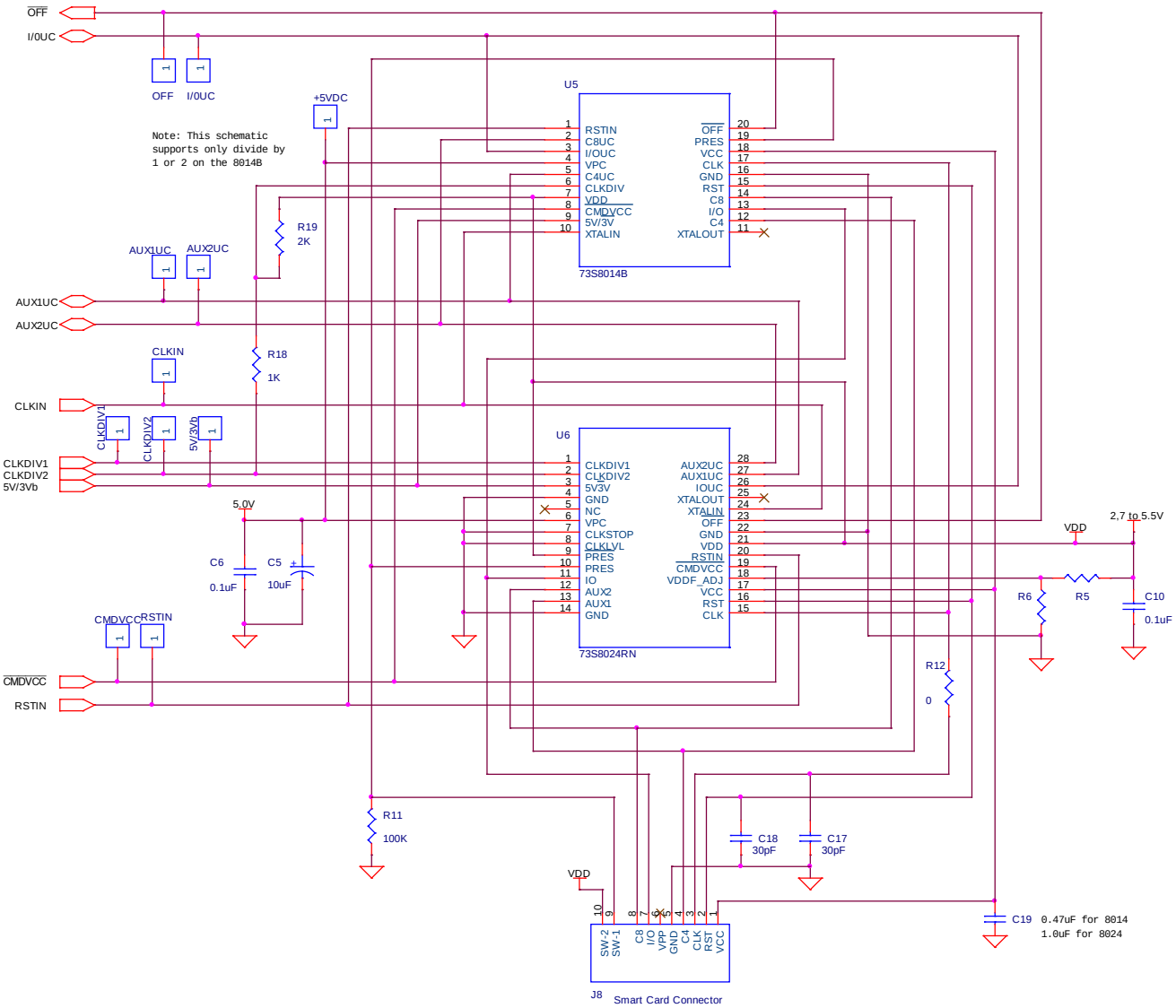

Figure 1: 73S8024RN and 73S8014BN Dual Schematic

5.2 Layout

An example of the dual layout of the schematic shown in 1 is shown in the following figures. The 73S8024RN and 73S8014BN are shown overlapping each other on the top of the PCB and the smart card connector is on the bottom. The smart card connector used is a full size smart card connector with card detection switch used on all Teridian smart card evaluation boards. See any 73S80xx Evaluation Board Users Guide for further details. Figure 2 shows the top and bottom silk screen with green showing the top and brown showing the bottom. The top layer is shown in Figure 3 and the bottom layer is shown in 4.

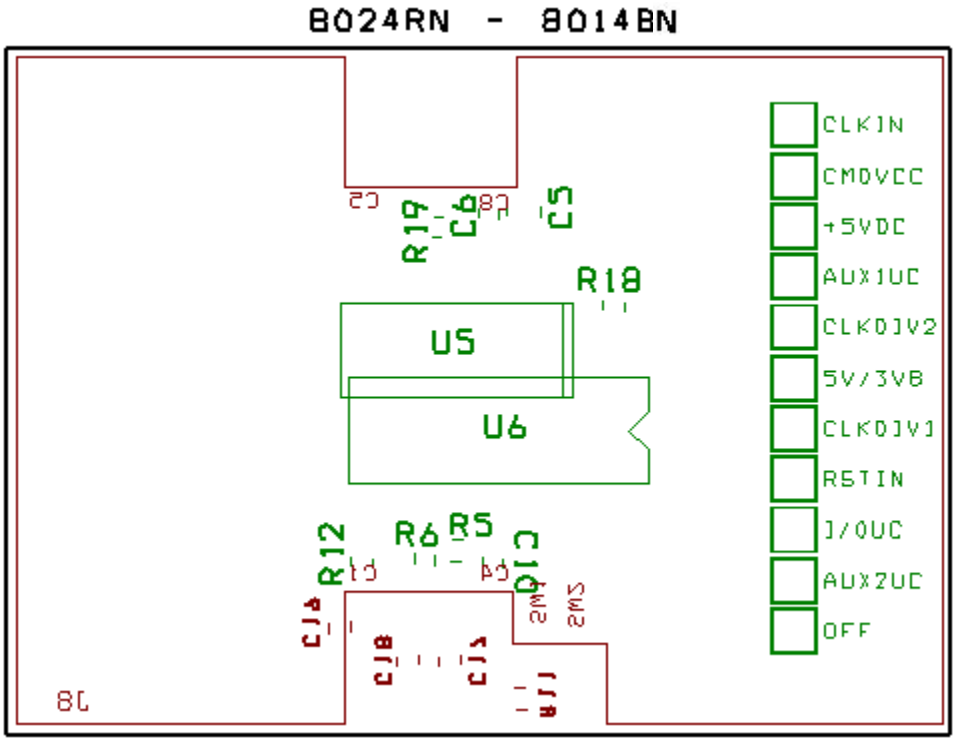

Figure 2: 73S8024RN and 73S8014BN Dual Layout Top and Bottom Silk Screen

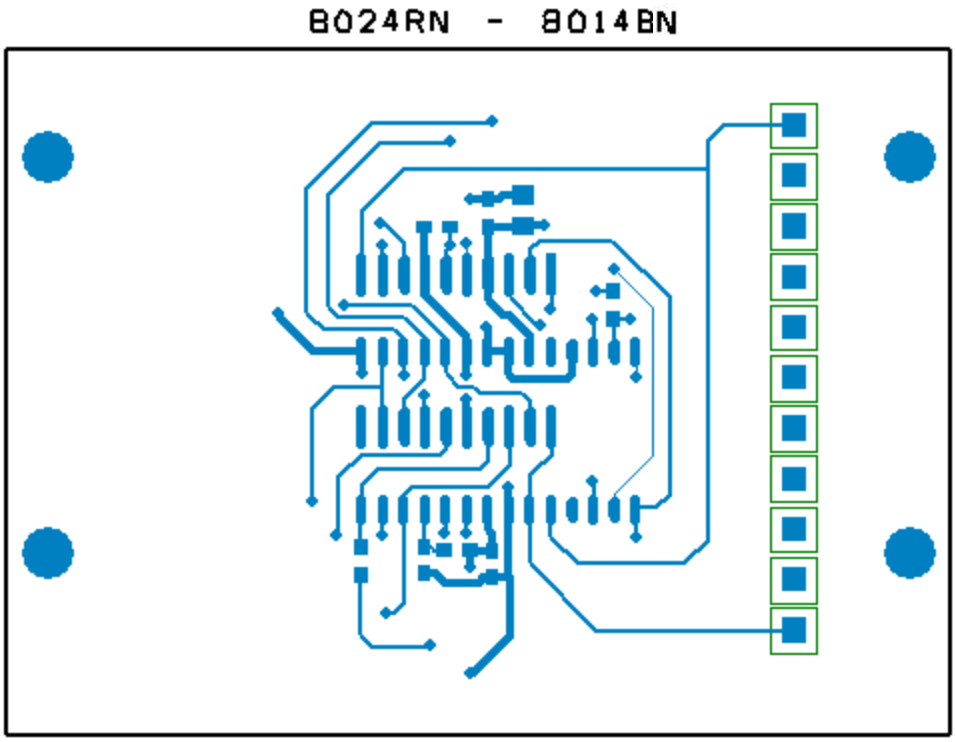

Figure 3: 73S8024RN and 73S8014BN Dual Layout – Top Layer

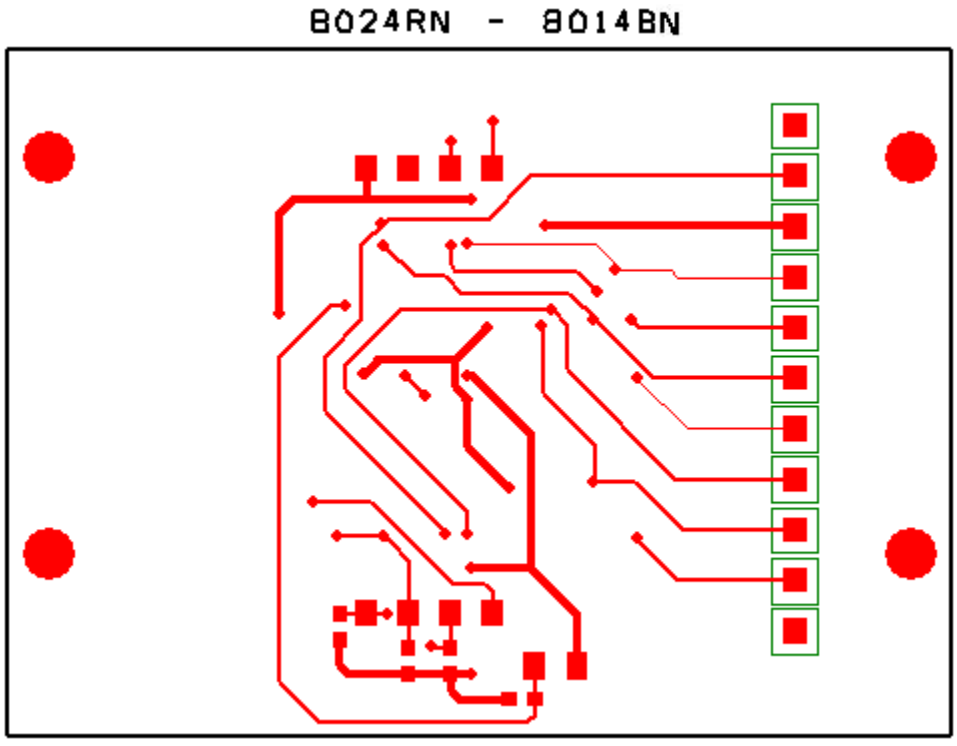

Figure 4: 73S8024RN and 73S8014BN Dual Layout – Bottom Layer

Revision History

Revision	Date	Description
1.0	1/29/2010	First publication.