Product Change Notification / SYST-10KUJJ120

Date:

11-Aug-2022

Product Category:

Ethernet Switches

PCN Type:

Document Change

Notification Subject:

Data Sheet - KSZ8567R Data Sheet

Affected CPNs:

SYST-10KUJJ120_Affected_CPN_08112022.pdf
SYST-10KUJJ120_Affected_CPN_08112022.csv

Notification Text:

SYST-10KUJJ120

Microchip has released a new Datasheet for the KSZ8567R Data Sheet of devices. If you are using one of these devices please read the document located at KSZ8567R Data Sheet.

Notification Status: Final

Description of Change:
-Section 5.1.4.72, "Global PM Available Register" The following has been defeatured in the document: 'low latency cut through mode' and 'time aware traffic scheduler per port'.
-Table 3-2, "Pin Descriptions" Updated Port Receive Error pin definition: from “MII Mode” to “MII/RMII Modes” and “RMII/RGMII Modes” to “RGMII Mode”.
-Table 3.2.1, "Configuration Straps" Updated strapping pin high instructions from “a non-LED pin” to “any pin”.
-Table 3-3, "Configuration Strap Descriptions" Updated In-Band Management to include the following note: “If using I2C, do not enable IBA.”
-Section 4.1.5, "Auto-Negotiation" Updated auto-negotiation bypass paragraph, changing “operating mode” to “operating speed”. Also added this sentence to the end of the paragraph: “With parallel detection, the duplex will always be half-duplex.”
-Section 5.1.1.6, "Global Interrupt Status Register" Updated field 29:0 definition: from “Reserved” to “APB Timeout Interrupt Status”.
-Section 5.1.1.7, "Global Interrupt Mask Register" Updated field 29:0 definition: from “Reserved” to “APB Timeout Interrupt Mask”.
-Section 5.1.2.3, "In-Band Management (IBA) Control Register" Updated bit 31 IBA Enable definition to add the following note: “If using I2C, do not enable IBA.”
-Section 5.1.4.72, "Global PM Available Register" Added new register to accommodate Packet Memory Available Block Count.

-Section 5.1.6.1, "Global PTP Clock Control Register" Added the following note to bit 1 definition: “The PTP Clock must be enabled when using the time stamp units (TSU) or trigger output units (TOU), even if IEEEE 1588 is not implemented.”
-Section 5.1.6.21, "Trigger Output Unit Control 2 Register" Added the following note to the definition of bits 0- 31: “The minimum value for this parameter is 0x50.”
-Section 5.1.6.24, "Trigger Output Unit Control 5 Register" Removed the following sentence from the description of this register: “This register contains the PTP event trigger output PPS signal pulse width for unit 2 and path delay compensation for unit 1.”
-Section 5.2.2.17, "Port Special Register" Added new register to accommodate Single-LED Mode Workaround Bit.
-Section 5.2.7.4, "Port Authentication Control Register" Updated bit 2 Access Control List (ACL) Enable definition from “0 = enable” to “0 = disable”.
-Section 5.2.8.3, "Port Transmit Queue Control 0 Register" Updated bits 4-5 Shaper Mode definition from: “10 = Time aware shaper (TAS) per IEEE 802.1Qbv for TSN” to “Reserved”.
-Section 5.2.9.3, "Port Transmit Queue Memory Register" Added new register to accommodate Port N Transmit Queue Blocks Used.
-Section 5.4.2, "MMD LED Mode Register" Updated bit 4 definition by adding the following sentence: “For Single-LED mode, set this bit and also set bit 9 in register 0xN13C-0xN13D.”
-Table 5-3, "Data Rate Selection Table for Ingress and Egress Rate Limiting" Updated 7d’1 - 7d’10 1000Mbps BPS definition from “1Mbps” to “10Mbps”.
-Section FIGURE 4-10:, "Power Connection Diagram" Updated AVDDH power supply option to include 3.3V.
-Section 5.2.2.1, "PHY Basic Control Register" Add the following note after bit 6 Reserved: “Bit 6 must be set to 0 when auto-negotiation is disabled.”
-Section 6.4.8, "Power-up and Reset Timing" For Note 3, updated first sentence from: “The recommended power down sequence is to power down the low voltage core before powering down the transceiver and digital I/O voltages, or to have all supplies power down in unison” to “The power supplies may be powered down in any sequence.”

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 11 Aug 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices::N/A

Attachments:

KSZ8567R Data Sheet

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Affected Catalog Part Numbers (CPN)

KSZ8567RTXI
KSZ8567RTXV-VAO
KSZ8567RTXV-TRV01
KSZ8567RTXV-TRV03
KSZ8567RTXV-TRVAO
KSZ8567RTXI-TR