BLC9H10XS-300P

Power LDMOS transistor

Rev. 1 — 29 May 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

300 W LDMOS power transistor for base station applications at frequencies from 600 MHz to 960 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a class-AB production circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	925 to 960	1000	48	60	21	34	–47 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

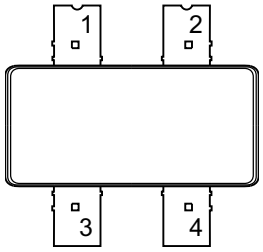
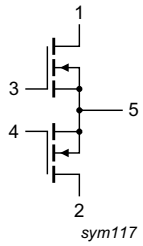
- 50 V operation voltage
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifier for W-CDMA base stations and multi carrier applications in the 600 MHz to 960 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9H10XS-300P	-	air cavity plastic earless flanged package; 4 leads	SOT1273-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	108	V
V_{GS}	gate-source voltage		–0.5	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 48 V; I_{Dq} = 1000 mA; T_{case} = 80 °C		
		P_L = 60 W	0.248	k/W
		P_L = 90 W	0.255	k/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.7 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 100 mA	1.5	2	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 48 V; I_D = 1.2 A	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 48 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	16	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	-	6.7	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.5 A	-	0.24	-	Ω

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on CCDF; 3GPP test model 1; 64 DPCH; f_1 = 927.5 MHz; f_3 = 957.5 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 1000 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 60 W	19.8	21	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 60 W	27	34	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 60 W	-	−21	−13	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 60 W	-	−47	−39	dBc

Table 8. RF characteristics

Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; f = 960 MHz; RF performance at V_{DS} = 48 V; I_{Dq} = 1000 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression		300	340	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9H10XS-300P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 48 V; I_{Dq} = 1000 mA; P_L = 240 W (CW); f = 925 MHz; tested on the common-source class-AB development test circuit.

7.2 Impedance information

Table 9. Typical impedance of maximum power and drain efficiency

Measured load-pull data (half section); I_{Dq} = 600 mA; V_{DS} = 50 V; typical values unless otherwise specified.

f	Z_S [1]	Z_L [1]	P_L	η_D	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
920	6.1 – j3.1	2.6 + j0.6	219	64.9	20.7
942	5.9 – j4.3	2.7 + j0.3	224	63.9	20.4
960	6.1 – j4.0	2.7 + j0.3	224	64.6	20.4
Maximum drain efficiency load					
920	6.1 – j3.1	2.1 + j2.6	145	75.2	23.3
942	5.9 – j4.3	1.9 + j2.4	141	76.2	23.2
960	6.1 – j4.0	1.9 + j2.4	135	75.7	23.3

[1] Z_S and Z_L defined in Figure 1.

[2] 8.0 dB power back off from 3 dB gain compression points.

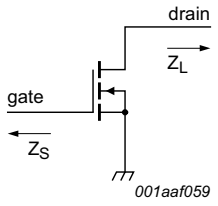
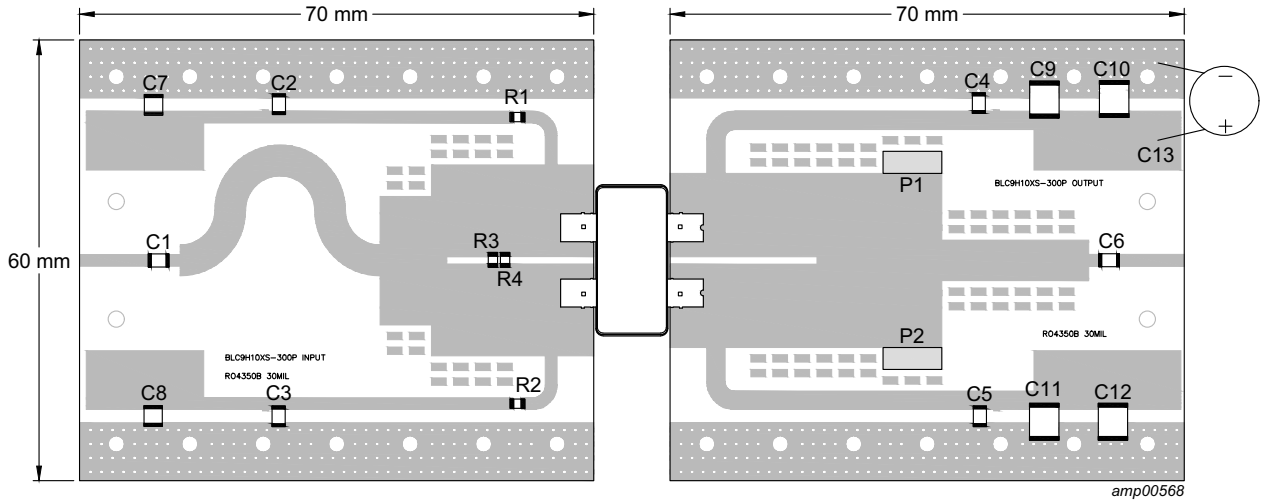


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RO4350B: ε_r = 3.5; thickness = 0.762 mm; thickness copper plating = 35 μm. See Table 10 for a list of components.

Fig 2. Component layout for common-source class-AB development test circuit

Table 10. List of components

See Figure 2 for component layout.

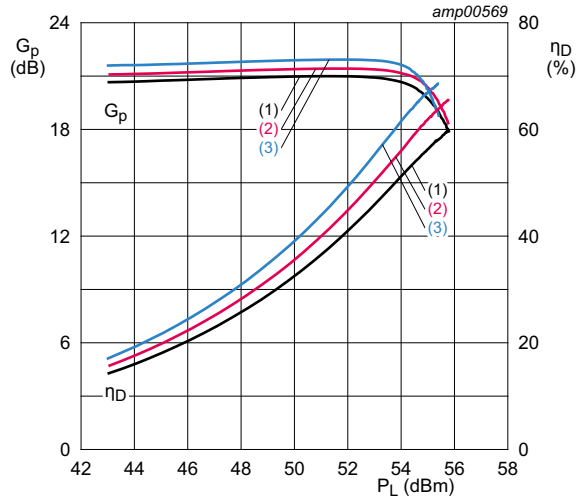
Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	43 pF	ATC 800B
C7, C8	multilayer ceramic chip capacitor	1 μF, 50 V [1]	
C9, C10, C11, C12	multilayer ceramic chip capacitor	10 μF, 100 V [1]	
C13	electrolytic capacitor	1000 μF, 100 V	
R1, R2, R3, R4	chip resistor	9.1 Ω	SMD 0805
P1, P2	copper foil		

[1] Murata or capacitor of same quality

7.4 Graphical data

All data are measured on the common-source class-AB development test circuit.

7.4.1 Pulsed CW



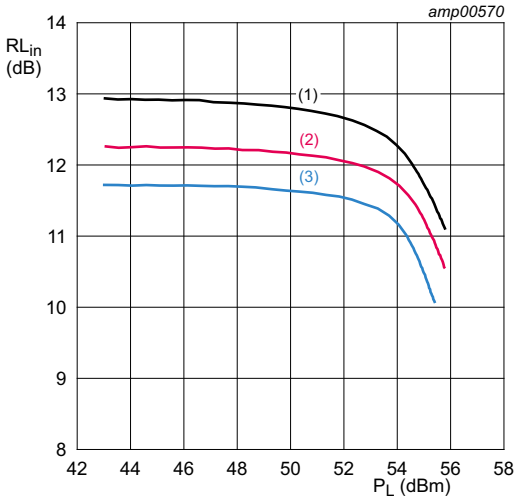
V_{DS} = 48 V; I_{Dq} = 1000 mA; t_p = 100 µs; δ = 10 %.

(1) f = 925 MHz

(2) f = 942 MHz

(3) f = 960 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 1000 mA; t_p = 100 µs; δ = 10 %.

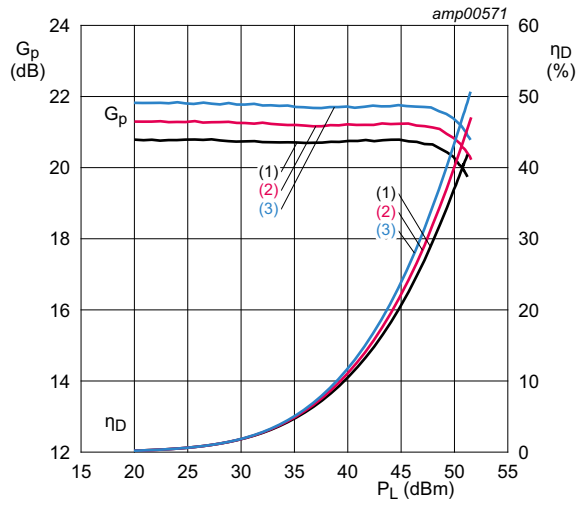
(1) f = 925 MHz

(2) f = 942 MHz

(3) f = 960 MHz

Fig 4. Input return loss as a function of output power; typical values

7.4.2 1-Carrier W-CDMA



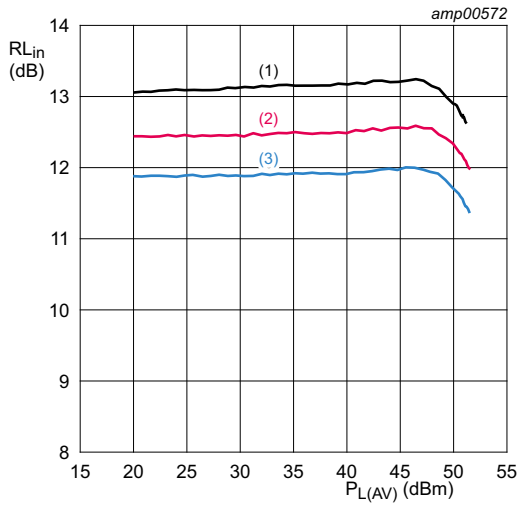
V_{DS} = 48 V; I_{Dq} = 1000 mA; 46 % clipping.

(1) f = 925 MHz

(2) f = 942 MHz

(3) f = 960 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



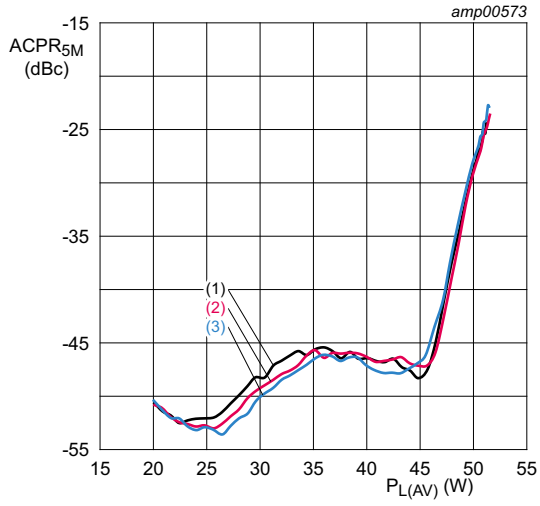
V_{DS} = 48 V; I_{Dq} = 1000 mA; 46 % clipping.

(1) f = 925 MHz

(2) f = 942 MHz

(3) f = 960 MHz

Fig 6. Input return loss as a function of output power; typical values



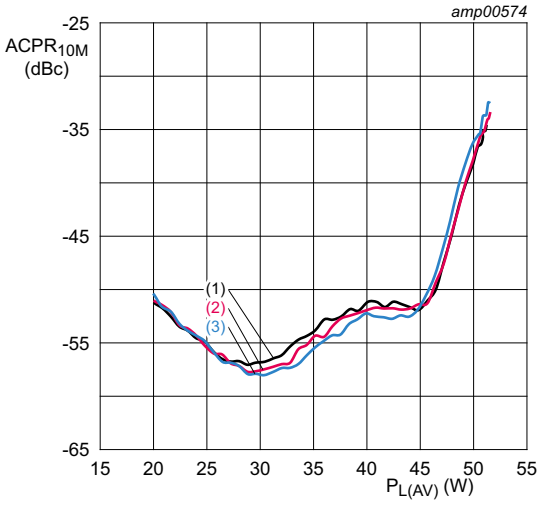
V_{DS} = 48 V; I_{Dq} = 1000 mA; 46 % clipping.

(1) f = 925 MHz

(2) f = 942 MHz

(3) f = 960 MHz

Fig 7. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 48 V; I_{Dq} = 1000 mA; 46 % clipping.

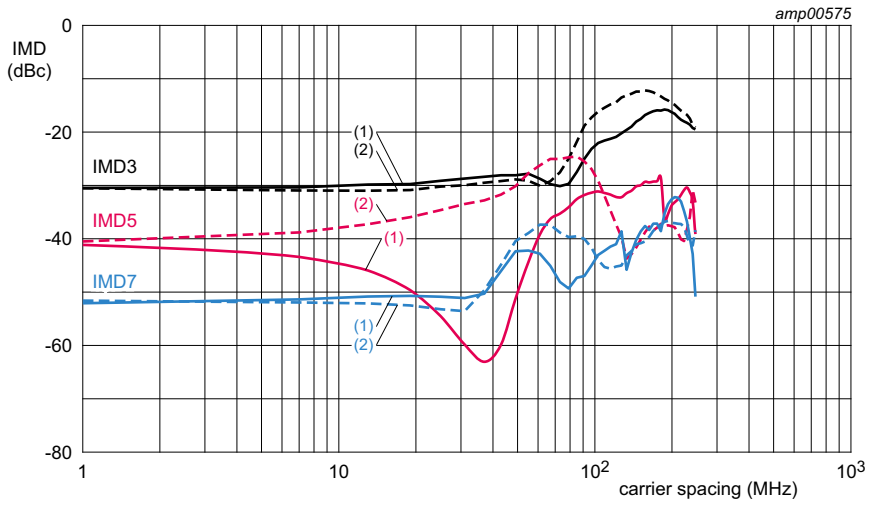
(1) f = 925 MHz

(2) f = 942 MHz

(3) f = 960 MHz

Fig 8. Adjacent channel power ratio (10 MHz) as a function of output power; typical values

7.4.3 2-Tone VBW



V_{DS} = 48 V; I_{Dq} = 1000 mA; f_c = 942 MHz.

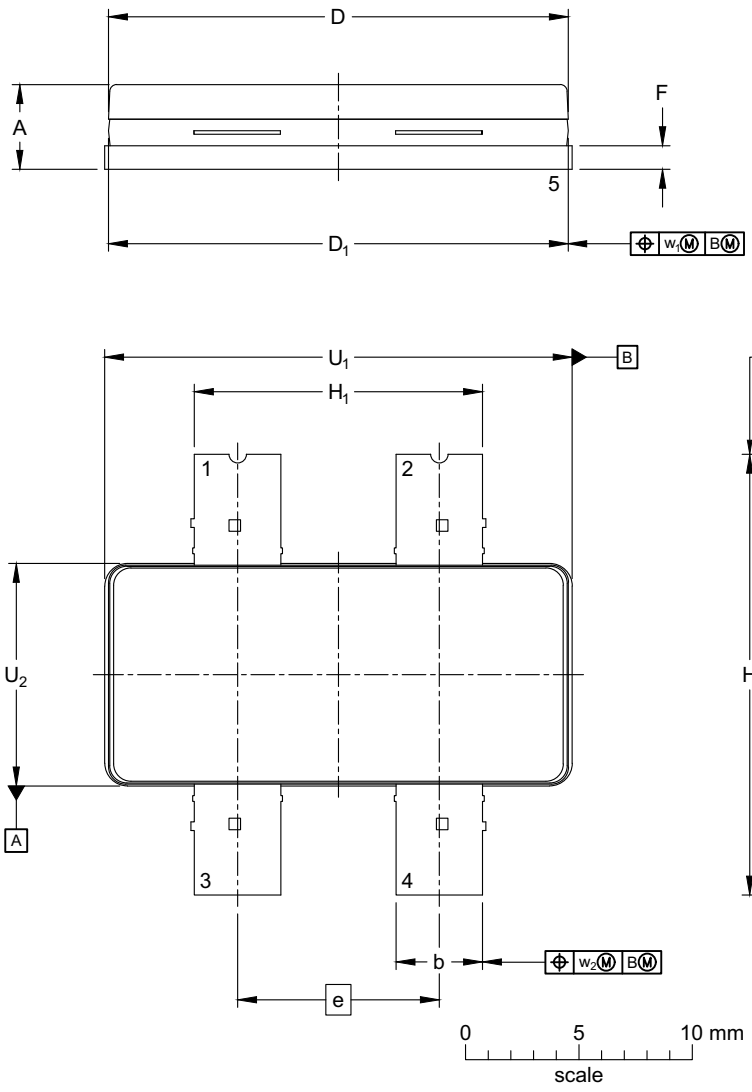
(1) IMD low

(2) IMD high

Fig 9. VBW capability on common-source class-AB development RF test circuit

8. Package outline

Air cavity plastic earless flanged package; 4 leads SOT1273-1



Dimensions

Unit		A	b	c	D	D_1	E	E_1	e	F	H	H_1	$Q^{(1)}$	U_1	U_2	v	w_1	w_2	y
mm	max	4.01	3.91	0.18	20.42	20.37	9.80	9.75		1.14	19.53	12.83	1.68	20.70	9.91	0.50	0.50	0.50	0.10
	nom								8.89										
	min	3.40	3.71	0.13	20.12	20.17	9.50	9.55		0.94	19.33	12.57	1.45	20.50	9.70				

Note:
1. Dimension Q is measured at 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1273-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1273-1						17-01-12

Fig 10. Package outline SOT1273-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2B is granted to any part that passes after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video Bandwidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9H10XS-300P v.1	20180529	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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