# CHANGE NOTIFICATION

Analog Devices, Inc.
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March 09, 2018 PCN_030918

Dear Sir/Madam:

**Subject: Notification of Change to LTM2893, LTM2893-1 Datasheet**

Please be advised that Analog Devices, Inc. Milpitas, California has made a minor change to the LTM2893, LTM2893-1 product datasheet to reconcile an electrical table limit with guidance provided in the Applications Information section of the datasheet. The changes are shown on the attached pages of the marked up datasheet. There was no change in form, fit, function, quality or reliability of the product. The product shipped after May 09, 2018 will be tested to the new limits.

Should you have any questions or concerns please contact your local Analog Devices sales representatives or you may contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@ANALOG.COM. If I do not hear from you by May 09, 2018, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

| For questions on this PCN, please contact Jason Hu or you may send an email to your regional contacts below or contact your local ADI sales representatives. | | | |
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## SWITCHING CHARACTERISTICS

**The ● denotes the specifications which apply over the full specified operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 5V, $V_L$ = 3.3V, GND = 0V, $V_{CC2}$ = 5V, $V_{L2}$ = 3.3V, GND2 = 0V unless otherwise noted. (Note 9)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Conversion Start** | | | | | | | |
| $t_{CNVH}$ | CNV Pulse Width | | ● | 20 | | | ns |
| $t_{BUSYLH}$ | CNV↑ to BUSY↑ Delay | | ● | | | 40 | ns |
| $t_{DCNV}$ | CNV↑ to CNV2↑ Delay (Aperture Delay) | | ● | 12 | 21 | 33 | ns |
| $t_{CNV2H}$ | CNV2 Pulse Width | (Config. SCK2 Frequency ≥ 40MHz) | ● | 20 | | 52 | ns |
| | | (Config. SCK2 Frequency ≤ 33MHz) | ● | 35 | | 80 | ns |
| | CNV to CNV2 Rising Edge Jitter RMS | (Note 7) | | | 30 | | ps |
| | Minimum Low Time for CNV | | | 100 | | | ns |
| **SPI Timing** | | | | | | | |
| $t_{QUIET}$ | SCK or $\overline{SS}$↑ Space to CNV↑ | LTM2893<br>LTM2893-1, Configuration Register = 0x9F | ● | 20<br>320 | | | ns<br>ns |
| $t_{SCK}$ | SCK Input Period | SCK2 Frequency 100MHz LTM2893 (Note 3)<br>SCK2 Frequency 100MHz LTM2893-1 (Note 3) | ●<br>● | 10<br>10 | | <br>1185 | ns<br>ns |
| $t_{SCKH}$ | SCK Input High Time | (Note 2) | ● | 4 | | | ns |
| $t_{SCKL}$ | SCK Input Low Time | (Note 2) | ● | 4 | | | ns |
| $t_{SCK2}$ | SCK2 Output Period | SCK2 Frequency 100MHz (Notes 3, 8) | ● | 9.5 | 10 | 10.8 | ns |
| $t_{SCK2H}$ | SCK2 Output High Time | (Note 2) | ● | 4 | | | ns |
| $t_{SCK2L}$ | SCK2 Output Low Time | (Note 2) | ● | 4 | | | ns |
| $t_{HDMISO2}$ | MISOA2, MISOB2 Data Hold Time from SCK2↑ | (Note 2) | ● | 1 | | | ns |
| $t_{DMISO}$ | MISOA, MISOB Data Valid Delay from SCK↑<br>SCK2 Frequency = 100MHz or 66MHz or from SCK↓ SCK2 Frequency ≤ 50MHz | $C_L$ = 20pF, $V_L$ = 5.5V (Note 2)<br>$C_L$ = 20pF, $V_L$ = 2.5V (Note 2)<br>$C_L$ = 20pF, $V_L$ = 1.71V (Note 2) | ●<br>●<br>● | | 5 | 7.5<br>8<br>9.5 | ns<br>ns<br>ns |
| $t_{SUMISO2}$ | MISOA2, MISOB2, Setup Time to SCK2↑ | (Note 2) | ● | 1.8 | | | ns |
| $t_{HMISO}$ | MISOA, MISOB Data Remains Valid Delay from SCK↑<br>SCK2 Frequency = 100MHz or 66MHz or from SCK↓ SCK2 Frequency ≤ 50MHz | $C_L$ = 20pF (Note 2) | ● | 2 | | | ns |
| $t_{DMISOSSF}$ | MISOA, MISOB Data Valid Delay from $\overline{SS}$↓ | $C_L$ = 20pF | ● | | | 10 | ns |
| | MISOA, MISOB Data Valid Delay from BUSY↓ | $\overline{SS}$ = 0V, LTM2893 | ● | | | 10 | ns |
| $t_{SSFSCK}$ | $\overline{SS}$↓ Delay to SCK↑ | SCK2 Frequency 100MHz (Note 8), LTM2893-1 | ● | 20 | | 1185 | ns |
| $t_{BUSYFSCKR}$ | BUSY↓ Delay to SCK↑ | $\overline{SS}$ = 0V, SCK2 Frequency 100MHz (Notes 9, 10) | ● | ~~15~~ 20 | | | ns |
| $t_{BUSY2FSS2F}$ | BUSY2↓ Delay to $\overline{SS2}$↓ | | ● | 15 | | 35 | ns |
| $t_{BUSY2FBUSYF}$ | BUSY2↓ to BUSY↓ | SCK2 Frequency 100MHz | ● | | | 100 | ns |
| $t_{SS2FSCK2}$ | $\overline{SS2}$↓ Delay to SCK2↑ | SCK2 Frequency 100MHz | ● | 15 | | 33 | ns |
| $t_{DIS}$ | Bus Relinquish Time After $\overline{SS}$↑ | | ● | | | 35 | ns |
| $t_{SCKSSDIS}$ | Last SCK↑ to $\overline{SS}$↑ | SCK2 Frequency 100MHz (Note 8) LTM2893-1 | ● | 20 | | 1185 | ns |
| $t_{SCK2SSDIS}$ | Last SCK2↑ to $\overline{SS2}$↑ | SCK2 Frequency 100MHz | ● | 8 | | | ns |
| | $\overline{SS}$↑ to $\overline{SS}$↓ Space | CRCENA Bit = 0 | | 60 | | | ns |
| | | CRCENA Bit = 1 | | 225 | | | ns |
| $t_{SUMOSI}$ | MOSI Setup to SCK↑ | LTM2893-1 or Configuration Port Write (Note 2) | ● | 1.5 | | | ns |
| $t_{HDMOSI}$ | MOSI Hold Time to SCK↑ | LTM2893-1 or Configuration Port Write (Note 2) | ● | 1 | | | ns |
| $t_{SS2FMOSI2}$ | $\overline{SS2}$↓ to MOSI2 Valid | LTM2893-1 | ● | | | 8 | ns |

## APPLICATIONS INFORMATION

The direction of the SA, SB, or SC signals may be changed independently with the configuration register. The default condition of '0' for each select bit maintains the signal flow from logic-to-isolated. Loading a '1' into the direction bits will change the direction for that pin(s) to isolated-to-logic.

*Warning: Careful planning is required for the use of SA, SB, and SC signals. Figure 12 shows the regions were transitions are safe and not safe for the logic side interface.*

The select signals are sampled and transferred as a packet of the current value of the three signals. The select signal sampling will have up to 10ns of sampling jitter. If a signal transitions after another signal was sampled and is in the process of being transferred to the adjacent side, it will be delayed until the next available transmission slot. The delay may cause a perceived jitter or uncertainty of 80ns.

### CONFIGURATION REGISTER

The LTM2893 contains a configuration register to adjust parameters of the speed and features of the ADC write and read process. After power up, write the configuration register by setting the $\overline{CSC}$ chip select input low and clocking in a one-byte configuration word with SCK and MOSI. The configuration register contains two bytes where the most significant bit of the SPI word selects which byte is addressed. Complete each configuration word by reasserting $\overline{CSC}$ high. The isolated side will be configured through an internal communication.

Table 3 shows the configuration register bit map for controlling the operation and frequency of the logic and isolated interfaces. The configuration register allows adjustment of the default SCK frequency, direction of the SA, SB, SC to SA2, SB2, SC2 signals, the length of the SPI word and number of SPI words to process per $\overline{SS}$ cycle. Figure 8 demonstrates access to the configuration register.

### ~~SCK2 FREQUENCY~~ SCK AND SCK2 FREQUENCY

The SCK2 frequency selection list is shown in Table 4. Select the SCK2 frequency that is equal or less than the specifications of the ADC's SPI port. Example: the LTC2338 has a 100MHz SCK maximum, 10ns minimum SCK period; therefore configure SCK2 for 100MHz.

The isolated SCK2 frequency is an internal trimmed oscillator. Graph SCK2 Frequency Variation versus Temperature shows the minimum and maximum characteristics over temperature and trim variation of the SCK2 frequency.

The logic side SPI SCK frequency cannot exceed the SCK2 frequency or else a SPI buffer under-run may occur. Equation 1 shows the relationship of SCK and SCK2 along with the delay between the BUSY falling edge and the first SCK rising that meet timing and will not under run the buffer. Replace this text with attached version parallel ADCs and the default DE y needed to meet timing at the m is equal to a single SCK cycle or the minimum SS to SCK required, therefor no additional delay is required. Access the LTM2893 with an SCK frequency between 0.925 • SCK2 and 0.00795 • SCK2, or with a delay calculated with Equation 1. This guarantees the internal SPI buffer will not under-run. In the case of a buffer under-run, the $\overline{FAULT}$ flag will assert low.

Equation 1:

$$SCK \leq \frac{WORD\ COUNT \bullet WORDLENGTH - 1}{\frac{WORD\ COUNT \bullet WORDLENGTH - 2}{SCK2 \bullet 0.925} - t_{BUSYFSCKR}}$$

Or for a maximum SCK find the $t_{BUSYFSCKR}$ needed

$$t_{BUSYFSCKR} \geq \left(\frac{WORD\ COUNT \bullet WORDLENGTH - 2}{SCK2 \bullet 0.925}\right) - \left(\frac{WORD\ COUNT \bullet WORDLENGTH - 1}{SCK_{MAX}}\right)$$

Note: SCK2 is the nominal configured value. SCK2 • 0.925 is the worst case value at maximum operating temperature.

where:

$t_{BUSYFSCKR}$ = delay from BUSY fall to $\overline{SS}$ fall + $t_{SSFSCK}$

## SCK AND SCK2 FREQUENCY

The logic-side SPI SCK frequency may be selected within a range that is dependent on the isolated-side's SCK2 frequency. The minimum SCK frequency is limited to avoid triggering the watchdog timer and the maximum SCK frequency is limited to prevent a SPI buffer under-run.

To prevent a watchdog time out, the logic-side SPI SCK frequency must be at least 0.00795 times SCK2. If a watchdog timeout occurs, the FAULT flag will assert low.

To prevent a SPI buffer under-run, either the logic-side SPI SCK frequency must be less than the SCK2 frequency or there needs to be a sufficient delay after BUSY falls, t_BUSYFSCKR, so that the buffer will be full enough to allow its reading at the desired logic-side SPI SCK frequency. If these conditions are not met and a buffer under-run occurs, then the FAULT flag will assert low.

Accounting for temperature and trim variations, the lowest SCK2 frequency will be 0.925 times the nominal SCK2 frequency.

The delay t_BUSYFSCKR is calculated using Equation 1 and Table 2 lists values of t_BUSYFSCKR for common operating conditions.

Equation 1:

$$t_{BUSYFSCKR} \geq \max\left[\left(\frac{WORDCOUNT \times WORDLENGTH - 2}{SCK2 \times 0.925}\right) - \left(\frac{WORDCOUNT \times WORDLENGTH - 1}{SCK_{MAX}}\right) + 2\text{ns}, t_{SSFSCK,MIN}\right]$$

where t_BUSYFSCKR is the time between the falling edge of BUSY and the 1st rising edge of SCK, SCK2 is the nominal configured frequency in Hz and SCK_MAX is the maximum frequency in Hz.

Note that provided the timing for SCK_MAX doesn't violate the other SCK timing specifications, SCK_MAX may exceed SCK2 if the corresponding t_BUSYFSCKR is observed.

Note that the minimum t_SSFSCK of 20ns must also be independently satisfied and so if the falling edge of SS is delayed sufficiently past the falling edge of BUSY, then the reading may need to be delayed beyond the value of t_BUSYFSCKR calculated in Equation 1.

When the number of bits to be transferred (WORDCOUNT*WORDLENGTH) is equal to or less than 32 bits, the delay needed to meet timing at the maximum SCK frequency of 100MHz is equal to the minimum SS to SCK required and therefore no additional delay is required.

## APPLICATIONS INFORMATION

**Table 2. BUSY Fall to SCK Rising Delay Required for Major Word Boundaries to Operate at Maximum SCK Under Worst Case SCK2 Tolerance**

| $t_{BUSYFSCKR}$ | TOTAL NUMBER OF BITS PER SPI TRANSACTION | | | |
|---|---|---|---|---|
| SCKMAX | 32 | 64 | 96 | 128 |
| 100MHz | 20 ns | 43 ns | 69 ns | 95 ns |
| 66MHz | 24 ns | 64 ns | 103 ns | 142 ns |
| 50MHz | 31 ns | 83 ns | 135 ns | 187 ns |
| 40MHz | 38 ns | 103 ns | 168 ns | 233 ns |
| 33MHz | 46 ns | 125 ns | 203 ns | 282 ns |
| 25MHz | 60 ns | 164 ns | 267 ns | 371 ns |
| 12.5MHz | 117 ns | 325 ns | 532 ns | 740 ns |
| 6.25MHz | 232 ns | 647 ns | 1062 ns | 1477 ns |

Add time delay to the Master FPGA or microcontroller between the BUSY fall and the first SCK in order to operate SCK at the configured SCK2 frequency. A minimum $t_{SSFSCK}$ of 15ns is required in the timing specifications between a fall of $\overline{SS}$ and the first SCK or the fall of BUSY and the first SCK if $\overline{SS}$ is always low. Referencing Table 2, under most cases with a single or a pair of parallel devices connected to the LTM2893, the minimum or a single SCK period is required between the BUSY falling edge and the rising edge of the first SCK to support the maximum operating frequency. As the WORDLENGTH and DEVICECOUNT increases, the $t_{BUSYFSCKR}$ must be increased if operating near the maximum SCK.

### CYCLIC REDUNDANCY CHECK (CRC)

The CRC enable selection bit (Config Register 0, bit 3) enables an internal CRC process to be completed during the communication of SPI data across the internal isolation barrier. The CRC is a 3-bit message added to the end of a SPI data word and is checked on the receiver side. The CRC is an internal function and the values are not readable. If the check fails, the $\overline{FAULT}$ pin is asserted low. When CRC is enabled, an additional wait of 225ns is required for the CRC to complete processing before the reassertion of a new SPI transaction or a new rising edge on CNV.

### DEVICECOUNT AND WORDLENGTH

The DEVICECOUNT configuration bits select the number of words the LTM2893 will process. The selection of this value is based on the number of ADCs isolated or the number of words that must be written or read from the ADC. The DEVICECOUNT selection is used in conjunction with the WORDLENGTH selection bits. The WORDLENGTH is set to the number of bits per word. The WORDLENGTH selection allows the SPI access to be tailored to a specific ADC result length to maximize throughput. When a controller that requires byte wide increments is used, set the word length to the number of bits on a byte size boundary (8, 16, 24, or 32). The total number of bits per SPI transaction is the WORD COUNT • WORDLENGTH as referenced in Table 6 and Table 7.

For example, a single 16-bit ADC is selected as DEVICECOUNT of 1-2 with a WORDLENGTH of 16. Two 16 bit ADCs in parallel (SDO of ADC1 connected to MISOA2 and SDO of ADC2 connected to MISOB2) are also selected as a DEVICECOUNT of 1-2 with a word length of 16. Chaining a device increases the DEVICECOUNT. Chaining two additional ADCs through the first pair of ADCs would change the DEVICECOUNT to 3-4 with a word-length of 16.

The DEVICECOUNT is interchangeable with the number of words, WORD COUNT, a device requires for communication. An example ADC may need 4 words of 32 bits. In this case, selecting the maximum DEVICECOUNT of 7-8 will write or read 4 words and setting the WORDLENGTH to 32 will set the length of each word. The LTM2893 writes or reads ½ the number of words as the DEVICECOUNT value. WORD COUNT is equal to ½ of DEVICECOUNT, see Table 7. A DEVICECOUNT of 1-2 will read 1 word, a DEVICECOUNT of 3-4 will read 2 words, a DEVICECOUNT of 5-6 will read 3 words, and a DEVICECOUNT of 7-8 will read 4 words.

### LTM2893-1 ADC READ/WRITE

The LTM2893-1 writes a SPI word to the isolated ADC after the read operation. On the logic side, a SPI transaction will output data from MISOA, MISOB and read in a command for the ADC in the MOSI pin. At start-up, prior