MAX2771 PLL Loop Filter Calculator User Guide

UG6827; Rev 0; 12/18

Abstract

This document briefly overviews PLL basic concepts and explains how to use the MAX2771 PLL loop filter spreadsheet calculator. The calculator allows the user to simulate the MAX2771 PLL for a given set of loop filter components or to calculate the required loop filter components to achieve a target loop bandwidth and phase margin.

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Introduction

The MAX2771 is a next-generation Global Navigation Satellite System (GNSS) receiver covering E5/L5, L2, E6, E1/L1 bands and GPS, GLONASS, Galileo, QZSS, IRNSS, and BeiDou navigation satellite systems on a single chip. This single-conversion GNSS receiver is designed to provide high performance for industrial and a wide range of consumer applications.

The MAX2771 includes an integrated voltage-controlled oscillator (VCO), a crystal oscillator, and a fractional-N frequency synthesizer to program the local oscillator (LO) frequency using different reference input frequencies.

A spreadsheet calculator for the PLL Loop filter design is available to download from the Design Resources tab for the MAX2771. This document describes how to use the PLL loop filter calculator.

Phase Locked Loops

Figure 1 shows the blocks of a generic PLL.

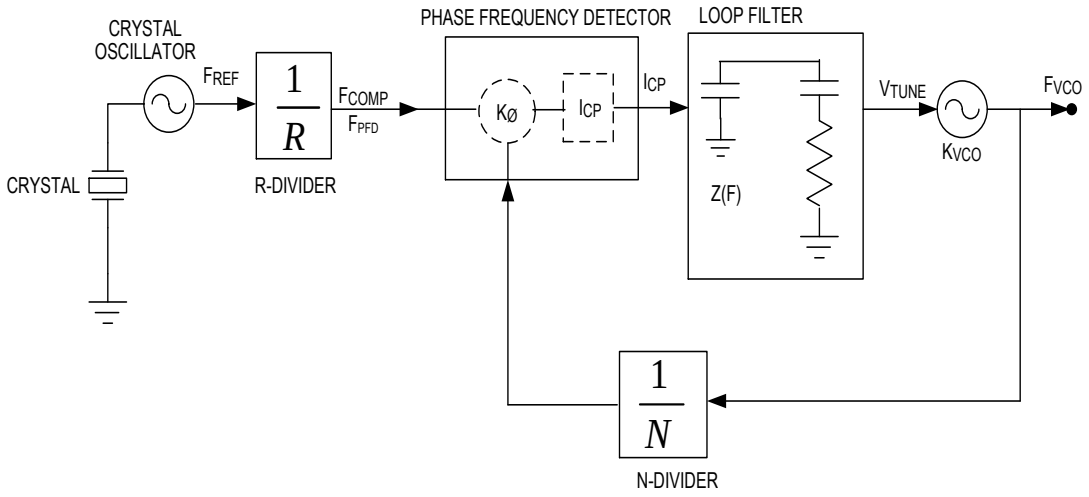

Figure 1. Generic PLL blocks.

The reference crystal oscillator frequency, F_{REF}, is divided by the reference divider, R-divider, to produce the comparison frequency (F_{COMP}) into the phase frequency detector (PFD).

The VCO frequency, F_{VCO}, is divided to produce the same F_{COMP} frequency by using the N-divider. In the event that the F_{VCO} is not an integer multiple of F_{COMP}, the PLL operates in fractional-N mode. In this case, the feedback divider is a sigma-delta modulator.

The PFD compares the frequency and phase differences between F_{VCO}/N and F_{REF}/R. The charge pump (CP) generates current pulses proportional to the mismatch.

The loop filter smooths and integrates the CP current to produce a voltage to tune the VCO frequency in the direction to eliminate the difference in phase and frequency between the two inputs to the PFD. The loop filter also serves to attenuate reference spurs.

Phase Noise in PLLs

Phase noise is a measure of short-term frequency deviation from the ideal frequency caused by random phase fluctuation, which is also called jitter in the time domain.

The phase noise is defined as the ratio of power measured in a 1Hz bandwidth at a specified offset to the total carrier power (dBc/Hz). It is customary to characterize an oscillator in terms of its single-sideband phase noise as shown in Figure 2.

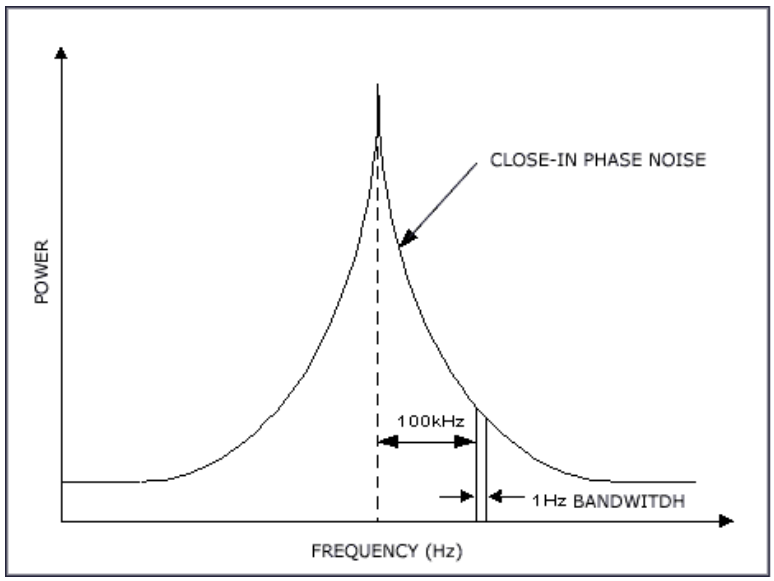

Figure 2. Phase noise plot.

Phase Noise Contributions from Different Blocks

The reference input, PFD, loop filter, VCO, feedback frequency divider, and sigma-delta modulator (if enabled) contribute to phase noise. The phase noise contribution of each block is weighted by a particular frequency response from the block to the PLL output.

All phase noise contributors, except for the VCO, are filtered by the PLL closed loop frequency response, H(f), which is low pass. The VCO phase noise is filtered by the PLL error response, which is high pass and is defined as 1 – H(f). As a result, the VCO phase noise is suppressed within the loop bandwidth. The other phase noise contributors are suppressed above the loop bandwidth.

These low-pass filtered phase noise contributors are weighted by the feedback division ratio, N.

The noise caused by the PFD and feedback divider is often called PLL noise and has a white or flat noise component and a flicker or 1/f component. The spreadsheet calculator treats these components as separate contributions.

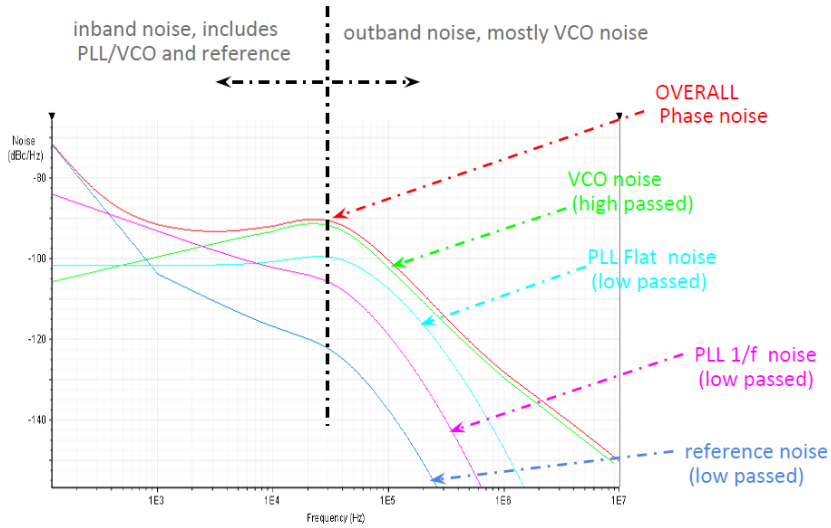

Figure 3. Phase noise contributions from different blocks.

Loop Filter

The loop filter integrates and filters the current pulses from the charge pump to generate the required VCO tuning voltage. The higher the loop filter order, the better the suppression of F_{COMP} related spurs. The loop filter can be passive or active. The PLL in the MAX2771 is passive.

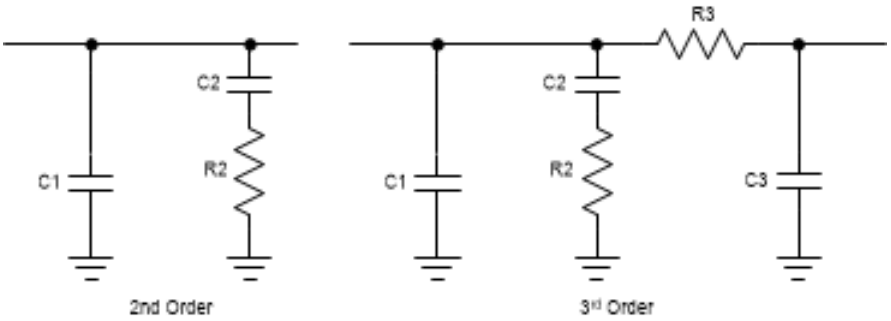

Figure 4. Different order loop filters.

The loop filter design is critical to get the desired performance from the PLL as there are many trade-offs between the design specifications that need to be met. The loop filter in the MAX2771 is third order. However, R3 and C3 that provide the third pole are integrated into the IC. The remaining components of the filter, C1, C2 and R2, are external components and, thus, can be changed.

Design Considerations

Designers must consider the following:

- PFD frequency: The higher the PFD frequency, the lower the N-divider value is and the better the phase noise is because the phase noise is directly proportional to the N-divider value (20×log(N)).
- Lock time: Lock time is the length of time to lock from one specified frequency to another specified frequency within a given frequency tolerance. Given that the MAX2771 PLL frequency is relatively static and does not dynamically switch from one frequency to another, the lock time is likely of little concern in most applications.
- Loop bandwidth: Loop bandwidth is a low-pass filter bandwidth that is achieved from the filter components. The wider the loop bandwidth, the shorter the lock time is, but the tradeoff is a worse spurious performance. The narrower the loop bandwidth, the better the spurious performance is but the lock time increases.
- PLL stability: For PLL stability, the phase margin must be greater than zero and is the difference between 180 degrees and the phase of the open-loop response when the magnitude of the open-loop response is 0dB. A minimum phase margin of 45 degrees is typically used.

How to Use the MAX2771 Loop Filter Spreadsheet Calculator

Overview

The loop filter spreadsheet calculator models the PLL as a linear model in the phase domain and is used to calculate the loop filter values and simulate the phase noise. The loop filter is a passive filter with capacitor and resistor values designated as C1, R2, and C2.

Figure 5 shows the correspondence between the filter components and these reference designators.

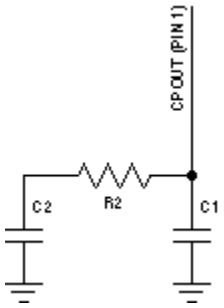

Figure 5. Loop filter components.

Input Controls

In the spreadsheet calculator, light-yellow cells contain user inputs that can be changed, whereas white colored cells are outputs derived from relevant formulae and cannot be changed.

Figure 6 and Figure 7 show the loop filter spreadsheet calculator GUI.

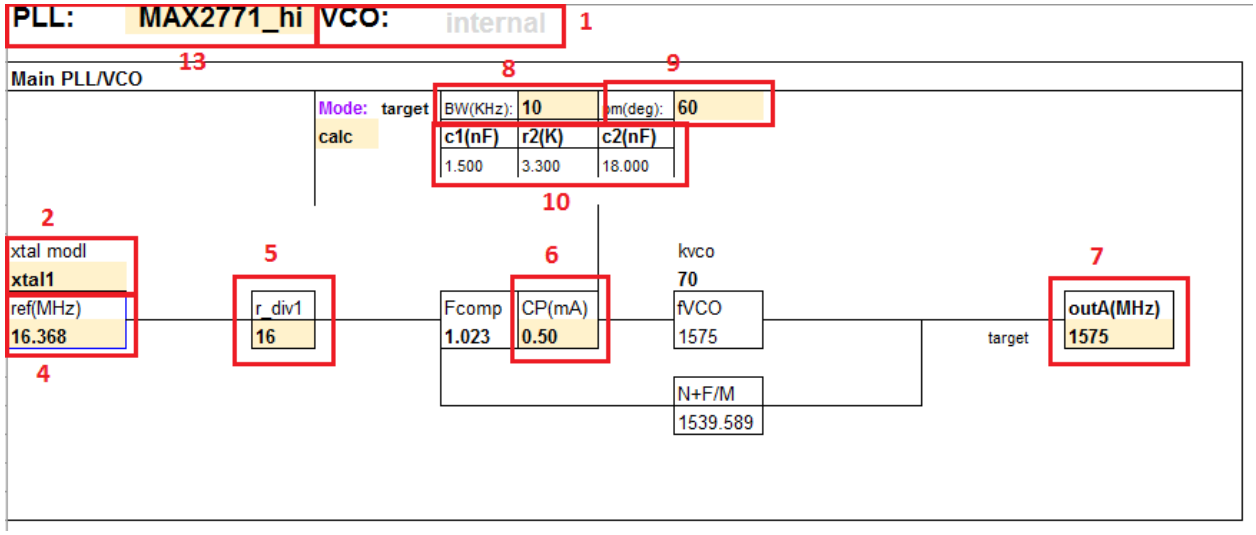

Figure 6. Loop filter spreadsheet calculator GUI.

The numbered spreadsheet calculator GUI components shown in Figure 6 and Figure 7 are described as follows:

1. The VCO phase noise is fixed and cannot be controlled because the MAX2771 has an integrated VCO.
2. Select the Xtal model from three options: xtal1, xtal2 and ideal.
3. Enter the reference phase noise input, as shown in Figure 7.

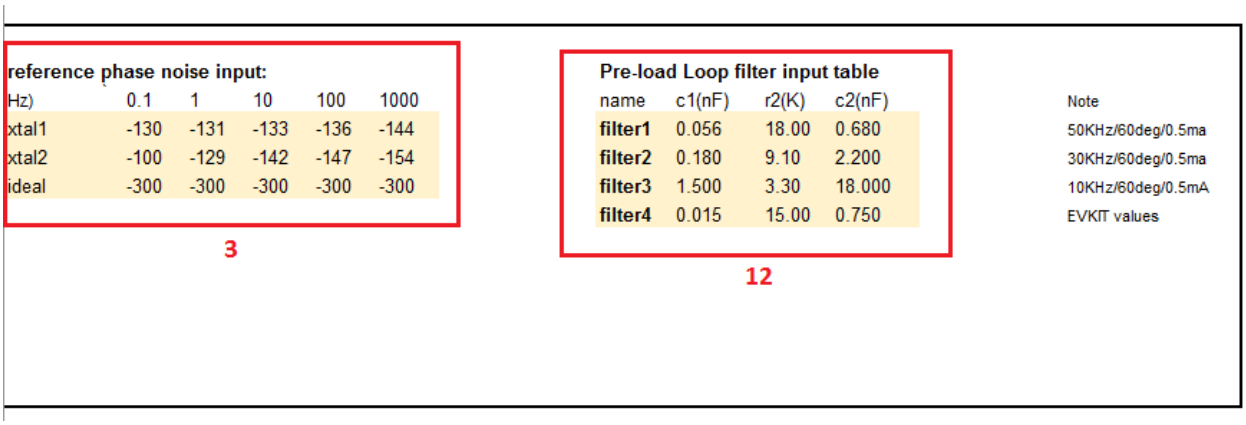

Figure 7. Reference phase noise input and pre-loaded loop filter inputs.

4. Enter the reference frequency input (ref(MHz)). The legal reference frequency range is 8MHz to 44MHz.
5. Enter the R-divider value. The legal R-divider value range is 1 to 1023 inclusive.
6. Select the charge pump current (CP(mA)) as either 0.5mA or 1mA.
7. Enter the desired PLL output (outA (MHz)), which has a legal range of 1525MHz to 1610MHz for the high-band VCO and 1160MHz to 1290MHz for the low-band VCO.
8. Set the mode to "calc" and enter the desired loop bandwidth (BW(KHz)).
9. Enter the desired phase margin value (pm(deg)).
10. The calculated loop filter values are displayed (c1(nF), r2(K), and c2(nF)).
11. (Optional) Set the mode to "freeze" to simulate the phase noise with pre-loaded values, as shown in Figure 8.

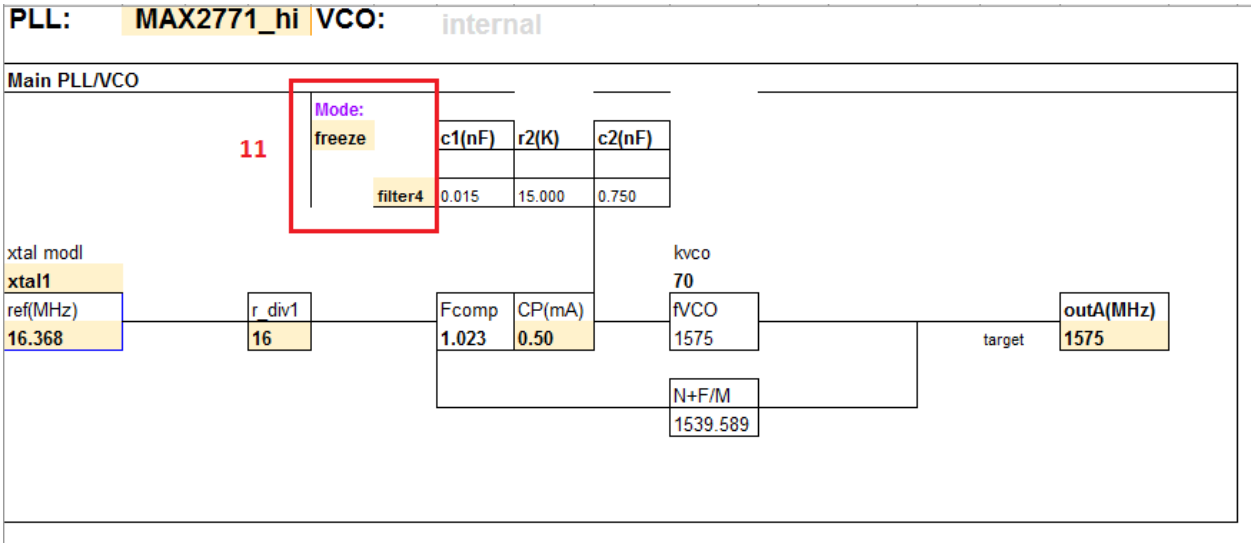

Figure 8. Loop filter spreadsheet freeze mode.

12. As shown in Figure 7, enter the pre-load loop filter values (filter1, filter2, filter3, filter4) and see the phase noise simulation results when the freeze mode is selected.
13. Select between the L1 band VCO (high-band VCO) and the L2/L5 band VCO (low-band VCO). The choices are displayed as MAX2771_hi for high-band and MAX2771_lo for low band.

Based on the parameters and loop filter values calculated, the phase noise is simulated and plotted, as shown in Figure 10.

Checking the Input Value Ranges

The spreadsheet checks that the input values are within their respective legal range. If the cell turns red and the word "oops" appears when inputting a data value, then the value is out-of-range and must be changed.

For example, if a reference clock frequency input is lower than 8MHz, the cell below the value is highlighted in red and the word "oops" appears, as shown in Figure 9.

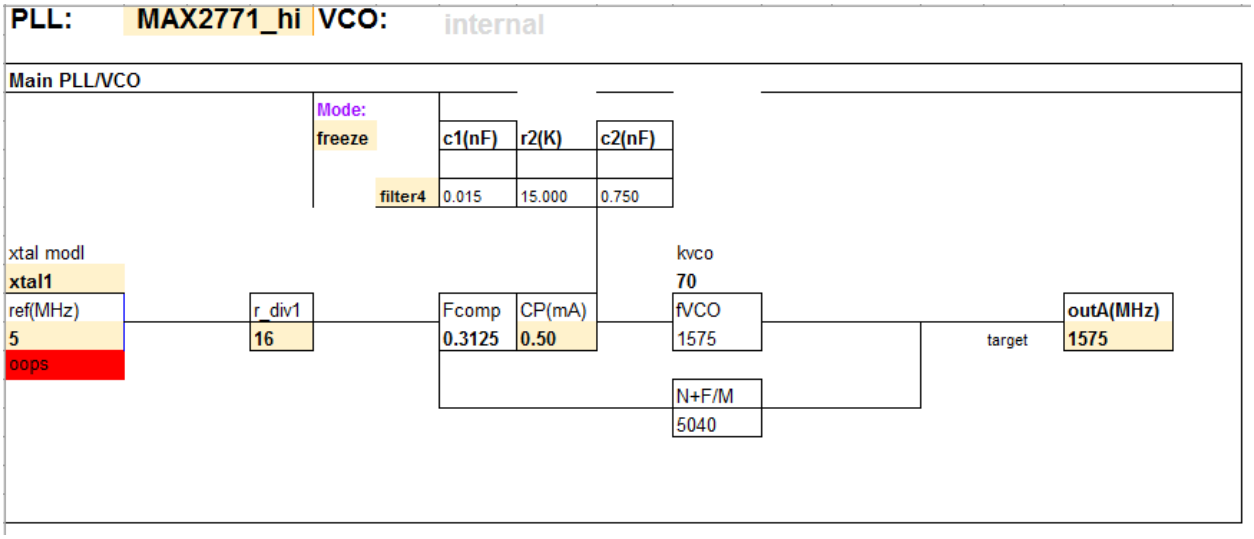

Figure 9. Out-of-range input warning.

Understanding the Simulation Results

Figure 10 shows the calculated simulation results.

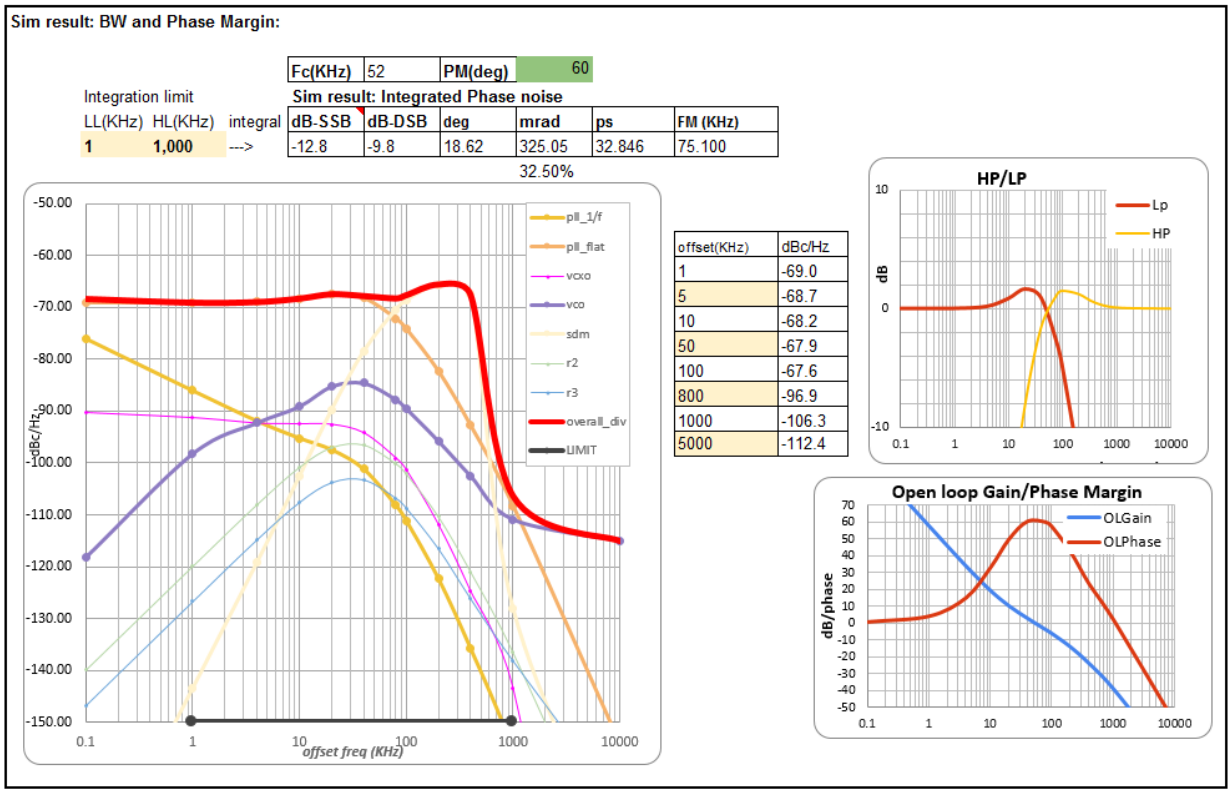

Figure 10. Simulation results.

The following describe the calculated simulation results in Figure 10:

- The achieved loop bandwidth Fc (KHz) and phase margin PM (deg) are displayed.
- Change the integration limits as needed (LL (KHz) and HL (KHz)).
- Based on the integration limits, different parameters such as the SSB phase noise (dB-SSB), DSB phase noise (dB-DSB), phase noise in degrees (deg), mrad, RMS jitter (ps) and frequency modulation (FM (KHz)) are calculated.
- Change the offset frequencies to determine the phase noise at a specific offset frequency.
- The phase noise contribution from different blocks and the total closed-loop phase noise has been plotted. The red curve shows the total phase noise.

  In cases where the PLL is operating in fractional-N mode, the sigma-delta modulator operates and contributes phase noise, as indicated by the light-yellow curve labelled "sdm" in the phase noise plot. If the feedback division ratio is not an integer (i.e., the user-specified VCO output frequency divided by the PFD comparison frequency has a non-zero fractional part), the spreadsheet automatically calculates the SDM phase noise and adds it to the plot. If there is no fractional part and the feedback division ratio is an integer value, then the SDM phase noise is omitted.

  For example, if the reference clock frequency is 16.368MHz, the reference divider value is 16 and the VCO output frequency is 1575.42MHz. Then, the feedback division ratio is exactly 1540, and the SDM is disabled.

- The closed loop transfer function is plotted and is shown as the low-pass (Lp) response. The error response is plotted and is shown as the high-pass (Hp) response.
- The open-loop gain and phase margin is plotted.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/18	Initial release	—