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MC21605A6W-FPTLW	2 x 16	5mm Character Height	LCD Module
Specification			
Version: 1		Date: 25/02/2011	
Revision			
1	23/02/2011	First Issue	

Display Features	
Character Count	2 x 16
Appearance	Black on White
Logic Voltage	5V
Interface	Parallel
Font Set	English / Japanese
Display Mode	Transflective
Character Height	5.23mm
LC Type	FSTN
Module Size	84.00 x 44.00 x 13.50 mm
Operating Temperature	-20°C ~ +70°C
Construction	COB
LED Backlight	White

RoHS compliant

Box Quantity	Weight / Display
---	---

* - For full design functionality, please use this specification in conjunction with the SPLC780D specification. (Provided Separately)

Display Accessories	
Part Number	**Description**
MCCMDB-16SIL	LCD Interconnect board, can be driven from either a PC or a single Board computer with a USB output.
MCCBL1A16SLIP -16DILS-150	16 Way, Sinlge in-line to Dual In-line connector Cable.
MCCBL1A16SLIP -16SILS-150	16 Way, Single in-line to Single In-line connector Cable.

Optional Variants		
Fonts	**Appearances**	**Voltage**

GENERAL SPECIFICATIONS

ITEM	NOMINAL DIMENSIONS / AVAILABLE OPTIONS
DISPLAY FORMAT	16 Characters by 2 Lines
LCD PANEL OPTIONS	FSTN (Silver-gray color)
POLARIZER OPTIONS	Positive, Transflective
BACKLIGHT OPTIONS	Edge type LED backlight (White color)
VIEWING ANGLE OPTIONS	6:00 (Bottom)
TEMPERATURE RANGE OPTIONS	Wide temp. range (-20°C ~ 70°C)
CONTROLLER IC	SUNPLUS
DISPLAY DUTY	1/16
DRIVING BIAS	1/5

MECHANICAL SPECIFICATIONS

OVERALL SIZE	LED backlight version : 84.0 x 44.0 x max 13.5				mm
VIEWING AREA	64.5W x 16.4H	mm	HOLE-HOLE	79/76W x 36.0H	mm
CHARACTER SIZE	3.00W x 5.23H	mm	CHARACTER PITCH	0.51W x 0.52H	mm
DOT SIZE	0.56W x 0.61H	mm	DOT PITCH	0.05W x 0.05H	mm

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT
POWER SUPPLY (LOGIC)	Vdd	25°C	-0.3	7.0	V
POWER SUPPLY (LCD)	V0	25°C	Vdd -13.5	Vdd +0.3	V
INPUT VOLTAGE	Vin	25°C	-0.3	Vdd +0.3	V
OPERATING TEMPERATURE	Vopr	–––	-20	70	°C
STORAGE TEMPERATURE	Vstg	–––	-30	80	°C

ELECTRONICAL CHARACTERISTIC*

ITEM	SYMBOL	CONDITION	STANDARD			UNIT
			MIN	TYP	MAX	
Input voltage	Vdd	+5V	4.7	5.0	5.5	V
Supply current	Idd	Vdd=5V	–––	1.5	–––	mA
Recommended LCD driving voltage for normal temp. Version module	Vdd - V0	-20°C	4.35	–––	4.85	V
		0°C	4.25	–––	4.75	
		25°C	4.20	4.50	4.70	
		50°C	4.10	–––	4.60	
		70°C	3.95	–––	4.50	
LED forward voltage	Vf	25°C	2.9	–––	3.4	V
LED forward current	If	25°C	–––	15	20	mA
LED reverse Current	Ir	25°C	–––	10	–––	μA
LED color range	X coordinate	25°C If = 15mA	0.25	–––	0.28	–––
	Y coordinate	25°C If = 15mA	0.26	–––	0.29	–––
LED illuminance (Without LCD)	Lv	25°C If = 15mA	200	–––	300	cd/m^2
LED life time	–––	25°C If = 15mA	50K**	–––	–––	Hours

*** The above data are for reference only.**

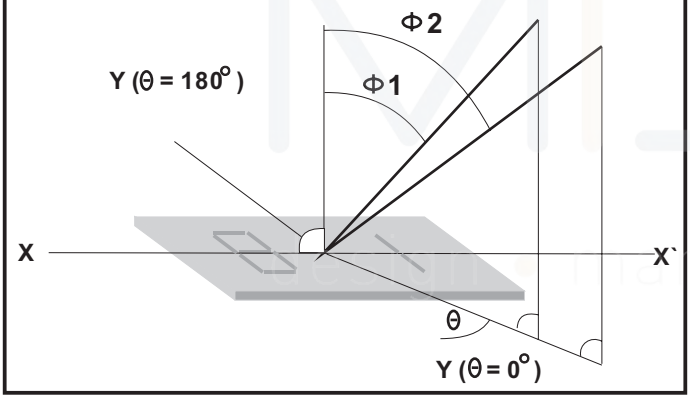
**** If you wanted to drive the LED BKL uninterruptedly exceed 12hours/day, you are not suggested this version**

OPTICAL CHARACTERISTIC

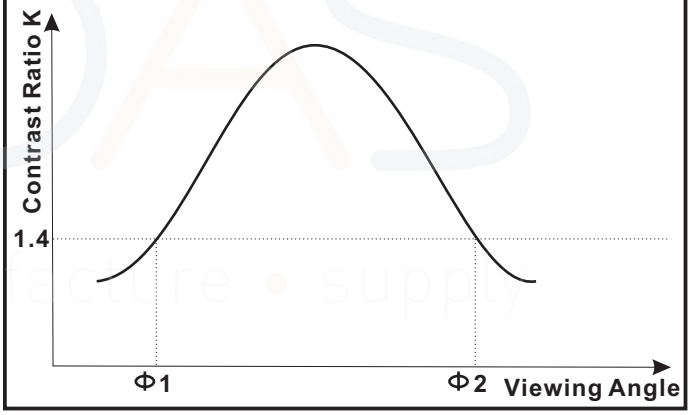
FOR TN TYPE LCD MODULE (T_A=25°C, Vdd=5.0V ± 0.25V)						
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
VIEWING ANGLE	**Φ2 – Φ1**	**K=4**	**30**	---	---	**deg**
	θ		**25**			
CONTRAST RATIO	**K**	---	---	**2**	---	---
RESPONSE TIME(RISE)	**T_R**	---	---	**120**	**150**	**ms**
RESPONSE TIME(FALL)	**T_F**	---	---	**120**	**150**	**ms**

FOR STN TYPE LCD MODULE (T_A=25°C, Vdd=5.0V ± 0.25V)						
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
VIEWING ANGLE	**Φ2 – Φ1**	**K=4**	**40**	---	---	**deg**
	θ		**60**			
CONTRAST RATIO	**K**	---	---	**6**	---	---
RESPONSE TIME(RISE)	**T_R**	---	---	**150**	**250**	**ms**
RESPONSE TIME(FALL)	**T_F**	---	---	**150**	**250**	**ms**

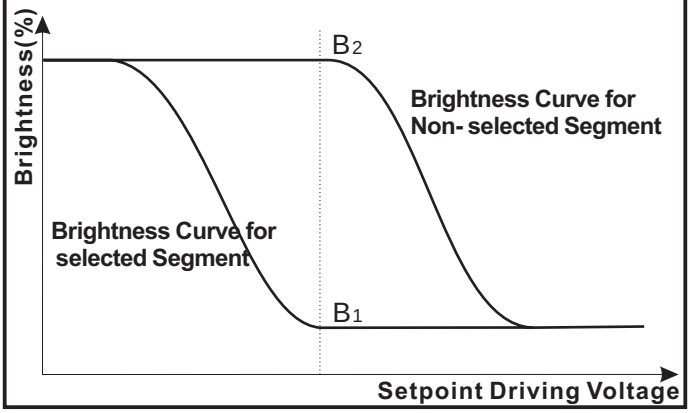
DEFINITION OF ANGLE Φ & θ



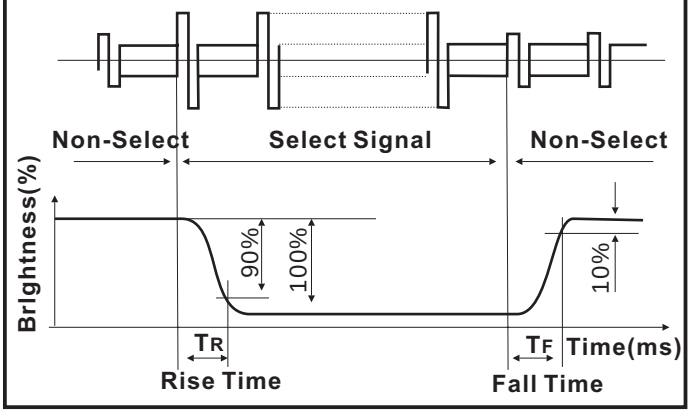
DEFINITION OF VIEWING ANGLE Φ1 & Φ2



DEFINITION OF CONTRAST RATIO K(=B_2/B_1)



DEFINITION OF OPTICAL RESPONSE TIME T_R & T_F



ELECTRICAL SPECIFICATIONS

1. DC CHARACTERISTICS (VDD = 4.5V to 5.5V, TA = 25 ℃)

CHARACTERISTICS	SYMBOL	LIMIT			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
INPUT HIGH VOLTAGE	V_{IH1}	2.2	---	Vdd	V	Pins (E. RS. R/W. DB0 - DB7)
INPUT LOW VOLTAGE	V_{IL1}	-0.3	---	0.6	V	
INPUT HIGH CURRENT	I_{IH}	-2.0	---	2.0	μA	Pins (RS. R/W. DB0 - DB7) Vdd = 5.0V
INPUT LOW CURRENT	I_{IL}	-20	-50	-100	μA	
OUTPUT HIGH VOLTAGE (TTL)	V_{OH1}	2.4	---	Vdd	V	I_{OH} = - 0.1mA Pins: DB0 - DB7
OUTPUT LOW VOLTAGE (TTL)	V_{OL1}	---	---	0.4	V	I_{OL} = 0.1mA Pins: DB0 - DB7

2. AC CHARACTERISTICS (VDD = 4.5V to 5.5V, TA = 25 ℃)

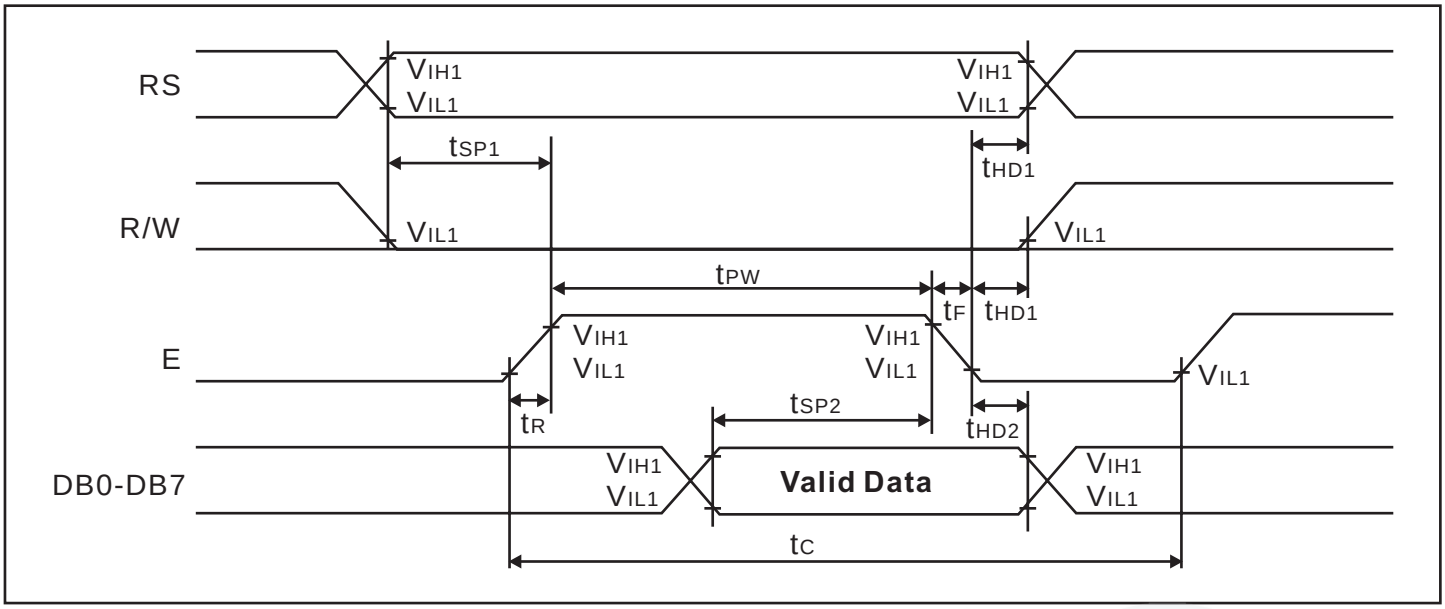
Write mode

CHARACTERISTICS	SYMBOL	LIMIT			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
ENABLE CYCLE TIME	t_C	500	---	---	ns	Pin E
ENABLE PULSE WIDTH	t_{PW}	230	---	---	ns	Pin E
ENABLE RISE/ FALL TIME	t_R, t_F	---	---	20	ns	Pin E
ADDRESS SETUP TIME	t_{SP1}	40	---	---	ns	Pins RS, R/W, E
ADDRESS HOLD TIME	t_{HD1}	10	---	---	ns	Pins RS, R/W, E
DATA SETUP TIME	t_{SP2}	80	---	---	ns	Pins: DB0 - DB7
DATA HOLD TIME	t_{HD2}	10	---	---	ns	Pins: DB0 - DB7

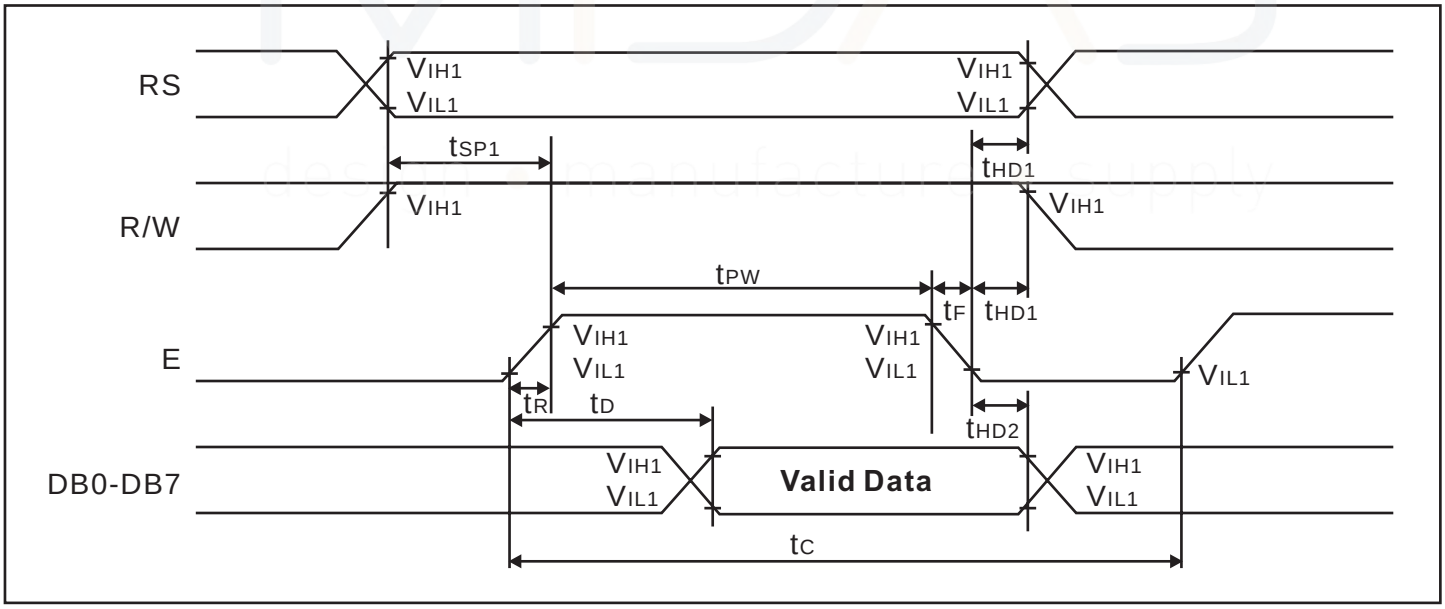
Read mode

CHARACTERISTICS	SYMBOL	LIMIT			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
ENABLE CYCLE TIME	t_C	500	---	---	ns	Pin E
ENABLE PULSE WIDTH	t_{PW}	230	---	---	ns	Pin E
ENABLE RISE/ FALL TIME	t_R, t_F	---	---	20	ns	Pin E
ADDRESS SETUP TIME	t_{SP1}	40	---	---	ns	Pins RS, R/W, E
ADDRESS HOLD TIME	t_{HD1}	10	---	---	ns	Pins RS, R/W, E
DATA OUTPUT DELAY TIME	t_D	---	---	120	ns	Pins: DB0 - DB7
DATA HOLD TIME	t_{HD2}	5	---	---	ns	Pins: DB0 - DB7

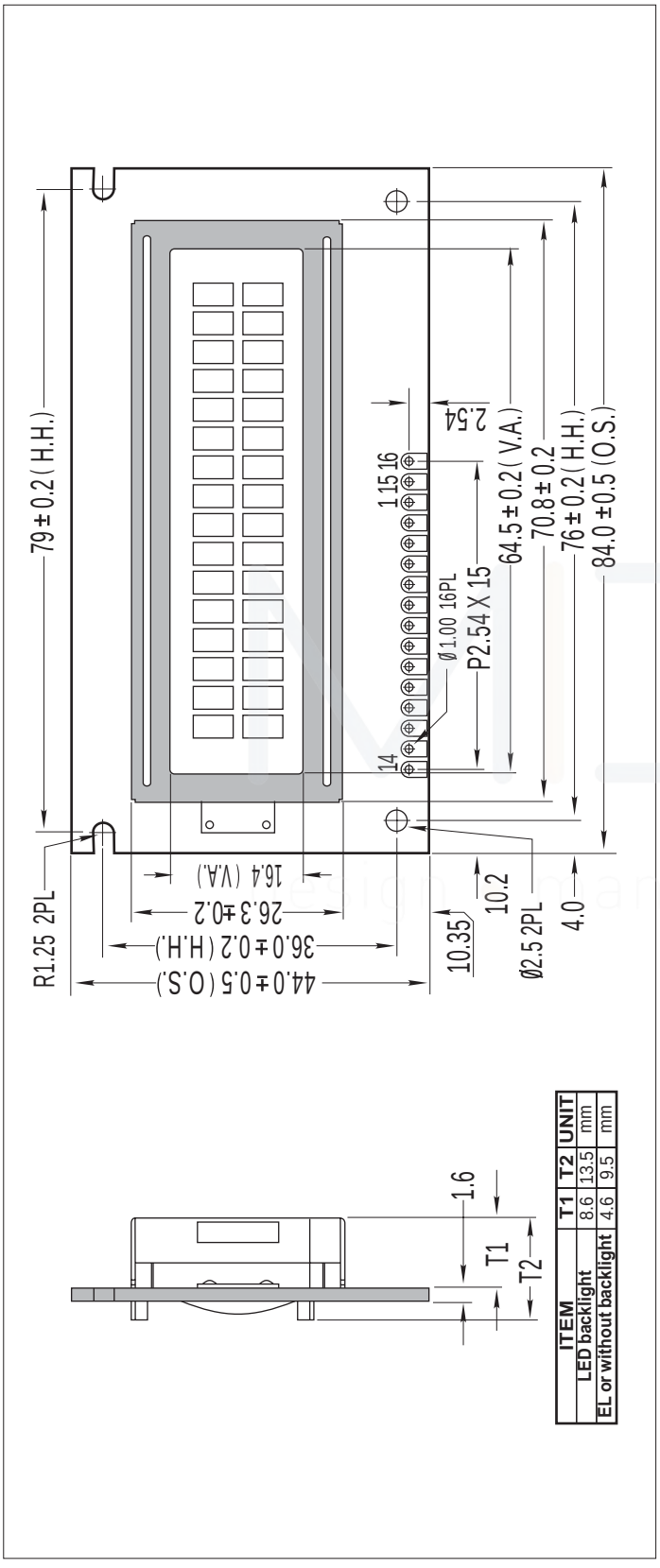
3.1 WRITE MODE TIMING DIAGRAM

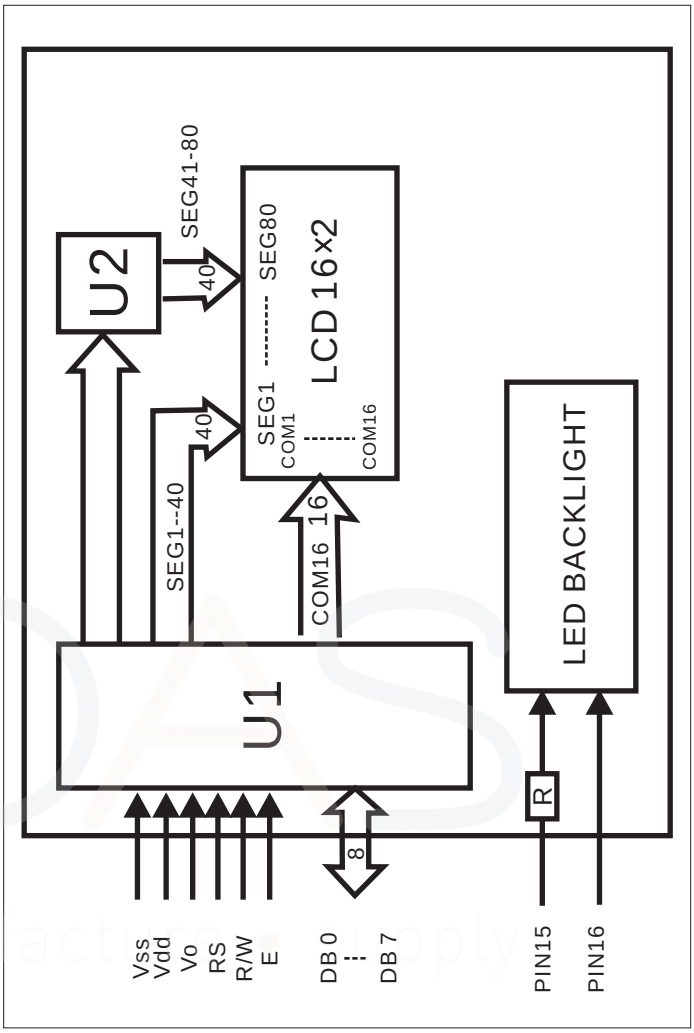


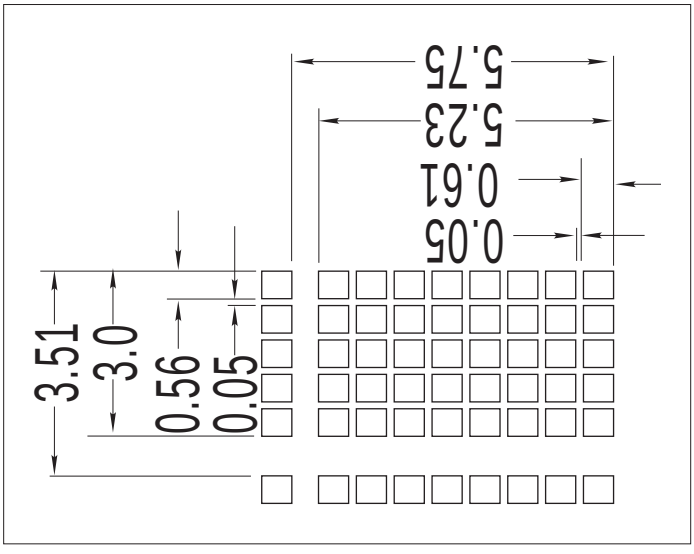
3.2 READ MODE TIMING DIAGRAM



EXTERNAL DIMENSIONS



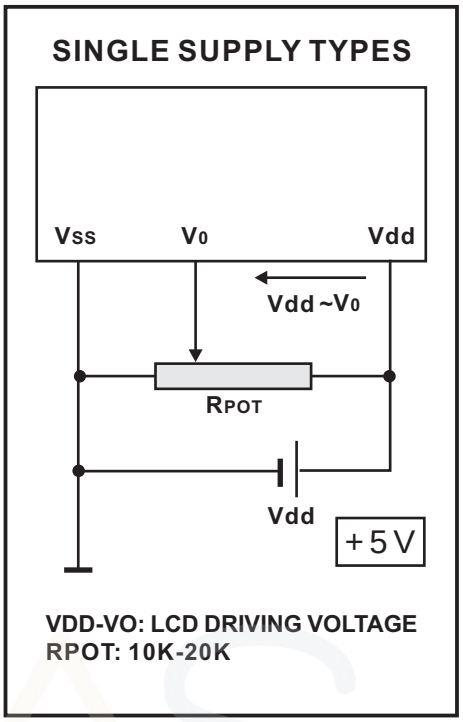




PIN ASSIGNMENT

PIN	SYMBOL	FUNCTION
1	Vss	GND
2	Vdd	Power supply for LCM (+5.0V)
3	V0	Contrast Adjust
4	RS	Register Select Signal
5	R/W	Data Read / Write
6	E	Enable Signal
7-14	DB0 - DB7	Data bus line
15	LED+	Power supply for BKL (+5.0V)
16	LED-	Power supply for BKL (0V)

POWER SUPPLY



REFLECTOR OF SCREEN AND DDRAM ADDRESS

Display position	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10
DDRAM address	00	01	02	03	04	05	06	07	08	09
Display position	1-11	1-12	1-13	1-14	1-15	1-16				
DDRAM address	0A	0B	0C	0D	0E	0F	10	11	12	13
Display position										
DDRAM address	14	15	16	17	18	19	1A	1B	1C	1D
Display position										
DDRAM address	1E	1F	20	21	22	23	24	25	26	27
Display position	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10
DDRAM address	40	41	42	43	44	45	46	47	48	49
Display position	2-11	2-12	2-13	2-14	2-15	2-16				
DDRAM address	4A	4B	4C	4D	4E	4F	50	51	52	53
Display position										
DDRAM address	54	55	56	57	58	59	5A	5B	5C	5D
Display position										
DDRAM address	5E	5F	60	61	62	63	64	65	66	67

1-1 means first character of line 1 on screen

INSTRUCTION TABLE

Instruction	Instruction Code										Description	Execution Time(fosc= 270kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write 20H to DDRAM set DDRAM address to 00H from AC	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to 00H from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display	38μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D) cursor(C) and blinking of cursor(B) on/off	38μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data	38μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length(DL:8bit/4bit), number of display line (N:2line/1line) and,display font type F:5X11dots / 5X8dots	38μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	38μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	38μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF The contents of address counter can also be read	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	38μs
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	38μs

INSTRUCTION DESCRIPTION

A. Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing 20H (space code) to all DDRAM address, and set DDRAM address to 00H into AC (address counter).
Return cursor to the original status, namely, bring the cursor to the left edge on the first line of the display.
Make the entry mode increment (I/D = HIGH)

B. Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Set DDRAM address to 00H into the address counter.
Return cursor to its original site and return display to its original status,if shifted.
Contents of DDRAM does not change.

C. Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.
I/D:Increment /decrement of DDRAM address(cursor or blink)
I/D=High,cursor/blink moves to right and DDRAM address is increased by 1.
I/D=low,cursor/blink moves to left and DDRAM address is decreased by 1.
*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.
SH:Shift of entire display
When DDRAM read (CGRAM read/write) operation or SH=Low,shifting of entire display is not performed.if SH=High, and DDRAM write operation,shift of entire display is performed according to I/D value(I/D=High,shift left, I/D=Low, shift right).

D. Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

D:Display ON/OFF control bit
When D=High, entire display is turned on.
When D=Low, display is turned off, but display data remains in DDRAM.
C:Cursor ON/OFF control bit
When C=High, cursor is turned on.
When C=Low, cursor is disappeared in current display ,but I/D register preserves its data.
B:Cursor Blink ON/OFF control bit
When B=High, cursor blink is on, which performs alternately between all the High data and display characters at the cursor position.
When B=Low ,blink is off.

E. Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.
During 2-line mode display, cursor moves to the 2ndline after the 40thdigit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When displayed data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left,cursor moves according to the display
1	1	Shift all the display to the right,cursor moves according to the display

F. Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL:Interface data length control bit
When DL=High, it means 8-bit bus mode with MPU.
When DL=Low, it means 4-bit bus mode with MPU.
When 4-bit bus mode, it needs to transfer 4-bit data twice.
N:Display line number control bit
When N=Low, 1-line display mode is set.
When N=High, 2-line display mode is set.
F:Display font type control bit
When F=Low, 5x8 dots format display mode is set.
When F=High, 5x11 dots format display mode.

G. Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

H. Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N=Low), DDRAM address is from 00H to 4FH
In 2-line display mode(N=High),DDRAM address in the 1st line is from 00H to 27H and DDRAM address in the 2nd line is from 40H to 67H

I. Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether IC is in internal operation or not .
If BF is High, internal operation is in progress and shall wait until BF is to be Low, which by then the next instruction can be performed. In this instruction you and also read the value of the address counter.

J. Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM,and CGRAM,is set by the previous address set instruction(DDRAM address set,CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased /decreased by 1,according the entry mode.

K. Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction.If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before read operation,the correct RAM data can be obtained from the second. But the first data would be incorrect,as there is no time margin to transfer RAM data.

In case of DDRAM read operation,cursor shift instruction plays the same role as DDRAM address set instruction,it also transfers RAM data to output data register.

After read operation,address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation,display shift may not be executed correctly.

Note:In case of RAM write operation,AC is increased/decreased by 1 as in read operation. At this time,AC indicates the next address position, but only the previous data can be read by the read instruction.

RELATIONSHIP BETWEEN CHARACTER CODE AND CGRAM

Character code								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0	1	1	1	0	pattern 1
											0	0	1	x	x	x	1	0	0	0	1	
											0	1	0	x	x	x	1	0	0	0	1	
											0	1	1	x	x	x	1	1	1	1	1	
											1	0	0	x	x	x	1	0	0	0	1	
											1	0	1	x	x	x	1	0	0	0	1	
											1	1	0	x	x	x	1	0	0	0	1	
											1	1	1	x	x	x	0	0	0	0	0	
0	0	0	0	x	1	1	1	0	0	0	0	0	0	x	x	x	1	0	0	0	1	pattern8
											0	0	1	x	x	x	1	0	0	0	1	
											0	1	0	x	x	x	1	0	0	0	1	
											0	1	1	x	x	x	1	1	1	1	1	
											1	0	0	x	x	x	1	0	0	0	1	
											1	0	1	x	x	x	1	0	0	0	1	
											1	1	0	x	x	x	1	0	0	0	1	
											1	1	1	x	x	x	0	0	0	0	0	

DISPLAY DATA RAM(DDRAM)

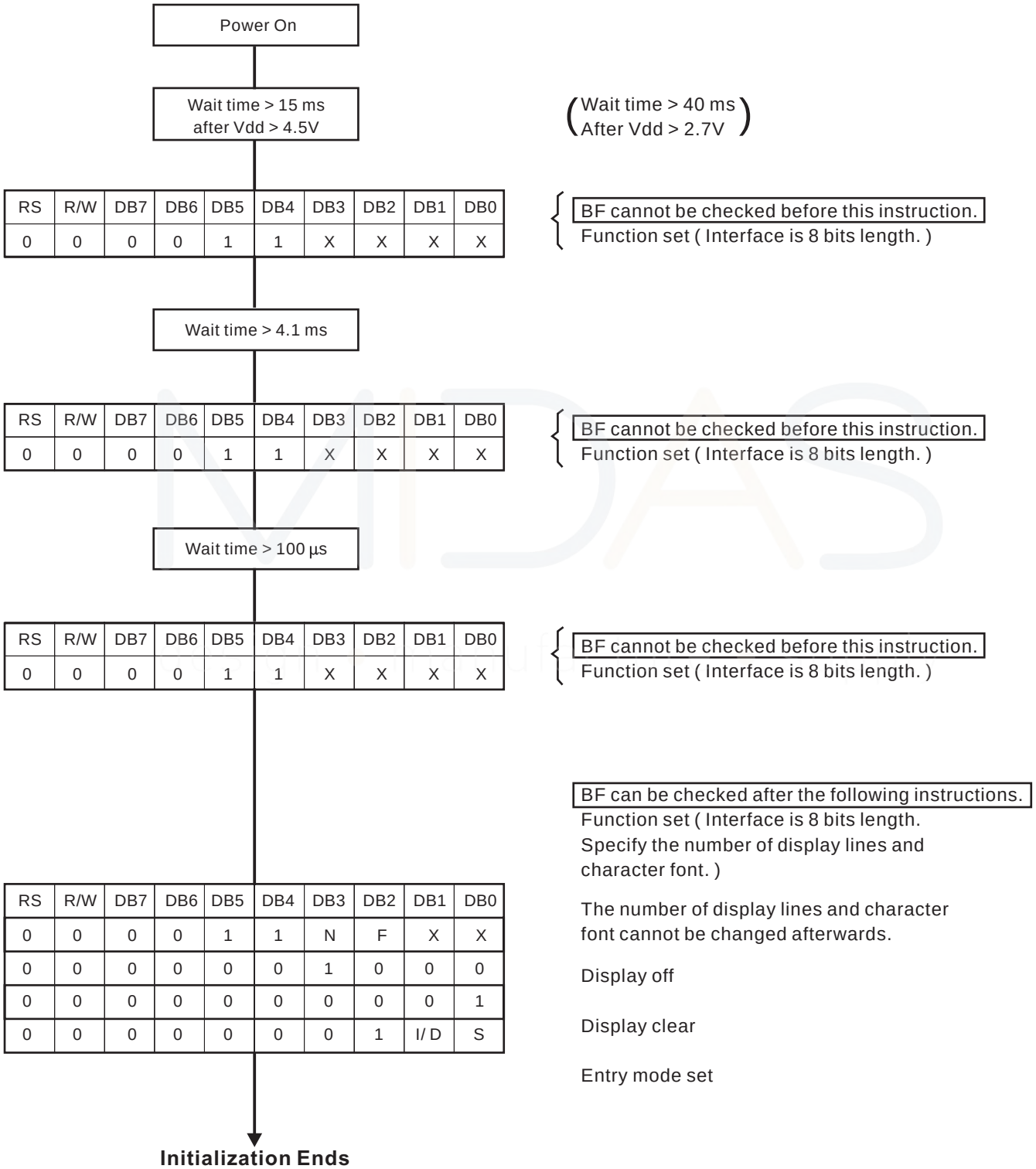
DDRAM stores display data of maximum 80x8 bits(80 characters).

DDRAM address is set in the address counter(AC) as a hexadecimal number

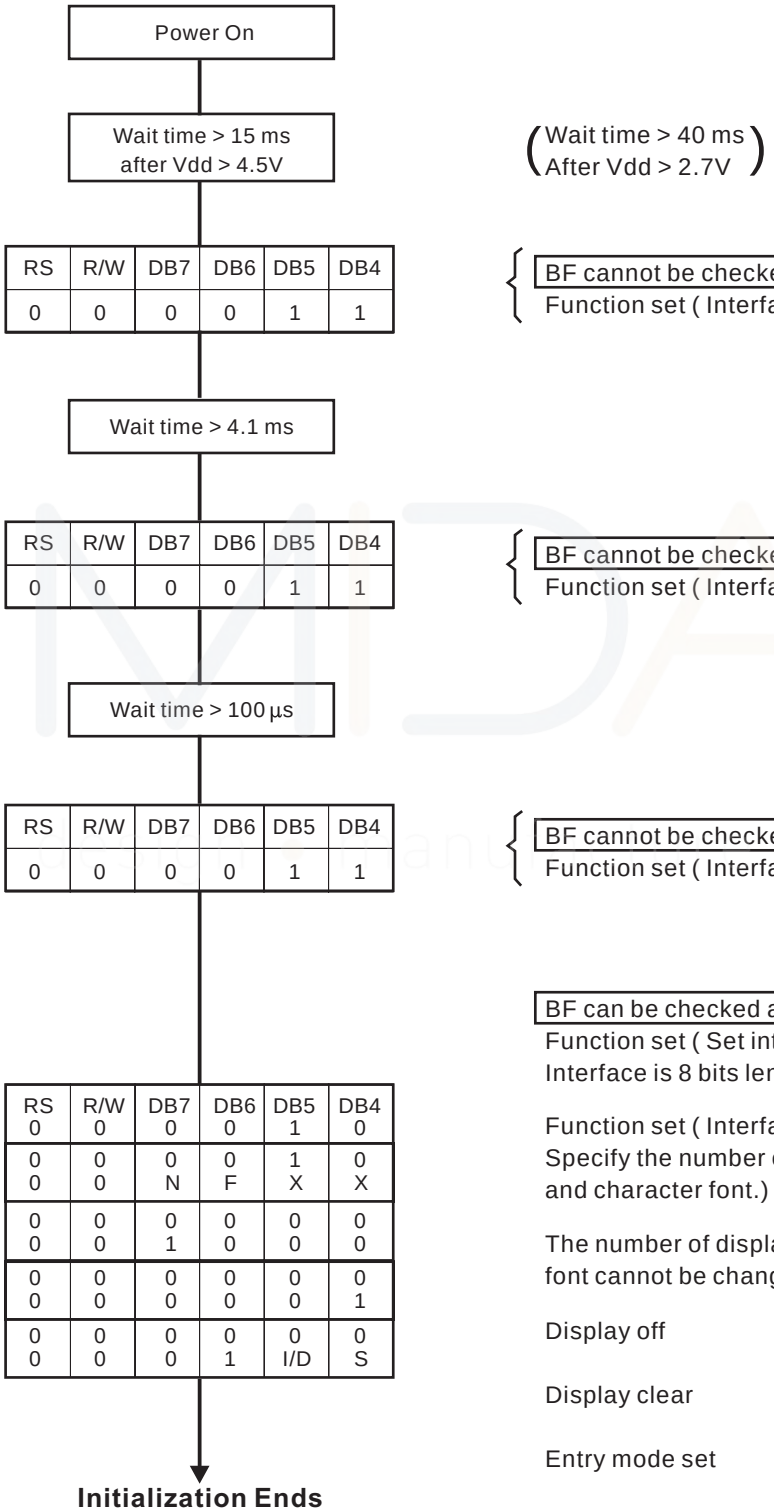
MSB						LSB
AC6	AC5	AC4	AC3	AC2	AC1	AC0

INITIALIZATION

1. 8-bit interface mode (Condition: fosc = 270KHZ)

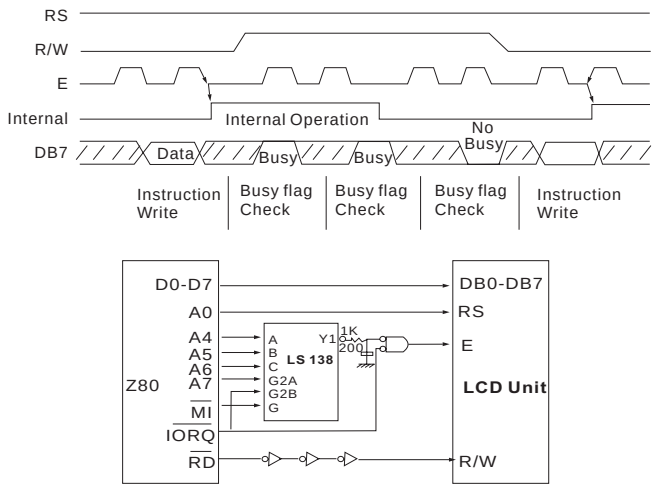


2. 4-bit interface mode (Condition: fosc = 270KHZ)



INTERFACE TO MPU

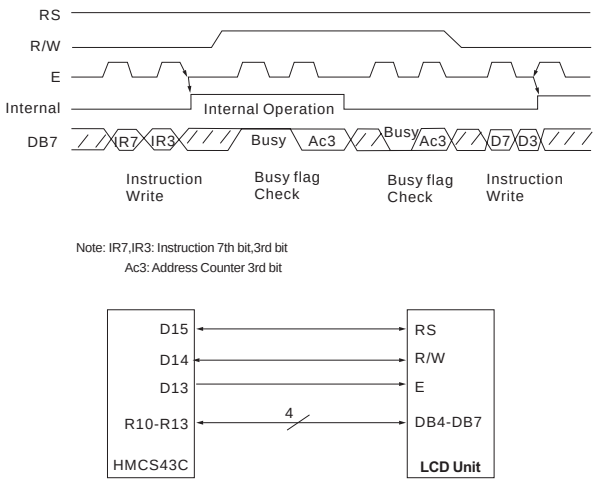
INTERFACE TO 8-BIT MPU



If Interface Data Is 8-bits Long

Data transfer is made through all 8 bus lines from DB0 to DB7

INTERFACE TO 4-BIT MPU



If Interface Data Is 4-bit Long

Data transfer is accomplished through 4 bus lines from DB4 to DB7.(while the rest of 4 bus lines from DB0 toDB3 are not used.)
Data transfer is completed when 4-bits of data is transferred twice.(upper 4-bits of data, then lower 4-bits of data.)

Features

1. **Interface to an 8-bit or 4-bit MPU is available.**
2. **192 types of alphanumeric, symbols and special characters can be displayed with the built - in character generator (ROM).**
3. **Other preferred characters can be displayed by character generator (RAM).**
4. **Various instructions may be programmed.**
   - **Clear display**
   - **Cursor at home**
   - **On/Off cursor**
   - **Blink character**
   - **Shift display**
   - **Shift cursor**
   - **Read/Write display data .etc.**
5. **Compact and light weight design which can easily be integrated into end products.**
6. **Single power supply +5V drive (except for extended temperature type).**
7. **Low power consumption.**

STANDARD FONT MAP

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															