ISL59834

Quad Channel, Single Supply, Video Reconstruction Filter with On-Board Charge Pump

FN6268
Rev 1.00
June 11, 2008

The ISL59834 is a quad channel, single supply, video reconstruction filter with integrated charge pump. It is designed to operate on a single supply (3.0V to 3.6V) and generate its own negative supply (-1.5V) using a regulated charge pump. Input signals to the ISL59834 can be AC- or DC-coupled. When AC-coupled, the backporch clamp sets the blank level to ground at the output. Channels 1 and 3 have a sync detector whose output is available at SYNC_OUTA and SYNC_OUTB, respectively. SYNC_INA and SYNC_INB are inputs that provide timing for Channel 2 and Channel 4, respectively. Channel 2 and Channel 4 have keyed clamps, which set the outputs to ground when SYNC_INA or SYNC_INB are driven to the logic high state. Each of the four outputs are capable of driving two DC or AC-coupled standard video loads. The ISL59834 features a 4th order Butterworth reconstruction filter that provides a 9MHz nominal -3dB frequency and 40dB of attenuation at 27MHz. Nominal operational current is 63mA. When powered down, the device draws 5µA maximum supply current. The ISL59834 is available in a 44 Ld 7x7 QFN package.

Ordering Information

PART NUMBER (NOTE)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59834IRZ	59 834IRZ	-40 to +85	44 Ld QFN	L44.7x7A

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

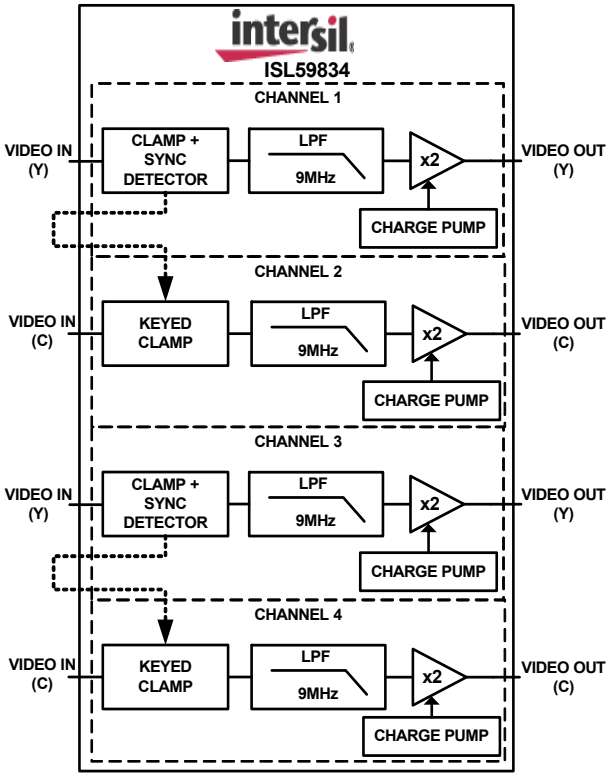
Features

- 3.3V Nominal Supply, Operates Down to 3.0V
- DC-Coupled Outputs
- Inputs can be AC- or DC-Coupled
- Eliminates the Need for Large Output Coupling Capacitor
- Integrated Sync Tip Clamp sets the Backporch to Ground at the Output for Channels 1 and 3
- Integrated Keyed Clamp puts Channel 2 and Channel 4 Outputs to Ground During Sync
- Each Output Drives 2 Standard Video Loads
- Response Flat to 5MHz with 40dB Attenuation at 27MHz
- Pb-Free (RoHS compliant)

Applications

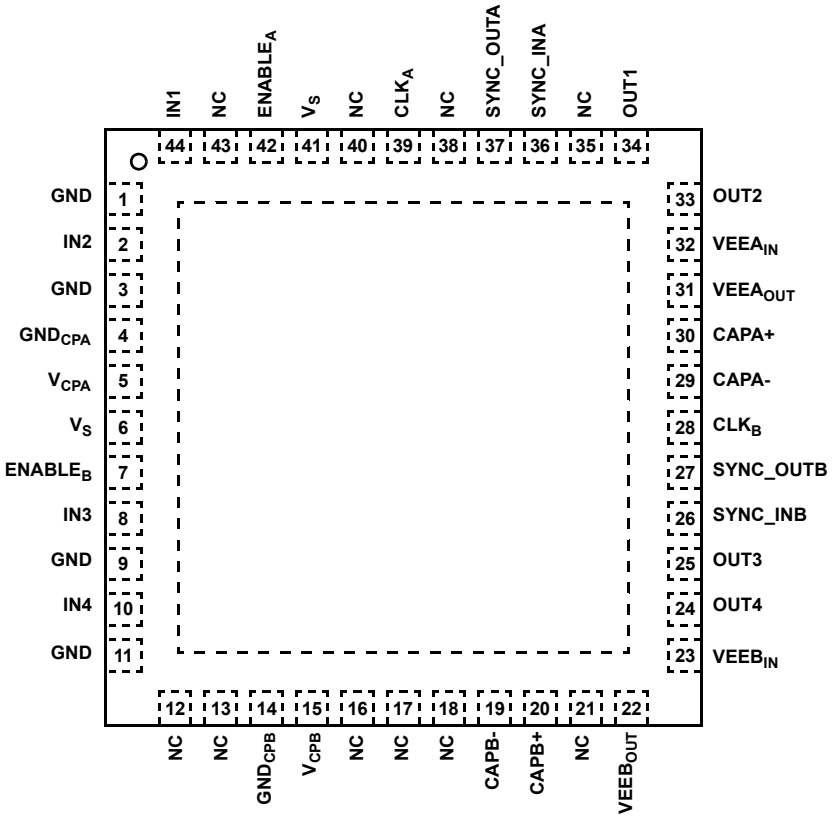
- Set-Top Box Receiver
- Television
- DVD Player
- Digital Camera
- Cell Phone

Block Diagram



Pinout

ISL59834
(44 LD QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

V_S to GND 4V
V_{IN} to GND. . . . . GND - 0.3V to V_S + 0.3V
Maximum Continuous Output Current . . . . . ±50mA
Maximum Current into Any Pin . . . . . ±50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . .3500V
Machine Model (Per EIAJ ED-4701 Method C-111). 350V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
44 Lead QFN	32

Maximum Junction Temperature (Plastic Package) . . . . . .+150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

Electrical Specifications

$V_{CP} = V_S = 3.3V$, $C_{F1} = C_{F2} = 0.1\mu F$, $C_{S1} = C_{S2} = 0.22\mu F$, $C_{FIL1} = C_{FIL2} = 0.4\mu F$, $C_{IN1} = C_{IN2} = C_{IN3} = C_{IN4} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$, Typical T_A = +27°C.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
DC CHARACTERISTICS						
V_S, V_{CP}	Supply Range	Guaranteed by PSRR	3.0	3.3	3.6	V
VEE_{OUT}	Charge Pump Output	Measured at VEE_{IN}	-1.75	-1.5	-1.25	V
I_S	Supply Current	No load		28	32	mA
I_{CP}	Charge Pump Supply Current	No load		35	40	mA
I_{PD}	Power-down Current	ENABLE = 0.4V		0.6	5	µA
I_{IN}	Input Pull-down Current	Channels 1 and 3, V_{IN} = 0.5V	0.4	4	10	µA
I_B	Input Bias Current	Channels 2 and 4, V_{IN} = 0.5V, SYNC_IN = 0V	-10	-3	10	µA
A_V	DC Gain		1.94	2	2.05	V/V
V_{IN_MAX}	Max DC Input Range	DC-coupled input, guaranteed by DC gain test	1.4			V
$V_{CLAMPOUT1}$	Output Sync Tip Clamp Level (Channels 1 and 3)	$V_{IN} \leq 0$, AC-coupled input	-650	-590	-525	mV
$V_{CLAMPOUT2}$	Keyed Clamp Level (Channels 2 and 4)	Output level when SYNC_IN ≥ 2.0V	-60	-25	0	mV
$V_{CLAMPIN1}$	Input Clamp Level (Channels 1 and 3)	Input floating	0	30	70	mV
$V_{CLAMPIN2}$	Input Keyed Clamp Level (Channels 2 and 4)	Input floating, input level when SYNC_IN ≥ 2.0V	275	300	375	mV
V_{OS}	Output Level Shift (Channels 1 and 3)	$V_{IN} > 0$, output shifted relative to input, DC-coupled input	-685	-620	-550	mV
	Output Level Shift (Channels 2 and 4)	$V_{IN} > 0$, output shifted relative to input, DC-coupled input	-380	-330	-280	mV
I_{CLAMP}	Clamp Restore Current	Force V_{IN} = -0.3V, Channels 1 and 3		-5	-2.5	mA
		Force V_{IN} = 1V, Channel 2 and 4	135	180		µA
		Force V_{IN} = -0.3V, Channels 2 and 4		-200	-160	µA
V_{SLICE}	Sync Detect Threshold	Channels 1 and 3	100		200	mV
$PSRR_{DC}$	Power Supply Rejection	V_S = +3.0 to +3.6	50	77		dB

Electrical Specifications $V_{CP} = V_S = 3.3V$, $C_{F1} = C_{F2} = 0.1\mu F$, $C_{S1} = C_{S2} = 0.22\mu F$, $C_{FIL1} = C_{FIL2} = 0.4\mu F$, $C_{IN1} = C_{IN2} = C_{IN3} = C_{IN4} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$, Typical $T_A = +27°C$. **(Continued)**

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
AC CHARACTERISTICS						
A_{PB}	Passband Flatness	f = 5MHz relative to 100kHz	0	0.8	1.25	dB
A_{SB}	Stopband Attenuation	f ≥ 27MHz relative to 100kHz		-50	-35	dB
dG	Differential Gain	11-step modulated staircase		0.45		%
dP	Differential Phase	11-step modulated staircase		-0.15		°
SNR	Signal-to-Noise Ratio	Peak signal ($1.4V_{P-P}$) to RMS noise, f = 10kHz to 10MHz		60		dB
GD_{MATCH}	DC Group Delay Match	Channel-to-channel group delay matching at 100kHz		0.1		ns
ΔGD	Group Delay Deviation	Deviation from 100kHz to 3.58MHz		8		ns
PSRR	Power Supply Rejection	$V_{IN} = 100mV_{P-P}$ sine wave, f = 100kHz to 5MHz		25		dB
X_{TALK}	Channel-to-Channel Crosstalk	f = 100kHz to 5MHz, inter-channel		-55		dB
V_{NOISE}	Input Voltage Noise			1.44		mV_{RMS}
LOGIC (ENABLEA, ENABLEB)						
V_{IL}	Logic Low Input Voltage				0.8	V
V_{IH}	Logic High Input Voltage		2.0			V
I_I	Logic Input Current		-1		1	µA
CHARGE PUMP						
f_{CP}	Charge Pump Clock Frequency			9.5		MHz

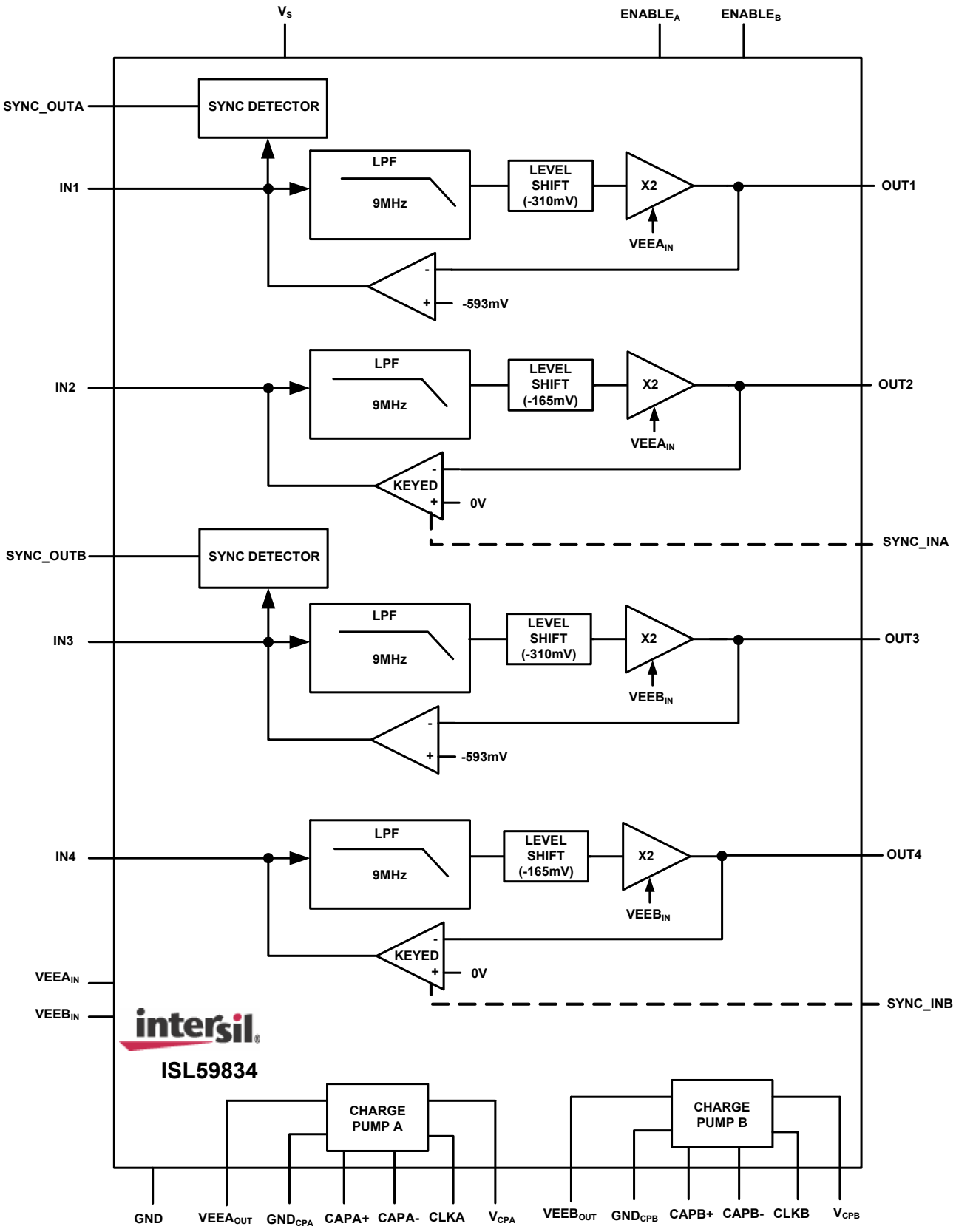
NOTE:

2. Parameters with MIN and/or MAX limits are 100% tested at +27°C, unless otherwise specified. Temperature limits are established by characterization and are not production tested.

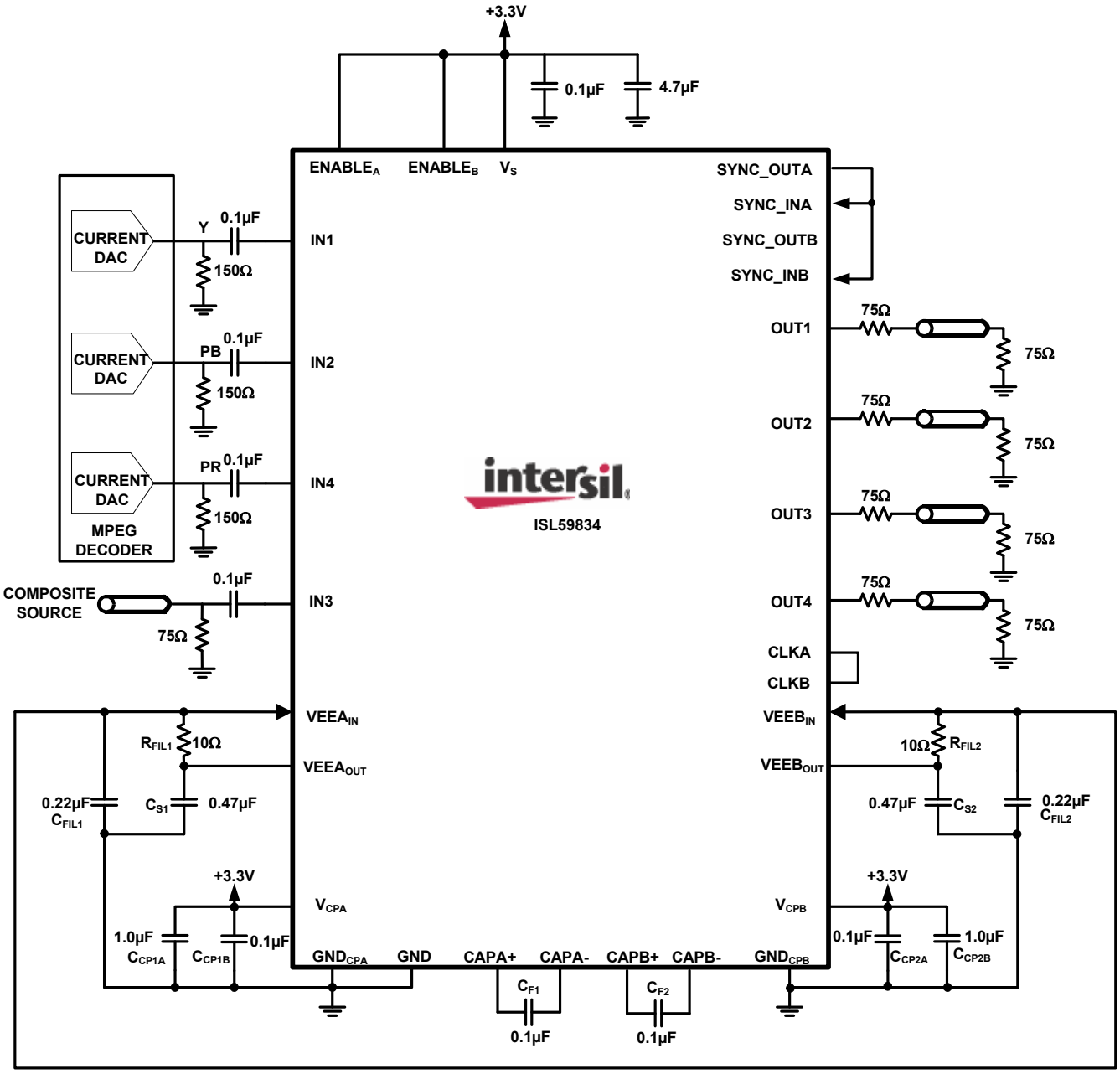
Pin Descriptions

NUMBER	NAME	FUNCTION
1, 3, 9, 11	GND	Ground
2	IN2	Video Input 2. Chroma Channel.
4	GND_{CPA}	Charge Pump A Ground
5	V_{CPA}	Charge Pump A Power Supply. Bypass with a 0.1µF capacitor to $GND_{CPA.}$
6, 41	V_S	Positive Power Supply. Bypass to GND with a 0.1µF capacitor.
7	$ENABLE_B$	Channel 3 and Channel 4 Enable. Connect to V_S to enable channels. **$ENABLE_A$ must be tied to $ENABLE_B$.**
8	IN3	Video Input 3. Luma Channel.
10	IN4	Video Input 4. Chroma Channel.
12, 13, 16, 17, 18, 21, 35, 38, 40, 43	NC	No Connect.
14	GND_{CPB}	Charge Pump B Ground.
15	V_{CPB}	Charge Pump B Power Supply. Bypass with a 0.1µF capacitor to GND_{CPB}.
19	CAPB-	Charge-Pump B Flying Capacitor Negative Terminal. Connect a 0.1µF capacitor from CAPB+ to CAPB-.
20	CAPB+	Charge-Pump B Flying Capacitor Positive Terminal. Connect a 0.1µF capacitor from CAPB+ to CAPB-.
22	$VEEB_{OUT}$	Charge Pump Negative Output. Bypass with a 0.22µF capacitor to GCP2.
23	$VEEB_{IN}$	Negative Supply for Channels 3 and 4. Connect an RC filter between $VEEB_{IN}$ and $VEEB_{OUT}$. See Typical Application Diagram. **$VEEA_{IN}$ must be tied to $VEEB_{IN}$.**
24	OUT4	Video Output 4
25	OUT3	Video Output 3
26	SYNC_INB	Sync Input. Sync logic input for Channel 4.
27	SYNC_OUTB	Sync Output. Sync logic output from Channel 3.
28	CLK_B	Channel 3 and Channel 4 Charge Pump Clock Output. Can also be driven by external clock. **CLK_A must be tied to CLK_B.**
29	CAPA-	Charge-Pump A Flying Capacitor Negative Terminal. Connect a 0.1µF capacitor from CAPA+ to CAPA-.
30	CAPA+	Charge-Pump A Flying Capacitor Positive Terminal. Connect a 0.1µF capacitor from CAPB+ to CAPB-.
31	$VEEA_{OUT}$	Charge Pump Negative Output. Bypass with a 0.22µF capacitor to GND_{CPA}.
32	$VEEA_{IN}$	Negative Supply for Channels 1 and 2. Connect an RC filter between $VEEA_{IN}$ and $VEEA_{OUT}$. See Typical Application Diagram. **$VEEA_{IN}$ must be tied to $VEEB_{IN}$.**
33	OUT2	Video Output 2
34	OUT1	Video Output 1
36	SYNC_INA	Sync Input. Sync logic input for Channel 2.
37	SYNC_OUTA	Sync Output. Sync logic output from Channel 1.
39	CLK_A	Channel 1 and Channel 2 Charge Pump Clock Output. Can also be driven by external clock. **CLK_A must be tied to CLK_B.**
42	$ENABLE_A$	Channel 1 and Channel 2 enable. Connect to V_S to enable channels. **$ENABLE_A$ must be tied to $ENABLE_B$.**
44	IN1	Video Input 1. Luma Channel.
-	EP	Exposed Pad. Connect to $VEEA_{IN}$ or $VEEB_{IN}$.

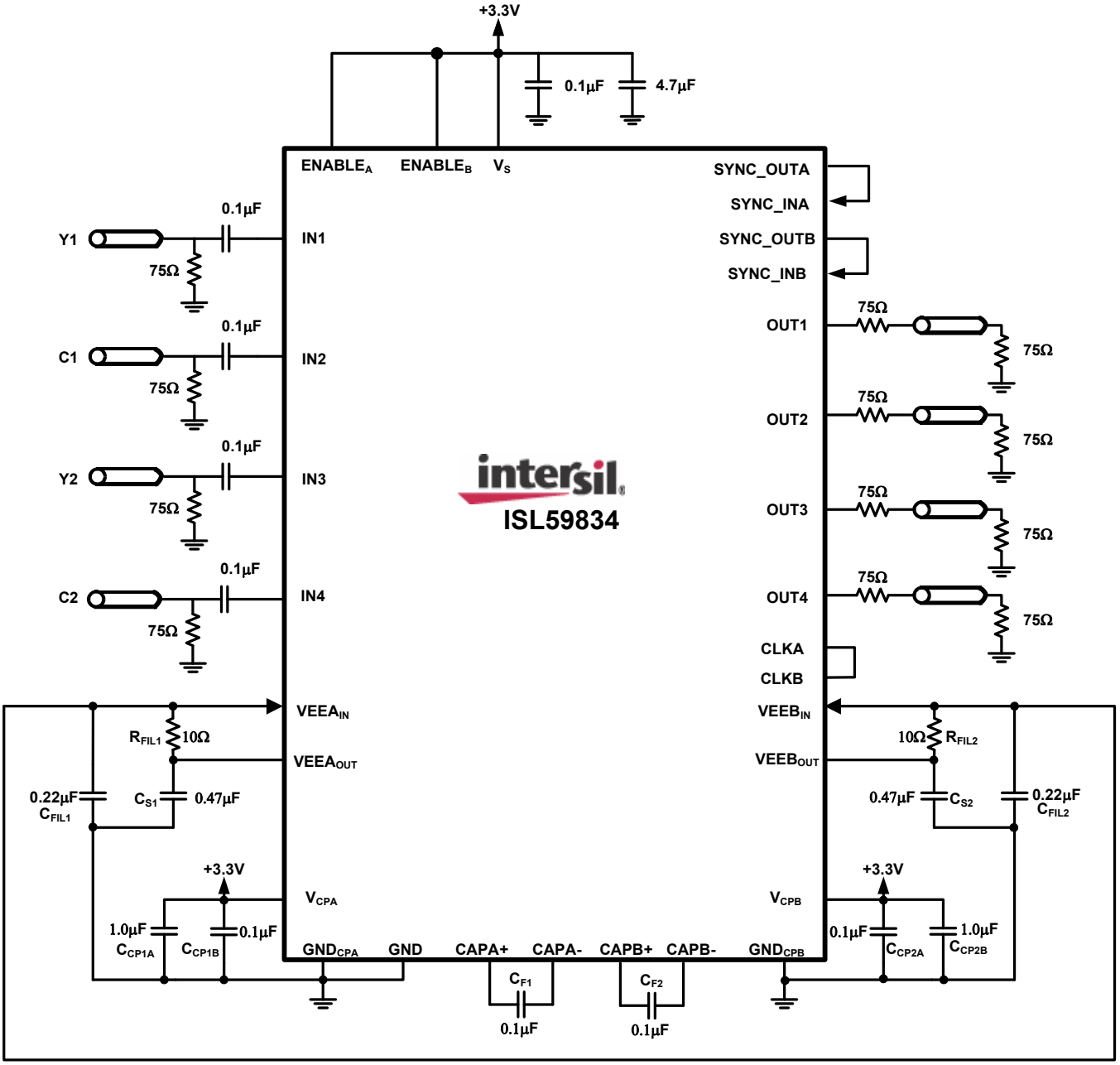
Functional Diagram



Component (YPbPr) Application Diagram



S-Video Application Diagram



Typical Performance Curves

$V_{CP} = V_S = 3.3V$, $C_{F1} = C_{F2} = 0.1\mu F$, $C_{S1} = C_{S2} = 0.22\mu F$, $C_{FIL1} = C_{FIL2} = 0.4\mu F$, $C_{IN1} = C_{IN2} = C_{IN3} = C_{IN4} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$.

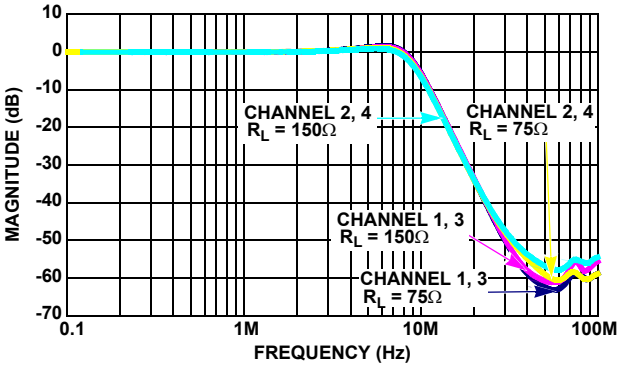


FIGURE 1. BANDWIDTH vs FREQUENCY

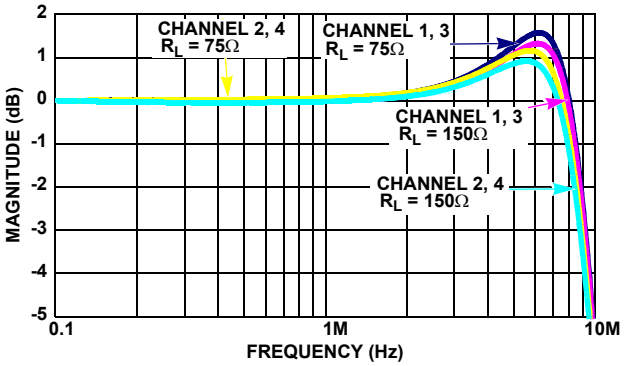


FIGURE 2. GAIN FLATNESS vs FREQUENCY

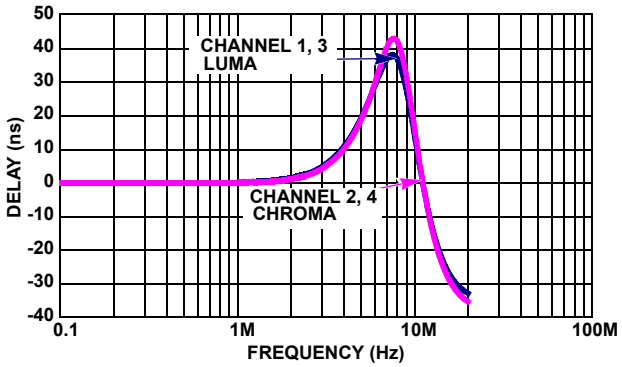


FIGURE 3. GROUP DELAY vs FREQUENCY

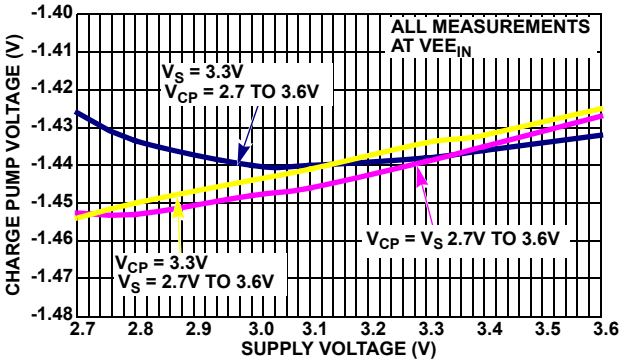


FIGURE 4. CHARGE PUMP VOLTAGE vs SUPPLY VOLTAGE

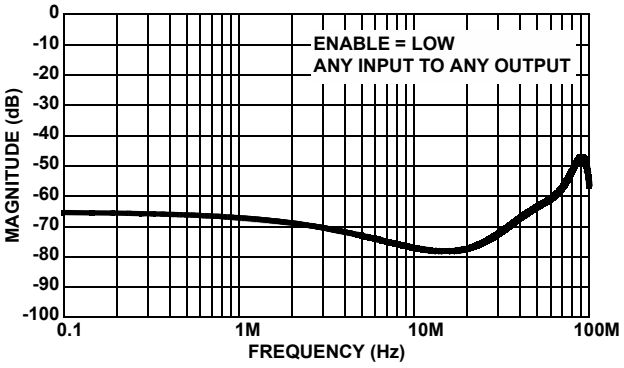


FIGURE 5. INPUT-TO-OUTPUT ISOLATION vs FREQUENCY

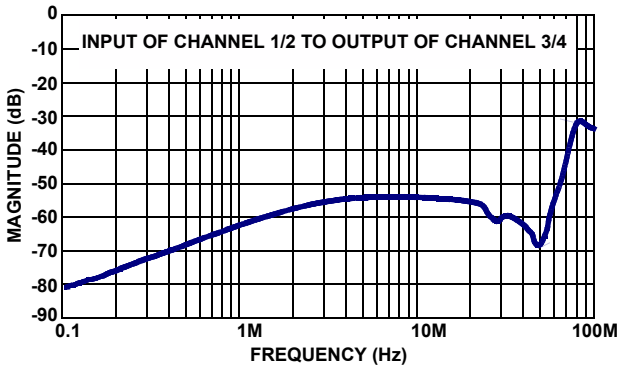


FIGURE 6. INTER-CHANNEL CROSSTALK

Typical Performance Curves

$V_{CP} = V_S = 3.3V$, $C_{F1} = C_{F2} = 0.1\mu F$, $C_{S1} = C_{S2} = 0.22\mu F$, $C_{FIL1} = C_{FIL2} = 0.4\mu F$, $C_{IN1} = C_{IN2} = C_{IN3} = C_{IN4} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$. **(Continued)**

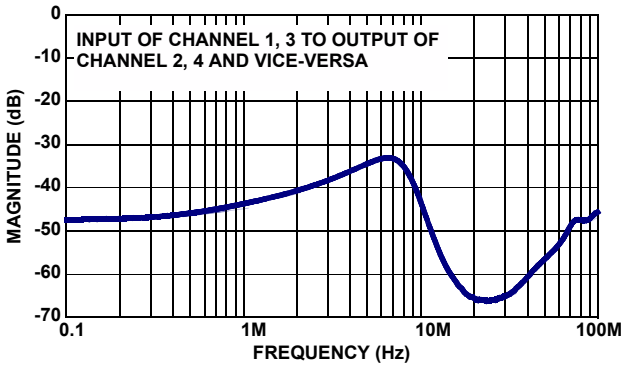


FIGURE 7. LUMA-TO-CHROMA CROSSTALK

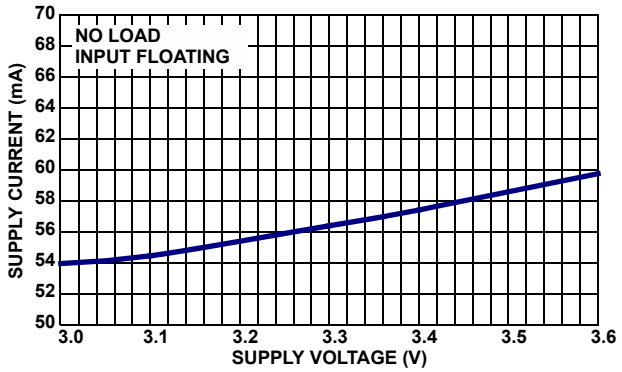


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE

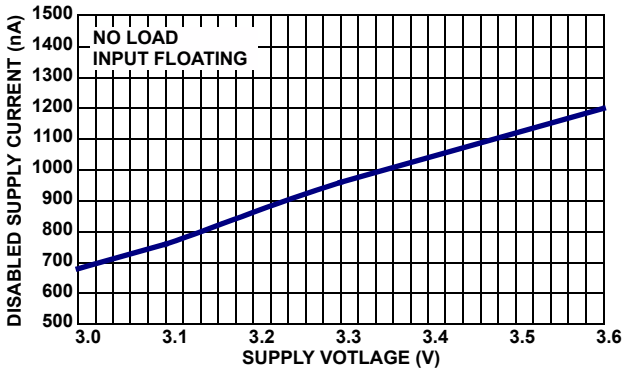


FIGURE 9. DISABLED SUPPLY CURRENT vs SUPPLY VOLTAGE

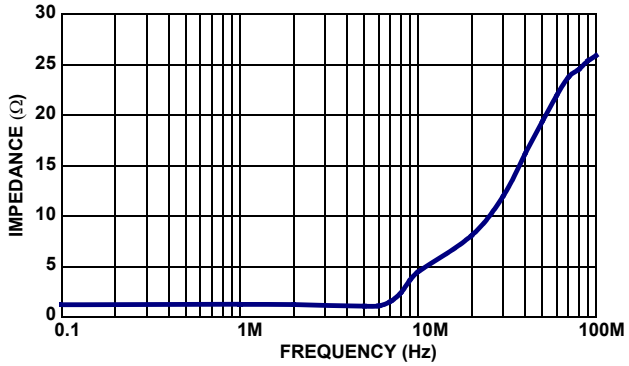


FIGURE 10. OUTPUT IMPEDANCE vs FREQUENCY

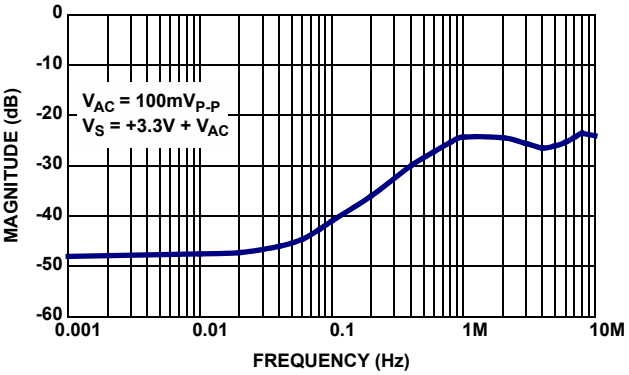


FIGURE 11. POWER SUPPLY REJECTION RATIO vs FREQUENCY

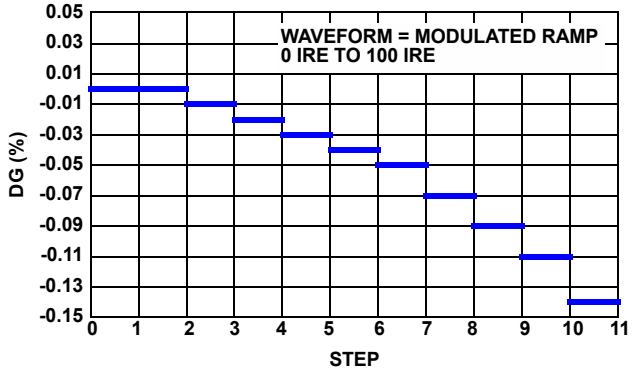


FIGURE 12. DIFFERENTIAL GAIN

Typical Performance Curves

$V_{CP} = V_S = 3.3V$, $C_{F1} = C_{F2} = 0.1\mu F$, $C_{S1} = C_{S2} = 0.22\mu F$, $C_{FIL1} = C_{FIL2} = 0.4\mu F$, $C_{IN1} = C_{IN2} = C_{IN3} = C_{IN4} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$. **(Continued)**

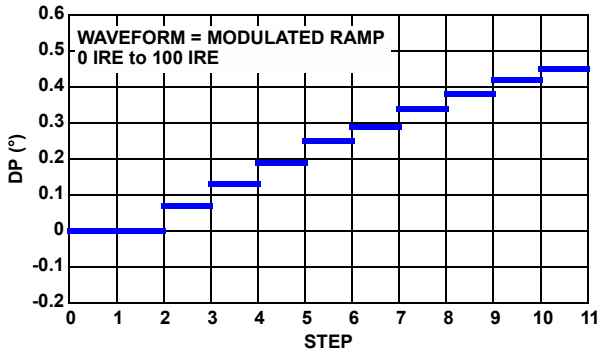


FIGURE 13. DIFFERENTIAL PHASE

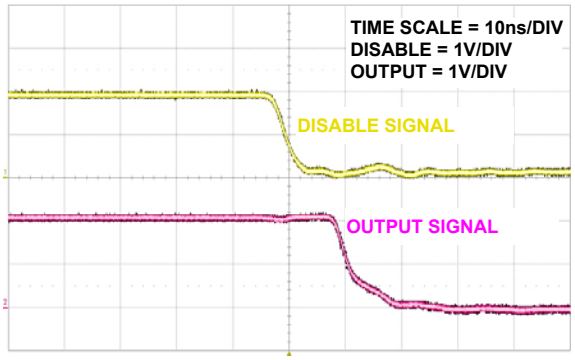


FIGURE 14. DISABLE TIME

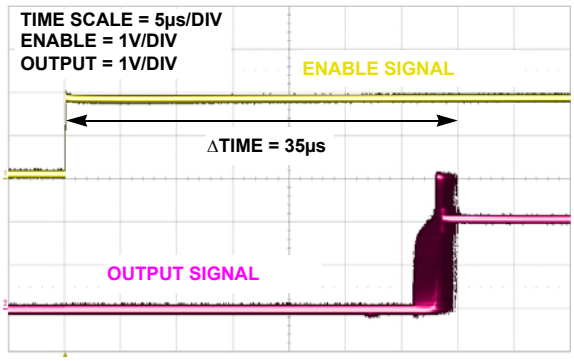


FIGURE 15. ENABLE TIME

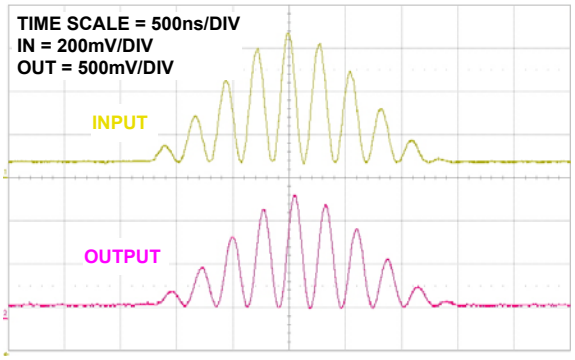


FIGURE 16. 12.5T RESPONSE (CHANNELS 1 and 3)

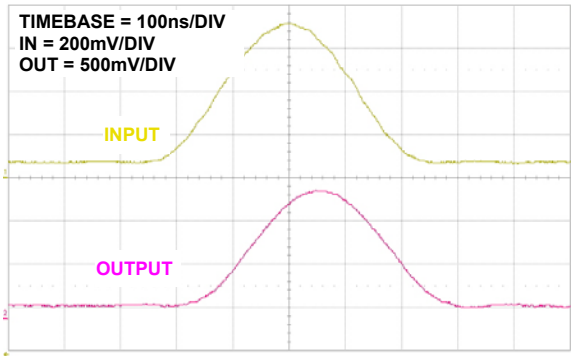


FIGURE 17. 2T RESPONSE (CHANNELS 1 and 3)

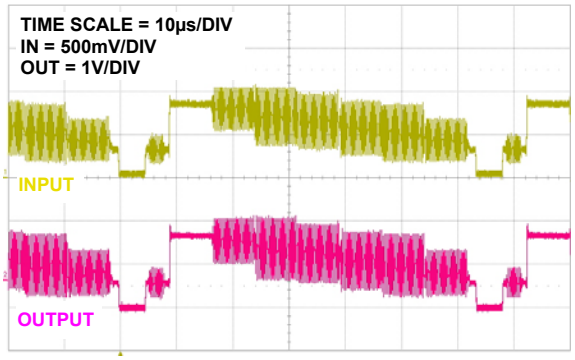


FIGURE 18. NTSC COLORBAR (CHANNELS 1 and 3)

Typical Performance Curves

$V_{CP} = V_S = 3.3V$, $C_{F1} = C_{F2} = 0.1\mu F$, $C_{S1} = C_{S2} = 0.22\mu F$, $C_{FIL1} = C_{FIL2} = 0.4\mu F$, $C_{IN1} = C_{IN2} = C_{IN3} = C_{IN4} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$. **(Continued)**

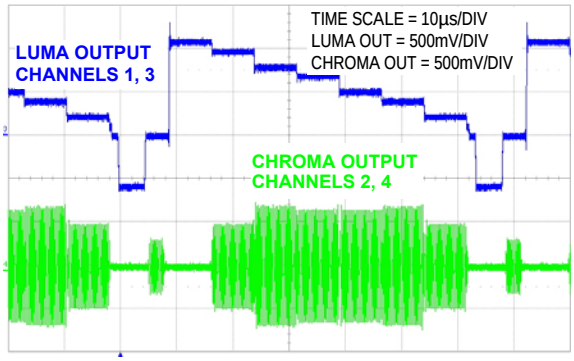


FIGURE 19. S-VIDEO SCOPE SHOT

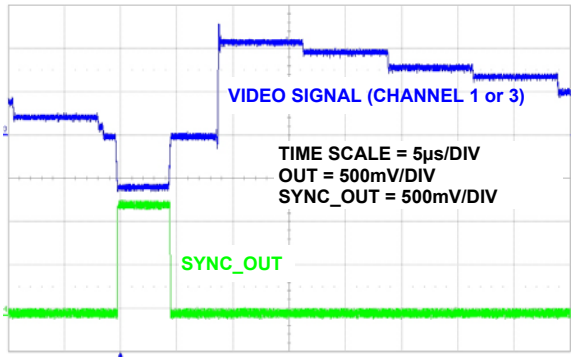


FIGURE 20. SYNC_OUT SIGNAL

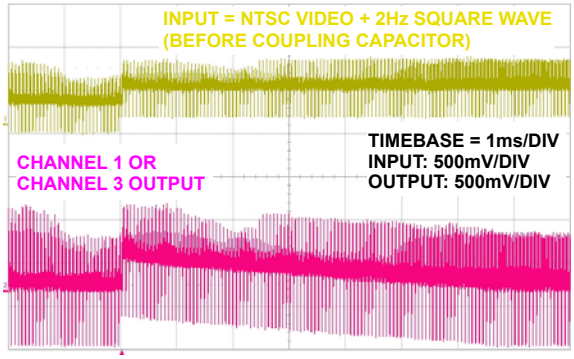


FIGURE 21. LUMA CLAMP RESPONSE TO POSITIVE TRANSIENT (CHANNEL 1 AND 3)

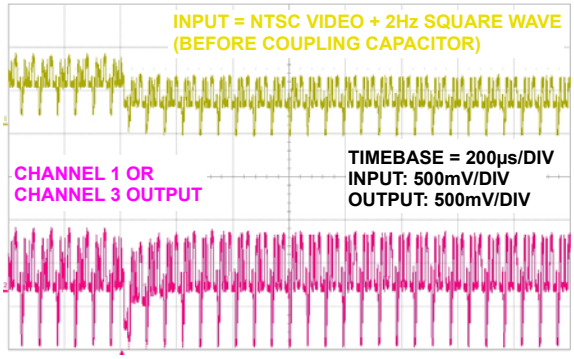


FIGURE 22. LUMA CLAMP RESPONSE TO NEGATIVE TRANSIENT (CHANNEL 1 AND 3)

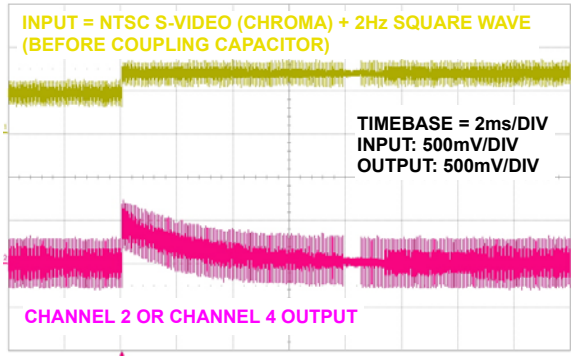


FIGURE 23. CHROMA CLAMP RESPONSE TO POSITIVE TRANSIENT (CHANNEL 2 AND 4)

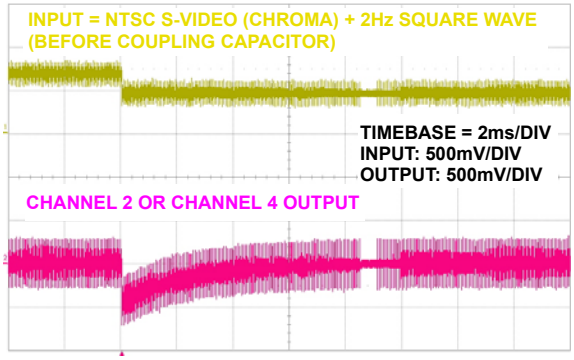


FIGURE 24. CHROMA CLAMP RESPONSE TO NEGATIVE TRANSIENT (CHANNEL 2 AND 4)

Typical Performance Curves

$V_{CP} = V_S = 3.3V$, $C_{F1} = C_{F2} = 0.1\mu F$, $C_{S1} = C_{S2} = 0.22\mu F$, $C_{FIL1} = C_{FIL2} = 0.4\mu F$, $C_{IN1} = C_{IN2} = C_{IN3} = C_{IN4} = 0.1\mu F$, $R_{L1} = R_{L2} = 150\Omega$. **(Continued)**

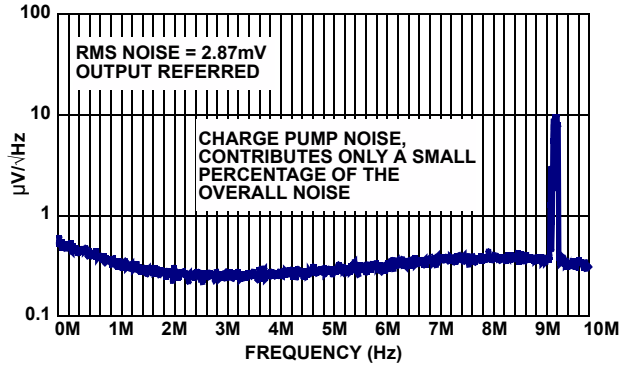


FIGURE 25. NOISE SPECTRUM

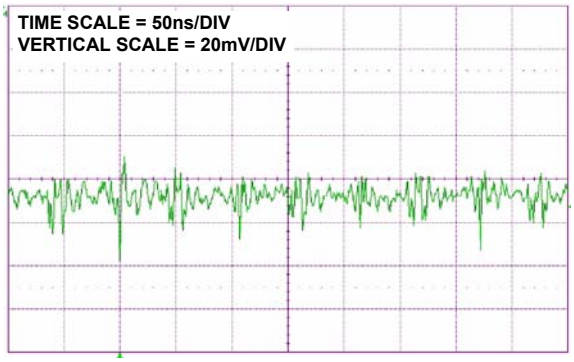


FIGURE 26. CHARGE PUMP FEEDTHROUGH AT AMPLIFIER OUTPUT

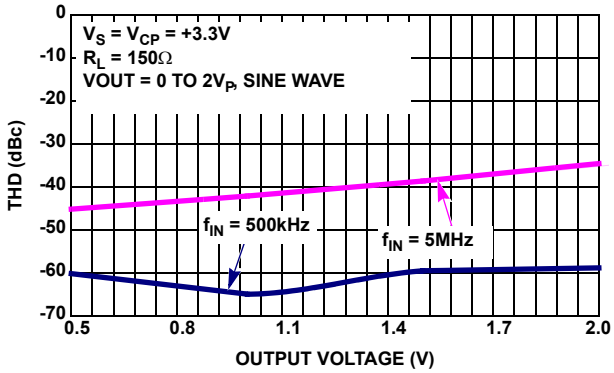


FIGURE 27. THD (dBc) vs OUTPUT VOLTAGE (V_{P-P})

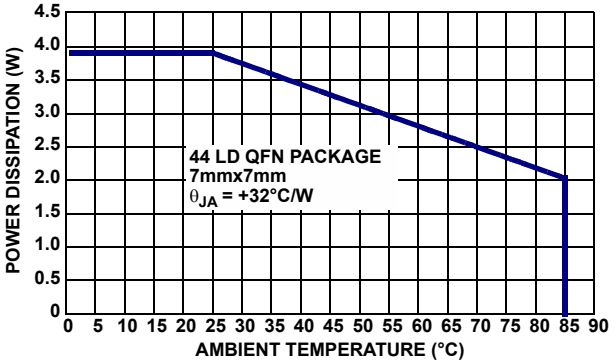


FIGURE 28. PACKAGE POWER DISSIPATION

Description of Operation and Application Information

Theory of Operation

The ISL59834 is a single supply video driver with a reconstruction filter and an on-board charge pump. It is designed to drive SDTV displays with component (YPbPr), S-video (Y-C), or composite video (CV) signals. The input signals can be AC or DC-coupled. When AC-coupled, a sync tip clamp sets the blank level to ground at the output of Channel 1 and Channel 3. Keyed clamps force the average levels of Channel 2 and Channel 4 to ground. The keyed clamps force the outputs to ground when SYNC_INA or SYNC_INB are driven to the logic high state. The ISL59834 outputs are capable of driving two AC or DC-coupled standard video loads and have a 4th order Butterworth reconstruction filter with nominal -3dB frequency set to 9MHz, providing 40dB of attenuation at 27MHz. The ISL59834 is designed to operate with a single supply voltage range ranging from 3.0V to 3.6V. This eliminates the need for a split supply with the incorporation of two charge pumps capable of generating a bottom rail as much as 1.5V below ground; providing a 4.8V range on a single 3.3V supply. This performance is ideal for NTSC video with negative-going sync pulses.

Output Amplifier

The ISL59834 output amplifiers provide a gain of +6dB. The output amplifiers are able to drive a $2.8V_{P-P}$ video signal into a 150Ω or 75Ω load to ground.

The outputs are highly-stable, low distortion, low power, high frequency amplifiers capable of driving moderate (~10pF) capacitive loads.

Input/Output Range

The ISL59834 has a dynamic input range of 0 to $1.4V_{P-P}$ This allows the device to handle high amplitude video signal inputs. As the input signal moves outside the specified range, the output signal will exhibit increasingly higher levels of harmonic distortion.

Charge Pump

The ISL59834 contains two charge pumps; charge pump A supplies Channel 1 and 2, while charge pump B supplies Channel 3 and 4. The ISL59834 charge pumps provide a bottom rail up to 1.5V below ground while operating on a 3.0V to 3.6V power supply. The charge pumps are internally regulated and are driven by internal 9.5MHz clocks. The clock

pins for both charge pumps (CLK_A and CLK_B) must be shorted together.

To reduce the noise on the power supply generated by the charge pump, connect a lowpass RC-network between VEE_{OUT} and VEE_{IN}. See the “Typical Application Circuits” for further information.

VEE_{OUT} Pins

$VEEA_{OUT}$ and $VEEB_{OUT}$ are the output pins for the charge pumps. Keep in mind that these outputs are fully regulated supplies that must be properly bypassed. Bypass these pins with a 0.47µF ceramic capacitor placed as close to the pin and connected to the ground plane of the board.

VEE_{IN} Pins

$VEEA_{IN}$ and $VEEB_{IN}$ are the subtrate connections for the ISL59834, **these two pins must be shorted together.** To reduce the noise on the power supply generated by the charge pump, connect a lowpass RC-network between VEE_{OUT} and VEE_{IN}. See the “Typical Application Circuits” for further information.

Video Performance

DIFFERENTIAL GAIN/PHASE

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency and phase response as DC levels are changed at the output. Special circuitry has been incorporated into the ISL59834 to reduce the output impedance variation with the current output. This results in outstanding differential gain and differential phase specifications of 0.45% and 0.15°, while driving 150Ω at a gain of +2V/V.

NTSC

The ISL59834, generating a negative rail internally, is ideally suited for NTSC video with its accompanying negative-going sync signals.

S-VIDEO

For a typical S-video application with two S-video signals, connect the luma signals to Channel 1 and 3, and connect the chrominance signals to Channel 2 and 4. For clamp timing, connect SYNC_OUTA to SYNC_INA and SYNC_OUTB to SYNC_INB. See the “S-Video Typical Application Circuit” on page 8.

YPbPr

For a typical component video application, connect Y to Channel 1, Pb to Channel 2 and Pr to Channel 4. Channel 3 can be optionally used a composite signal. For the clamp timing, connect SYNC_OUTA to both SYNC_INA and SYNC_INB and leave SYNC_OUTB floating. See the “YPbPr Typical Application Circuit” on page 7.

AC-Coupled Inputs

SYNC TIP CLAMP (CHANNEL 1 AND 3)

The ISL59834 features a sync tip clamp that forces the black level of the output video signal to ground. This ensures that the sync-tip voltage level will be approximately -300mV at the back-termination resistor of a standard video load. The clamp is activated whenever the input voltage falls below 0V. The correction voltage required to do this is stored across the input AC-coupling capacitor. Refer to Typical Application Circuit for a detailed diagram.

KEYED CLAMP (CHANNEL 2 AND 4)

Channel 2 and Channel 4 have a keyed clamp, which forces the output to ground when SYNC_INA (Channel 2) or SYNC_INB (Channel 4) are driven to the logic high state. The SYNC_IN pins may be connected to either SYNC_OUT pins or they may be driven by external sources.

SYNC DETECTOR AND CLAMP TIMING

Channel 1 and Channel 3 also have sync detectors whose outputs are available at SYNC_OUTA and SYNC_OUTB pins respectively.

The slice level for the sync detectors is between 100mV to 200mV. This means that if the signal level is below 100mV at Channel 1 or 3, then SYNC_OUTA or SYNC_OUTB are high. If the signal level is above 200mV, then SYNC_OUTA or SYNC_OUTB are low. Figure 29 shows the operation of the sync detector.

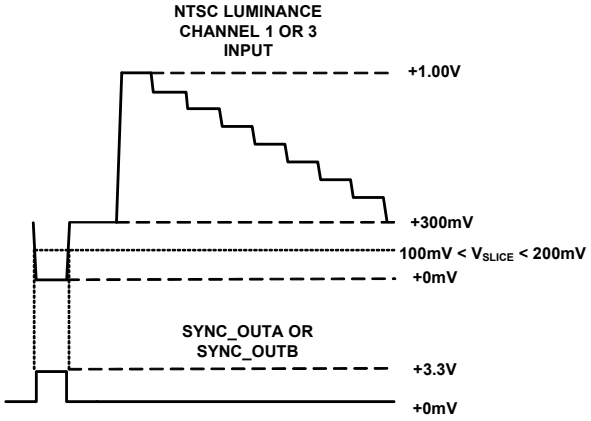


FIGURE 29. SYNC DETECTOR SLICE LEVEL

DC-Coupled Inputs (Channel 1 and 3)

When DC-coupling the inputs, ensure that the lowest signal level is greater than +50mV to prevent the clamp from turning on and distorting the output. When DC-coupled, the ISL59834 shifts the signal by -620mV.

Amplifier Disable

The ISL59834 can be disabled and its output placed in a high impedance state. ENABLEA shuts off Channel 1 and 2 while ENABLEB shuts off Channel 3 and 4. **Both ENABLE pins must be shorted together**. The turn-off time is around 10ns and the turn-on time is around 35µs. The turn-on time is longer because extra time is needed for the charge pump to settle before the amplifiers are enabled. When disabled, the device supply current is reduced to 5µA. Power-down is controlled by standard TTL or CMOS signal levels at the ENABLE pins. The applied logic signal is relative to the GND pin. Applying a signal that is less than 0.8V above GND will disable the device. The device will be enabled when the ENABLE signals are 2V above GND.

Output Drive Capability

The maximum output current for the ISL59834 is ±50mA. Maximum reliability is maintained if the output current never exceeds ±50mA, after which the electro-migration limit of the process will be exceeded and the part will be damaged. This limit is set by the design of the internal metal interconnections.

Driving Capacitive Loads and Cables

The ISL59834 (internally-compensated to drive 75Ω cables) will drive 10pF loads in parallel with 150Ω or 75Ω with less than 1.3dB of peaking.

Power Dissipation

With the high output drive capability of the ISL59834, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}i) \times \frac{V_{OUT}i}{R_{LOAD}i} \quad \text{(EQ. 2)}$$

for sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT}i - V_S) \times I_{LOAD}i \quad \text{(EQ. 3)}$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

i = Number of output channels

By setting Equation 1 equal to Equation 2 and 3, we can solve for the output current and R_{LOAD} values needed to avoid exceeding the maximum junction temperature.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Strip line design techniques are recommended for the input and output signal traces to help control the characteristic impedance. Furthermore, the characteristic impedance of the traces should be 75Ω. Trace lengths should be as short as possible between the output pin and the series 75Ω resistor. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S and V_{CP} to GND will suffice.

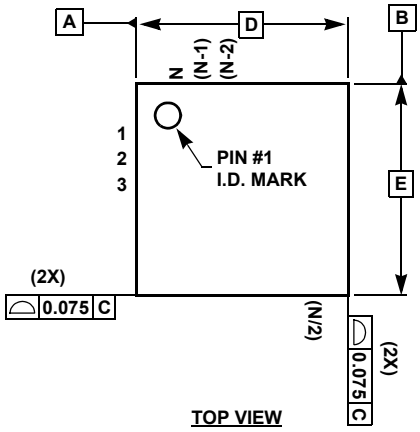
The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- Use low inductance components, such as chip resistors and chip capacitors whenever possible.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners; use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces longer than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. To maintain frequency performance with longer traces, use striplines.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.

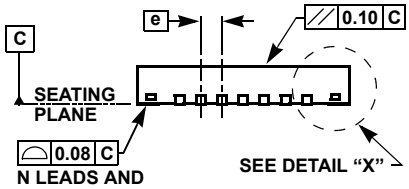
- Route all signal I/O lines over continuous ground planes (i.e. no split planes or PCB gaps under these lines).
- Place termination resistors in their optimum location as close to the device as possible.
- Use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum when testing.
- Place flying and output capacitors as close to the device as possible for the charge pump.

Decouple well, using a minimum of 2 power supply decoupling capacitors, placed as close to the device as possible. Avoid vias between the capacitor and the device because vias add unwanted inductance. Larger capacitors may be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.

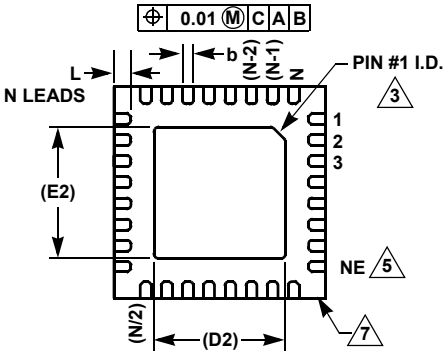
Quad Flat No-Lead Plastic Package (QFN)



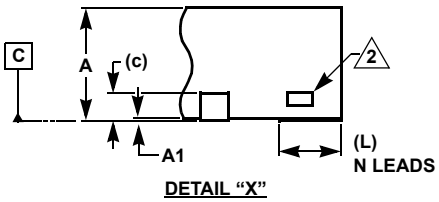
TOP VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "X"

L44.7x7A

44 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.85	0.90	-
A1	0.00	0.02	0.05	-
b	0.20	0.25	0.30	-
c		0.203 REF		-
D		7.00 BASIC		-
D2		5.10 REF		8
E		7.00 BASIC		-
E2		5.10 REF		8
e		0.50 BASIC		-
L	0.50	0.55	0.60	-
N		44 REF		4
ND		11 REF		6
NE		11 REF		5

Rev. 1 1/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.
9. One of 10 packages in MDP0046