

4-1/2 Digit Analog-to-Digital Converters with On-Chip LCD Drivers

Features:

- Count Resolution: $\pm 19,999$
- Resolution on 200 mV Scale: $10 \mu\text{V}$
- True Differential Input and Reference
- Low Power Consumption: $500 \mu\text{A}$ at 9V
- Direct LCD Driver for 4-1/2 Digits, Decimal Points, Low Battery Indicator, and Continuity Indicator
- Overrange and Underrange Outputs
- Range Select Input: 10:1
- High Common Mode Rejection Ratio: 110 dB
- External Phase Compensation Not Required

Applications:

- Full-Featured Multimeters
- Digital Measurement Devices

Device Selection Table

Package Code	Pin Layout	Package	Temperature Range
TC7129CPL	Normal	40-Pin PDIP	0°C to +70°C
TC7129CKW	Formed	44-Pin PQFP	0°C to +70°C
TC7129CLW	–	44-Pin PLCC	0°C to +70°C

General Description:

The TC7129 is a 4-1/2 digit Analog-to-Digital Converter (ADC) that directly drives a multiplexed Liquid Crystal Display (LCD). Fabricated in high-performance, low-power CMOS, the TC7129 ADC is designed specifically for high-resolution, battery-powered digital multimeter applications. The traditional dual-slope method of A/D conversion has been enhanced with a successive integration technique to produce readings accurate to better than 0.005% of full-scale and resolution down to $10 \mu\text{V}$ per count.

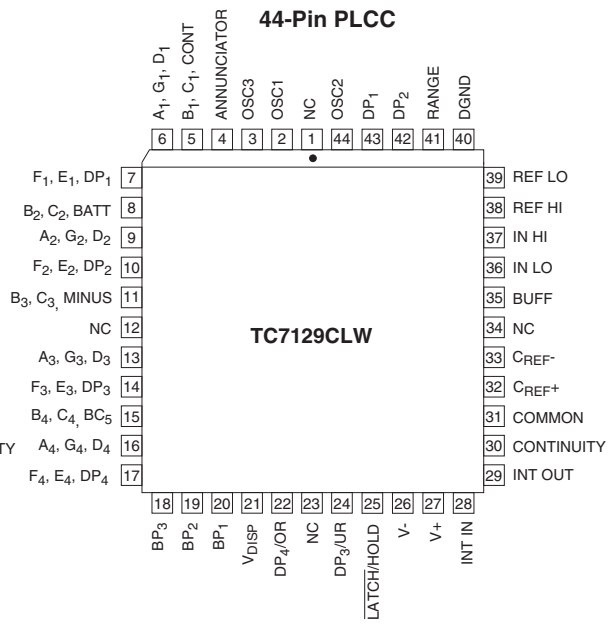
The TC7129 includes features important to multimeter applications. It detects and indicates low battery condition. A continuity output drives an annunciator on the display and can be used with an external driver to sound an audible alarm. Overrange and underrange outputs, along with a range-change input, provide the ability to create auto-ranging instruments. For snapshot readings, the TC7129 includes a latch-and-hold input to freeze the present reading. This combination of features makes the TC7129 the ideal choice for full-featured multimeter and digital measurement applications.

Typical Application



TC7129

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V+ to V-)	15V
Reference Voltage (REF HI or REF LO)	V+ to V-
Input Voltage (IN HI or IN LO) (Note 1)	V+ to V-
V _{DISP}	V+ to (DGND - 0.3V)
Digital Input (Pins 1, 2, 19, 20, 21, 22, 27, 37, 39, 40)	DGND to V+
Analog Input (Pins 25, 29, 30)	V+ to V-
Package Power Dissipation (T _A ≤ 70°C)	
Plastic DIP	1.23W
PLCC	1.23W
Plastic QFP	1.00W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC7129 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V+ to V- = 9V, V _{REF} = 1V, T _A = +25°C, f _{CLK} = 120 kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Input						
	Zero Input Reading	-0000	0000	+0000	Counts	V _{IN} = 0V, 200 mV scale
	Zero Reading Drift	—	±0.5	—	μV/°C	V _{IN} = 0V, 0°C < T _A < +70°C
	Ratiometric Reading	9996	—	10000	Counts	V _{IN} = V _{REF} = 1000 mV, Range = 2V
	Range Change Accuracy	0.9999	1.0000	1.0001	Ratio	V _{IN} = 1V on High Range, V _{IN} = 0.1V on Low Range
RE	Rollover Error	—	1	2	Counts	V _{IN-} = V _{IN+} = 199 mV
NL	Linearity Error	—	1	—	Counts	200mV Scale
CMRR	Common Mode Rejection Ratio	—	110	—	dB	V _{CM} = 1V, V _{IN} = 0V, 200 mV scale
CMVR	Common Mode Voltage Range	—	(V-) + 1.5	—	V	V _{IN} = 0V
		—	(V+) - 1	—	V	200 mV scale
e _N	Noise (Peak-to-Peak Value not Exceeded 95% of Time)	—	14	—	μV _{P-P}	V _{IN} = 0V, 200 mV scale
I _{IN}	Input Leakage Current	—	1	10	pA	V _{IN} = 0V, pins 32, 33
	Scale Factor Temperature Coefficient	—	2	7	ppm/°C	V _{IN} = 199 mV, 0°C < T _A < +70°C, External V _{REF} = 0 ppm/°C

Note 1: Input voltages may exceed supply voltages, provided input current is limited to ±400 μA. Currents above this value may result in invalid display readings, but will not destroy the device if limited to ±1 mA. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

TC7129

TC7129 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: V_+ to $V_- = 9V$, $V_{REF} = 1V$, $T_A = +25^\circ C$, $f_{CLK} = 120\text{ kHz}$, unless otherwise indicated. Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Power						
V_{COM}	Common Voltage	2.8	3.2	3.5	V	V_+ to pin 28
	Common Sink Current	—	0.6	—	mA	$\Delta Common = +0.1V$
	Common Source Current	—	10	—	μA	$\Delta Common = -0.1V$
DGND	Digital Ground Voltage	4.5	5.3	5.8	V	V_+ to pin 36, V_+ to $V_- = 9V$
	Sink Current	—	1.2	—	mA	$\Delta DGND = +0.5V$
	Supply Voltage Range	6	9	12	V	V_+ to V_-
I_S	Supply Current Excluding Common Current	—	0.8	1.3	mA	V_+ to $V_- = 9V$
f_{CLK}	Clock Frequency	—	120	360	kHz	
	V_{DISP} Resistance	—	50	—	k Ω	V_{DISP} to V_+
	Low Battery Flag Activation Voltage	6.3	7.2	7.7	V	V_+ to V_-
Digital						
	Continuity Comparator Threshold Voltages	100	200	—	mV	V_{OUT} pin 27 = High
		—	200	400	mV	V_{OUT} pin 27 = Low
	Pull-down Current	—	2	10	μA	Pins 37, 38, 39
	"Weak Output" Current Sink/Source	—	3/3	—	μA	Pins 20, 21 sink/source
		—	3/9	—	μA	Pin 27 sink/source
	Pin 22 Source Current	—	40	—	μA	
	Pin 22 Sink Current	—	3	—	μA	

Note 1: Input voltages may exceed supply voltages, provided input current is limited to $\pm 400\ \mu A$. Currents above this value may result in invalid display readings, but will not destroy the device if limited to $\pm 1\text{ mA}$. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

2.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. 40-Pin PDIP	Pin No. 44-Pin PQFP	Pin No. 44-Pin PLCC	Symbol	Function
1	40	2	OSC1	Input to first clock inverter.
2	41	3	OSC3	Output of second clock inverter.
3	42	4	ANNUNCIATOR	Backplane square wave output for driving annunciators.
4	43	5	B ₁ , C ₁ , CONT	Output to display segments.
5	44	6	A ₁ , G ₁ , D ₁	Output to display segments.
6	1	7	F ₁ , E ₁ , DP ₁	Output to display segments.
7	2	8	B ₂ , C ₂ , LO BATT	Output to display segments.
8	3	9	A ₂ , G ₂ , D ₂	Output to display segments.
9	4	10	F ₂ , E ₂ , DP ₂	Output to display segments.
10	5	11	B ₃ , C ₃ , MINUS	Output to display segments.
11	7	13	A ₃ , G ₃ , D ₃	Output to display segments.
12	8	14	F ₃ , E ₃ , DP ₃	Output to display segments.
13	9	15	B ₄ , C ₄ , BC ₅	Output to display segments.
14	10	16	A ₄ , D ₄ , G ₄	Output to display segments.
15	11	17	F ₄ , E ₄ , DP ₄	Output to display segments.
16	12	18	BP ₃	Backplane #3 output to display.
17	13	19	BP ₂	Backplane #2 output to display.
18	14	20	BP ₁	Backplane #1 output to display.
19	15	21	V _{DISP}	Negative rail for display drivers.
20	16	22	DP ₄ /OR	Input: When high, turns on most significant decimal point. Output: Pulled high when result count exceeds ±19,999.
21	18	24	DP ₃ /UR	Input: Second-most significant decimal point on when high. Output: Pulled high when result count is less than ±1000.
22	19	25	LATCH/HOLD	Input: When floating, ADC operates in Free Run mode. When pulled high, the last displayed reading is held. When pulled low, the result counter contents are shown incrementing during the de-integrate phase of cycle. Output: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	20	26	V-	Negative power supply terminal.
24	21	27	V+	Positive power supply terminal and positive rail for display drivers.
25	22	28	INT IN	Input to integrator amplifier.
26	23	29	INT OUT	Output of integrator amplifier.
27	24	30	CONTINUITY	Input: When low, continuity flag on the display is off. When high, continuity flag is on. Output: High when voltage between inputs is less than +200 mV. Low when voltage between inputs is more than +200 mV.
28	25	31	COMMON	Sets common mode voltage of 3.2V below V+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	26	32	C _{REF+}	Positive side of external reference capacitor.
30	27	33	C _{REF-}	Negative side of external reference capacitor.
31	29	35	BUFFER	Output of buffer amplifier.
32	30	36	IN LO	Negative input voltage terminal.
33	31	37	IN HI	Positive input voltage terminal.
34	32	38	REF HI	Positive reference voltage.
35	33	39	REF LO	Negative reference voltage

TC7129

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin No. 40-Pin PDIP	Pin No. 44-Pin PQFP	Pin No. 44-Pin PLCC	Symbol	Function
36	34	40	DGND	Internal ground reference for digital section. See Section 4.2.1 “±5V Power Supply” .
37	35	41	RANGE	3 μ A pull-down for 200 mV scale. Pulled high externally for 2V scale.
38	36	42	DP ₂	Internal 3 μ A pull-down. When high, decimal point 2 will be on.
39	37	43	DP ₁	Internal 3 μ A pull-down. When high, decimal point 1 will be on.
40	38	44	OSC2	Output of first clock inverter. Input of second clock inverter.
—	6,17, 28, 39	12, 23, 34, 1	NC	No connection.

3.0 DETAILED DESCRIPTION

(All pin designations refer to 40-pin PDIP.)

The TC7129 is designed to be the heart of a high-resolution analog measurement instrument. The only additional components required are a few passive elements: a voltage reference, a LCD and a power source. Most component values are not critical; substitutes can be chosen based on the information given below.

The basic circuit for a digital multimeter application is shown in Figure 3-1. See **Section 4.0 “Typical Applications”**, for variations. Typical values for each component are shown. The sections below give component selection criteria.

3.1 Oscillator (X_{OSC} , C_{O1} , C_{O2} , R_O)

The primary criterion for selecting the crystal oscillator is to choose a frequency that achieves maximum rejection of line frequency noise. To do this, the integration phase should last an integral number of line cycles. The integration phase of the TC7129 is 10,000 clock cycles on the 200 mV range and 1000 clock cycles on the 2V range. One clock cycle is equal to two oscillator cycles. For 60 Hz rejection, the oscillator frequency should be chosen so that the period of one line cycle equals the integration time for the 2V range.

EQUATION 3-1:

$$\frac{1}{60} \text{ second} = 16.7 \text{ msec} = \frac{1000 \text{ clock cycles} * 2 \text{ OSC cycles/clock cycle}}{\text{OSC Frequency}}$$

This equation gives an oscillator frequency of 120 kHz. A similar calculation gives an optimum frequency of 100 kHz for 50 Hz rejection.

The resistor and capacitor values are not critical; those shown work for most applications. In some situations, the capacitor values may have to be adjusted to compensate for parasitic capacitance in the circuit. The capacitors can be low-cost ceramic devices.

Some applications can use a simple RC network instead of a crystal oscillator. The RC oscillator has more potential for jitter, especially in the least significant digit. See **Section 4.5 “RC Oscillator”**.

3.2 Integrating Resistor (R_{INT})

The integrating resistor sets the charging current for the integrating capacitor. Choose a value that provides a current between 5 μA and 20 μA at 2V, the maximum full-scale input. The typical value chosen gives a charging current of 13.3 μA :

EQUATION 3-1:

$$I_{\text{CHARGE}} = \frac{2\text{V}}{150 \text{ k}\Omega} = 13.3 \mu\text{A}$$

Too high a value for R_{INT} increases the sensitivity to noise pickup and increases errors due to leakage current. Too low a value degrades the linearity of the integration, leading to inaccurate readings.

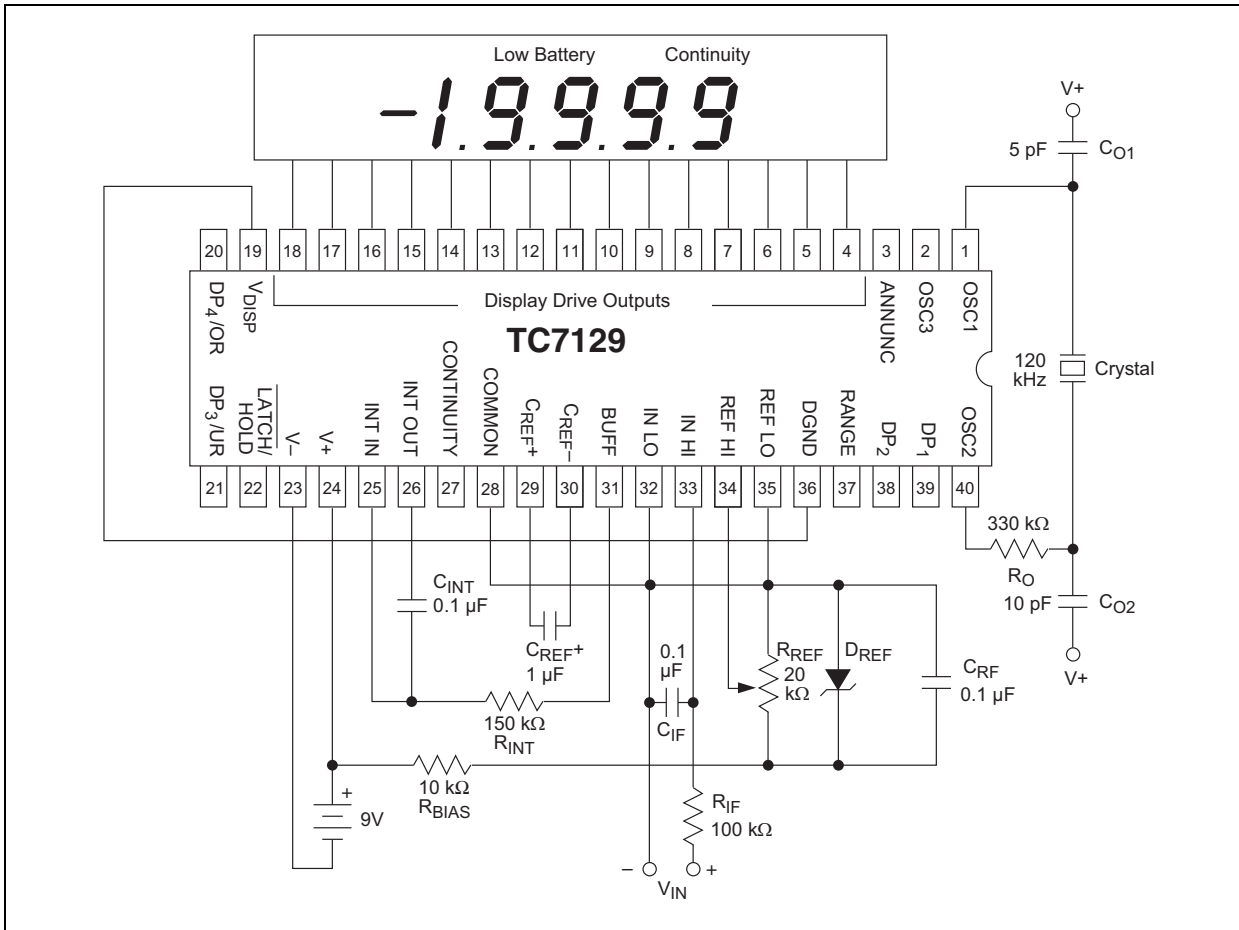


Figure 3-1: Standard Circuit.

3.3 Integrating Capacitor (C_{INT})

The charge stored in the integrating capacitor during the integrate phase is directly proportional to the input voltage. The primary selection criterion for C_{INT} is to choose a value that gives the highest voltage swing while remaining within the high-linearity portion of the integrator output range. An integrator swing of 2V is the recommended value. The capacitor value can be calculated using the following equation:

EQUATION 3-1:

$$C_{INT} = \frac{t_{INT} \times I_{INT}}{V_{SWING}}$$

Where t_{INT} is the integration time.

Using the values derived above (assuming 60 Hz operation), the equation becomes:

EQUATION 3-2:

$$C_{INT} = \frac{16.7 \text{ msec} \times 13.3 \mu\text{A}}{2\text{V}} = 0.1 \mu\text{A}$$

The capacitor should have low dielectric absorption to ensure good integration linearity. Polypropylene and Teflon® capacitors are usually suitable. A good measurement of the dielectric absorption is to connect the reference capacitor across the inputs by connecting:

Pin-to-Pin:

20 → 33 (C_{REF+} to IN HI)

30 → 32 (C_{REF-} to IN LO)

A reading between 10,000 and 9998 is acceptable; anything lower indicates unacceptably high dielectric absorption.

3.4 Reference Capacitor (C_{REF})

The reference capacitor stores the reference voltage during several phases of the measurement cycle. Low leakage is the primary selection criterion for this component. The value must be high enough to offset the effect of stray capacitance at the capacitor terminals. A value of at least 1 μF is recommended.

3.5 Voltage Reference (D_{REF} , R_{REF} , R_{BIAS} , C_{RF})

The reference potentiometer (R_{REF}) provides an adjustment for adjusting the reference voltage; any value above 20 k Ω is adequate. The bias resistor (R_{BIAS}) limits the current through D_{REF} to less than 150 μ A. The reference filter capacitor (C_{RF}) forms an RC filter with R_{BIAS} to help eliminate noise.

3.6 Input Filter (R_{IF} , C_{IF})

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value should not exceed 100 k Ω . A typical RC time constant value is 16.7 msec to help reject line frequency noise. The input filter capacitor should have low leakage for a high-impedance input.

3.7 Battery

The typical circuit uses a 9V battery as a power source. However, any value between 6V and 12V can be used. For operation from batteries with voltages lower than 6V and for operation from power supplies, see Section 4.2 "Powering the TC7129".

4.0 TYPICAL APPLICATIONS

4.1 TC7129 as a Replacement Part

The TC7129 is a direct pin-for-pin replacement part for the ICL7129. Note, however, that the ICL7129 requires a capacitor and resistor between pins 26 and 28 for phase compensation. Since the TC7129 uses internal phase compensation, these parts are not required and, in fact, must be removed from the circuit for stable operation.

4.2 Powering the TC7129

While the most common power source for the TC7129 is a 9V battery, there are other possibilities. Some of the more common ones are explained below.

4.2.1 $\pm 5V$ Power Supply

Measurements are made with respect to power supply ground. DGND (pin 36) is set internally to about 5V less than $V+$ (pin 24); it is not intended to be a power supply input and must not be tied directly to power supply ground. It can be used as a reference for external logic, as explained in Section 4.3 "Connecting to External Logic", (see Figure 4-1).



Figure 4-1: Powering the TC7129 From a $\pm 5V$ Power Supply.

4.2.2 Low Voltage Battery Source

A battery with voltage between 3.8V and 6V can be used to power the TC7129 when used with a voltage doubler circuit, as shown in Figure 4-2. The voltage doubler uses the TC7660 DC-to-DC voltage converter and two external capacitors.

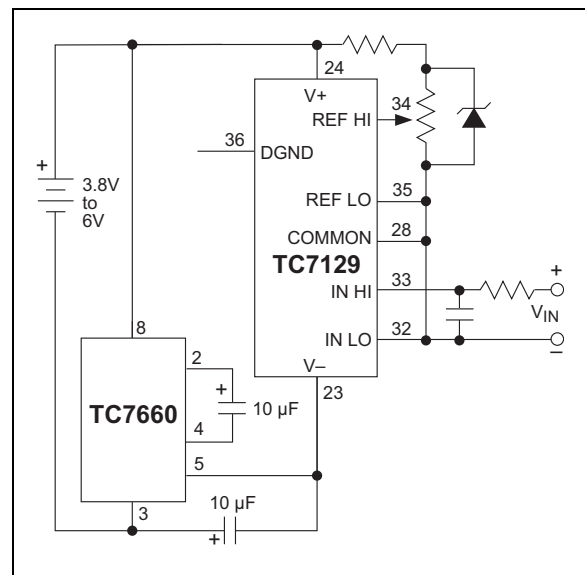


Figure 4-2: Powering the TC7129 From a Low-Voltage Battery.

TC7129

4.2.3 +5V Power Supply

Measurements are made with respect to power supply ground. COMMON (pin 28) is connected to REF LO (pin 35). A voltage doubler is needed, since the supply voltage is less than the 6V minimum needed by the TC7129. DGND (pin 36) must be isolated from power supply ground (see Figure 4-3).

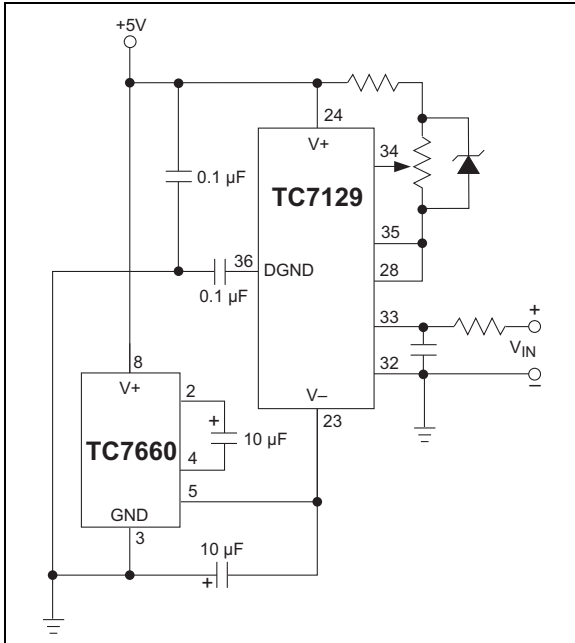


Figure 4-3: Powering the TC7129 From a +5V Power Supply.

4.3 Connecting to External Logic

External logic can be directly referenced to DGND (pin 36), provided that the supply current of the external logic does not exceed the sink current of DGND (Figure 4-4). A safe value for DGND sink current is 1.2 mA. If the sink current is expected to exceed this value, a buffer is recommended (see Figure 4-5).

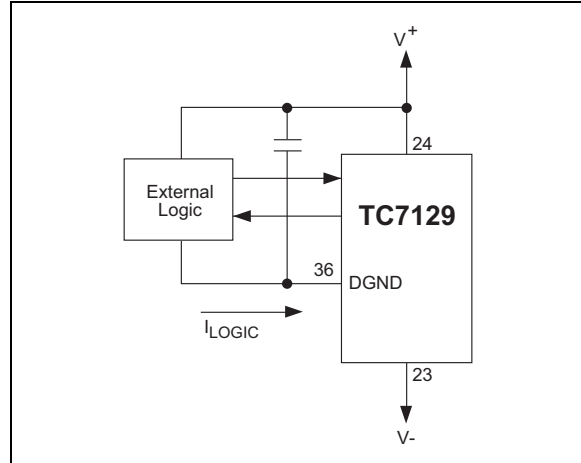


Figure 4-4: External Logic Referenced Directly to DGND.

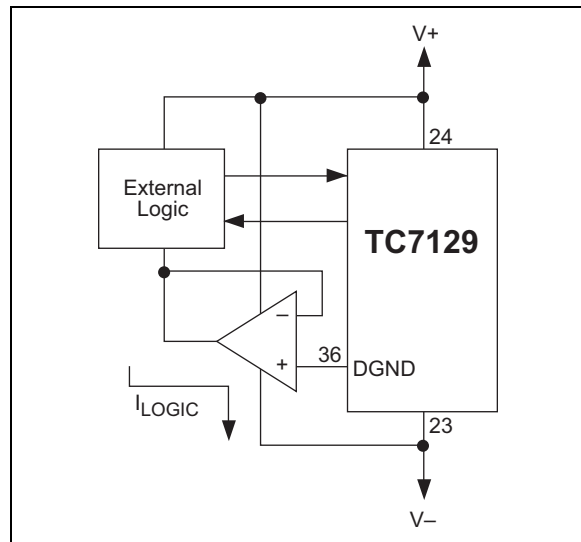


Figure 4-5: External Logic Referenced to DGND with Buffer.

4.4 Temperature Compensation

For most applications, V_{DISP} (pin 19) can be connected directly to DGND (pin 36). For applications with a wide temperature range, some LCDs require that the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 4-6 shows two circuits that can be adjusted to give temperature compensation of about 10 mV/°C between $V+$ (pin 24) and V_{DISP} . The diode between DGND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed 0.3V below DGND.



Figure 4-6: Temperature Compensating Circuits.

4.5 RC Oscillator

For applications in which 3-1/2 digit (100 μ V) resolution is sufficient, an RC oscillator is adequate. A recommended value for the capacitor is 51 pF. Other values can be used as long as they are sufficiently larger than the circuit parasitic capacitance. The resistor value is calculated as:

EQUATION 4-1:

$$R = \frac{0.45}{\text{Freq} * C}$$

For 120 kHz frequency and C = 51 pF, the calculated value of R is 75 k Ω . The RC oscillator and the crystal oscillator circuits are shown in Figure 4-7.



Figure 4-7: Oscillator Circuits.

4.6 Measuring Techniques

Two important techniques are used in the TC7129: successive integration and digital auto-zeroing. Successive integration is a refinement to the traditional dual-slope conversion technique.

4.7 Dual-Slope Conversion

A dual-slope conversion has two basic phases: integrate and de-integrate. During the integrate phase, the input signal is integrated for a fixed period of time; the integrated voltage level is thus proportional to the input voltage. During the de-integrate phase, the integrated voltage is ramped down at a fixed slope, and a counter counts the clock cycles until the integrator voltage crosses zero. The count is a measurement of the time to ramp the integrated voltage to zero and is, therefore, proportional to the input voltage being measured. This count can then be scaled and displayed as a measurement of the input voltage. Figure 4-8 shows the phases of the dual-slope conversion.

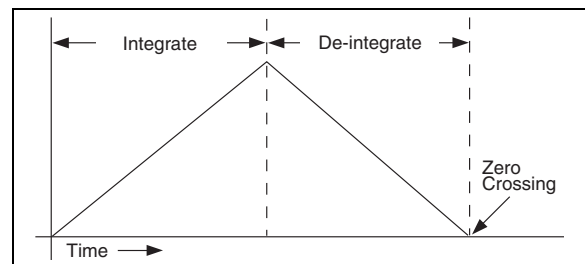


Figure 4-8: Dual-Slope Conversion.

The dual-slope method has a fundamental limitation. The count can only stop on a clock cycle, so that measurement accuracy is limited to the clock frequency. In addition, a delay in the zero-crossing comparator can add to the inaccuracy. Figure 4-9 shows these errors in an actual measurement.

TC7129



Figure 4-9: Accuracy Errors in Dual-Slope Conversion.



Figure 4-10: Integration Waveform.

4.8 Successive Integration

The successive integration technique picks up where dual-slope conversion ends. The overshoot voltage shown in Figure 4-9 (called the “integrator residue voltage”) is measured to obtain a correction to the initial count. Figure 4-10 shows the cycles in a successive integration measurement.

The waveform shown is for a negative input signal. The sequence of events during the measurement cycle is shown in Table 4-1.

TABLE 4-1: MEASUREMENT CYCLE SEQUENCE

Phase	Description
INT ₁	Input signal is integrated for fixed time (1000 clock cycles on 2V scale, 10,000 on 200 mV).
DE ₁	Integrator voltage is ramped to zero. Counter counts up until zero-crossing to produce reading accurate to 3-1/2 digits. Residue represents an overshoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE ₂	Integrator voltage is ramped to zero. Counter counts down until zero-crossing to correct reading to 4-1/2 digits. Residue represents an undershoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE ₃	Integrator voltage is ramped to zero. Counter counts up until zero-crossing to correct reading to 5-1/2 digits. Residue is discarded.

4.9 Digital Auto-Zeroing

To eliminate the effect of amplifier offset errors, the TC7129 uses a digital auto-zeroing technique. After the input voltage is measured as described above, the measurement is repeated with the inputs shorted internally. The reading with inputs shorted is a measurement of the internal errors and is subtracted from the previous reading to obtain a corrected measurement. Digital auto-zeroing eliminates the need for an external auto-zeroing capacitor used in other ADCs.

4.10 Inside the TC7129

Figure 4-11 shows a simplified block diagram of the TC7129.

TC7129



Figure 4-11: TC7129 Functional Block Diagram.



Figure 4-12: Integrator Block Diagram.

4.11 Integrator Section

The integrator section includes the integrator, comparator, input buffer amplifier and analog switches (see Table 4-2) used to change the circuit configuration during the separate measurement phases described earlier. (See Figure 4-12).

TABLE 4-2: SWITCH LEGENDS

Label	Description
Label	Meaning.
DE	Open during all de-integrate phases.
DE-	Closed during all de-integrate phases when input voltage is negative.
DE+	Closed during all de-integrate phases when input voltage is positive.
INT ₁	Closed during the first integrate phase (measurement of the input voltage).
INT ₂	Closed during the second integrate phase (measurement of the amplifier offset).
INT	Open during both integrate phases.
REST	Closed during the rest phase.
ZI	Closed during the zero integrate phase.
X10	Closed during the X10 phase.
X10	Open during the X10 phase.

The buffer amplifier has a common mode input voltage range from 1.5V above V₋ to 1V below V₊. The integrator amplifier can swing to within 0.3V of the rails. However, for best linearity, the swing is usually limited to within 1V. Both amplifiers can supply up to 80 μA of output current, but should be limited to 20 μA for good linearity.

4.12 Continuity Indicator

A comparator with a 200 mV threshold is connected between IN HI (pin 33) and IN LO (pin 32). Whenever the voltage between inputs is less than 200 mV, the CONTINUITY output (pin 27) will be pulled high, activating the continuity annunciator on the display. The continuity pin can also be used as an input to drive the continuity annunciator directly from an external source (see Figure 4-13).

A schematic of the input/output nature of this pin is also shown in Figure 4-14.

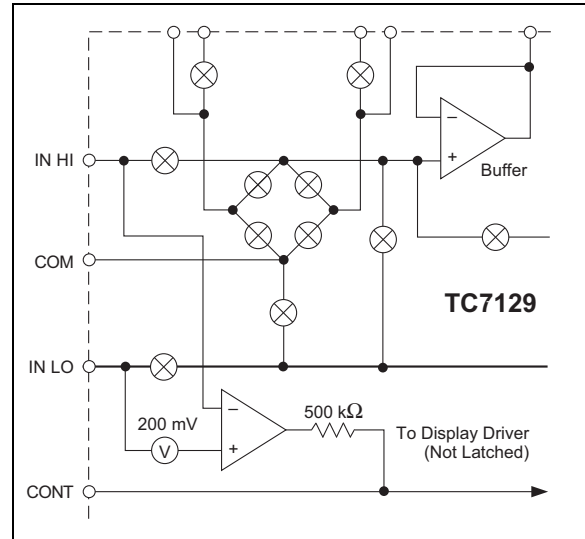


Figure 4-13: Continuity Indicator Circuit.

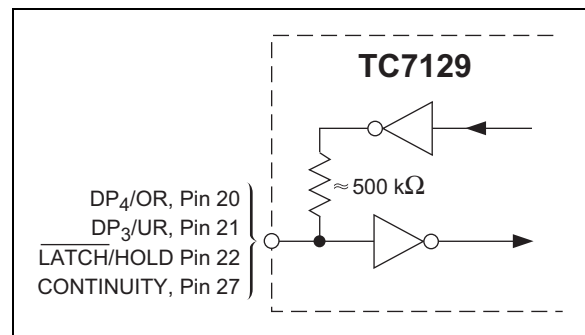


Figure 4-14: Input/Output Pin Schematic.

4.13 Common and Digital Ground

The common and digital ground (DGND) outputs are generated from internal Zener diodes. The voltage between V₊ and DGND is the internal supply voltage for the digital section of the TC7129. Common can source approximately 12 μA; DGND has essentially no source capability (see Figure 4-15).

TC7129

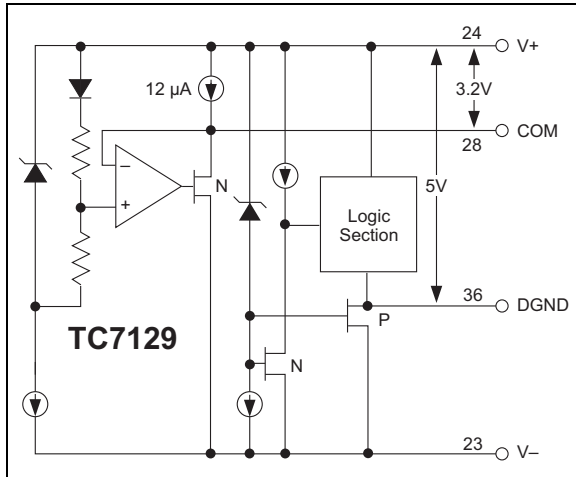


Figure 4-15: Digital Ground (DGND) and Common Outputs.

4.14 Low Battery

The low battery annunciator turns on when supply voltage between V^- and V^+ drops below 6.8V. The internal zener diode has a threshold of 6.3V. When the supply voltage drops below 6.8V, the transistor tied to V^- turns off pulling the “Low Battery” point high.

4.15 Sequence and Results Counter

A sequence counter and associated control logic provide signals that operate the analog switches in the integrator section. The comparator output from the integrator gates the results counter. The results counter is a six-section up/down decade counter that holds the intermediate results from each successive integration.

4.16 Overrange and Underrange Outputs

When the results counter holds a value greater than $\pm 19,999$, the DP_4/OR output (Pin 20) is driven high. When the results counter value is less than ± 1000 , the DP_3/UR output (Pin 21) is driven high. Both signals are valid on the falling edge of $\overline{LATCH}/\overline{HOLD}$ ($\overline{L}/\overline{H}$) and do not change until the end of the next conversion cycle. The signals are updated at the end of each conversion, unless the $\overline{L}/\overline{H}$ input (Pin 22) is held high. Pins 20 and 21 can also be used as inputs for external control of decimal points 3 and 4. Figure 4-14 shows a schematic of the input/output nature of these pins.

4.17 LATCH/Hold

The $\overline{L}/\overline{H}$ output goes low during the last 100 cycles of each conversion. This pulse latches the conversion data into the display driver section of the TC7129. This pin can also be used as an input. When driven high, the display will not be updated; the previous reading is displayed. When driven low, the display reading is not latched; the sequence counter reading will be displayed. Since the counter is counting much faster than the backplanes are being updated, the reading shown in this mode is somewhat erratic.

4.18 Display Driver

The TC7129 drives a triplexed LCD with three backplanes. The LCD can include decimal points, polarity sign and annunciators for continuity and low battery. Figure 4-16 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 1200. This results in a backplane drive frequency of 100 Hz for 60 Hz operation (120 kHz crystal) and 83.3 Hz for 50 Hz operation (100 kHz crystal).

Backplane waveforms are shown in Figure 4-17. These appear on outputs BP_1 , BP_2 , BP_3 (pins 16, 17 and 18). They remain the same, regardless of the segments being driven.

Other display output lines (pins 4 through 15) have waveforms that vary depending on the displayed values. Figure 4-18 shows a set of waveforms for the A, G, D outputs (pins 5, 8, 11 and 14) for several combinations of “ON” segments.

The ANNUNCIATOR DRIVE output (pin 3) is a square wave, running at the backplane frequency (100 Hz or 83.3 Hz) with a peak-to-peak voltage equal to DGND voltage. Connecting an annunciator to pin 3 turns it on; connecting it to its backplane turns it off.



Figure 4-16: Display Segment Assignments.

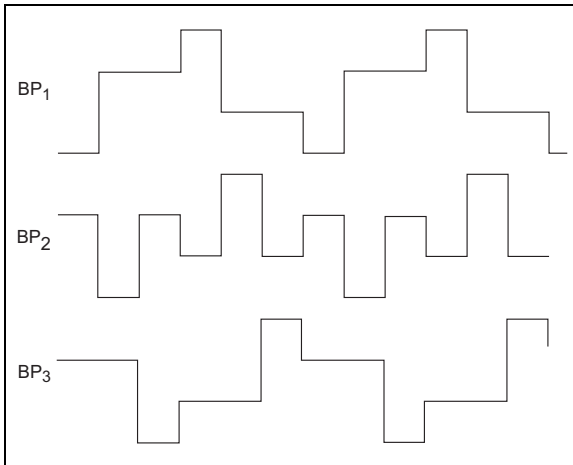


Figure 4-17: Backplane Waveforms.

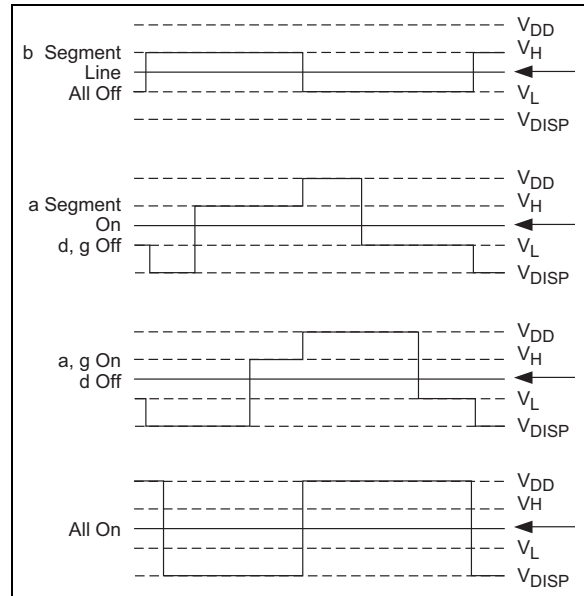


Figure 4-18: Typical Display Output Waveforms.

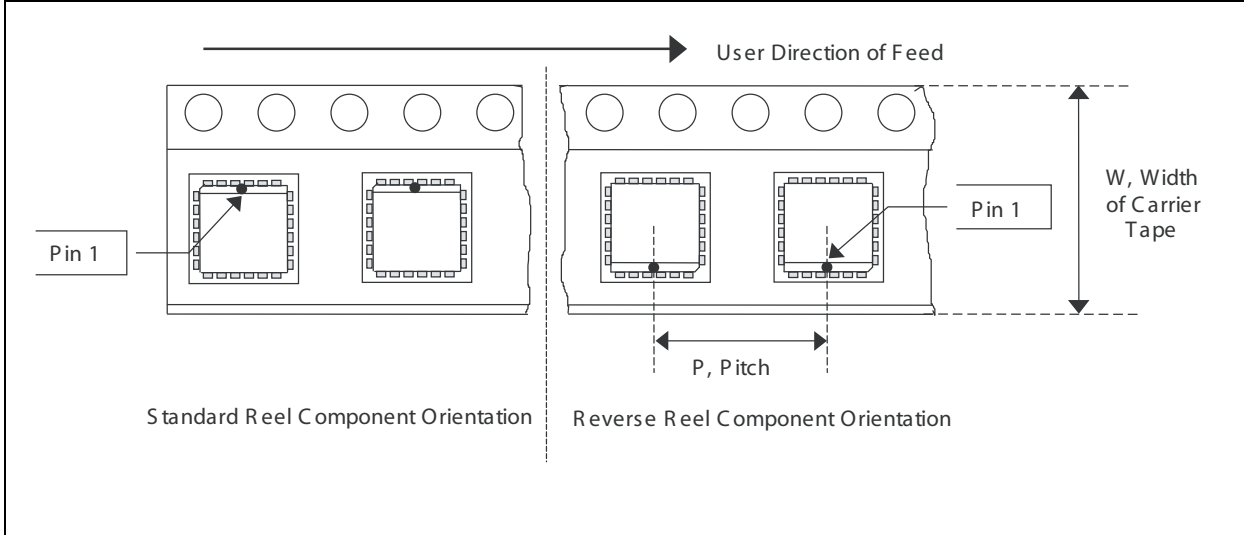
TC7129

5.0 PACKAGING INFORMATION

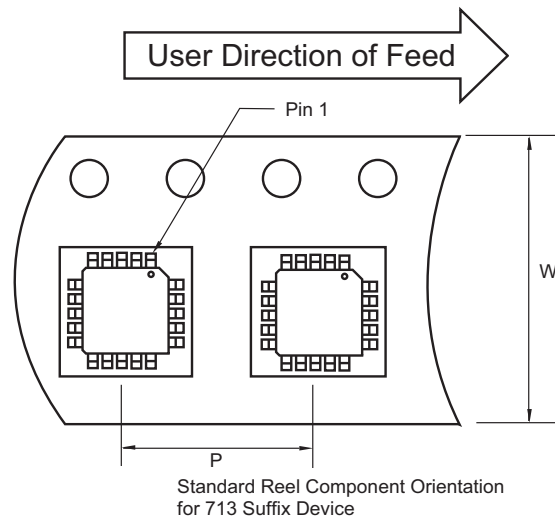
5.1 Package Marking Information

Package marking data not available a this time.

5.2 Taping Forms



Component Taping Orientation for 44-Pin PQFP Devices



Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

Note: Drawing does not represent total number of pins.

40-Lead Plastic Dual In-line (P) – 600 mil Body (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	40			40		
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.530	.545	.560	13.46	13.84	14.22
Overall Length	D	2.045	2.058	2.065	51.94	52.26	52.45
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-011

Drawing No. C04-016

TC7129

44-Lead Plastic Leaded Chip Carrier (LW) – Square (PLCC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	44			44		
Pitch	p		.050			1.27	
Pins per Side	n1		11			11	
Overall Height	A	.165	.173	.180	4.19	4.39	4.57
Molded Package Thickness	A2	.145	.153	.160	3.68	3.87	4.06
Standoff §	A1	.020	.028	.035	0.51	0.71	0.89
Side 1 Chamfer Height	A3	.024	.029	.034	0.61	0.74	0.86
Corner Chamfer 1	CH1	.040	.045	.050	1.02	1.14	1.27
Corner Chamfer (others)	CH2	.000	.005	.010	0.00	0.13	0.25
Overall Width	E	.685	.690	.695	17.40	17.53	17.65
Overall Length	D	.685	.690	.695	17.40	17.53	17.65
Molded Package Width	E1	.650	.653	.656	16.51	16.59	16.66
Molded Package Length	D1	.650	.653	.656	16.51	16.59	16.66
Footprint Width	E2	.590	.620	.630	14.99	15.75	16.00
Footprint Length	D2	.590	.620	.630	14.99	15.75	16.00
Lead Thickness	c	.008	.011	.013	0.20	0.27	0.33
Upper Lead Width	B1	.026	.029	.032	0.66	0.74	0.81
Lower Lead Width	B	.013	.020	.021	0.33	0.51	0.53
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

Notes:

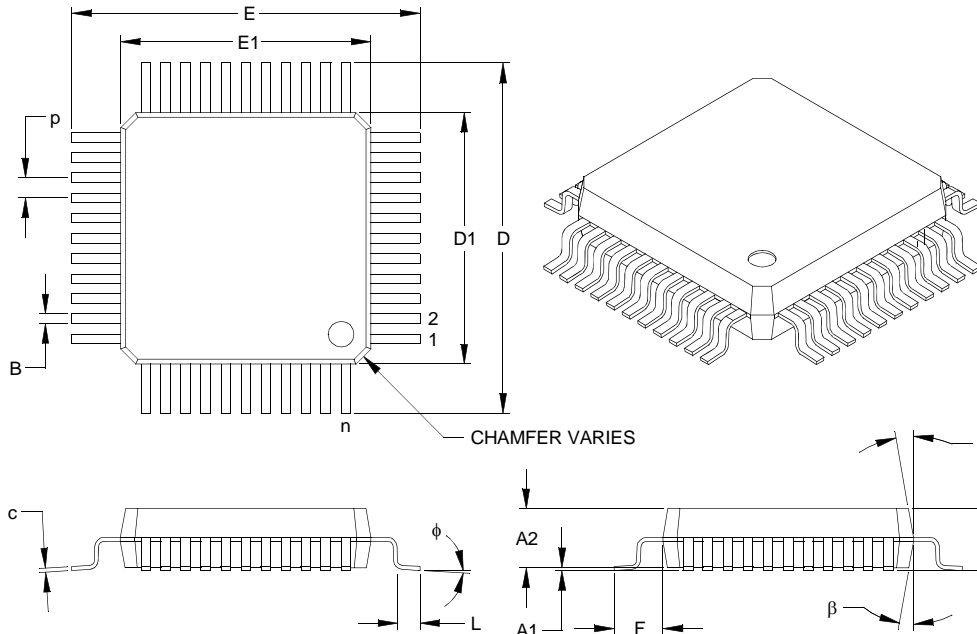
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-047

Drawing No. C04-048

44-Lead Plastic Quad Flatpack (KW) 10x10x2.0 mm Body, 1.95/0.25 mm Lead Form (PQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	P	.031 BSC			0.80 BSC		
Overall Height	A	-	-	.096	-	-	2.45
Molded Package Thickness	A2	.077	.079	.083	1.95	2.00	2.10
Standoff §	A1	.010	-	-	0.25	-	-
Foot Length	L	.029	.035	.041	0.73	0.88	1.03
Footprint	F	.077 REF.			1.95 REF.		
Foot Angle	φ	0°	3.5°	7°	0°	3.5°	7°
Overall Width	E	.547 BSC			13.90 BSC		
Overall Length	D	.547 BSC			13.90 BSC		
Molded Package Width	E1	.394 BSC			10.00 BSC		
Molded Package Length	D1	.394 BSC			10.00 BSC		
Lead Thickness	c	.004	-	.009	0.11	-	0.23
Lead Width	B	.012	-	.018	0.30	-	0.45
Mold Draft Angle Top	α	5°	-	16°	5°	-	16°
Mold Draft Angle Bottom	β	5°	-	16°	5°	-	16°

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.

See ASME Y14.5M

JEDEC Equivalent: MO-112 AA-1

Drawing No. C04-119

Revised 07-21-05

6.0 REVISION HISTORY

Revision E (December 2012)

Added a note to each package outline drawing.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>XX</u>	<u>XX</u>
Device	Temp.	Pkg	Taping Direction
Device:	DSTEMP: 4-1/2 Digit Analog-to-Digital Converter		
Temperature:	C = 0°C to +70°C I = -25°C to +85°C		
Package:	PL = 40-Pin PDIP KW = 40-Pin PQFP LW = 44-Pin PLCC JL = 40-Pin CDIP		
Taping Direction:	713 = Standard Taping		
Examples:			
a) TC7129CPL: 40-Pin PDIP			
b) DSTEMPCKW713: 44-Pin PQFP Tape and Reel			
c) DSTEMPCLW: 44-Pin PLCC			

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under "Support", click on "Customer Change Notification" and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: Technical Publications Manager Total Pages Sent _____

RE: Reader Response

From: Name _____

Company _____

Address _____

City / State / ZIP / Country _____

Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? Y N

Device:

Literature Number: DS21459E

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC³² logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2002-2012, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 9781620768389

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC[®] MCUs and dsPIC[®] DSCs, KEELOQ[®] code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7828
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

11/29/12