PT5161L PCI Express® Gen-5 and Compute Express Link™ x16 Low-Latency Smart Retimer

1 Benefits and Features

- Compatible with PCI Express® Gen-5/4/3/2/1 and Compute Express Link™
- 32 GT/s, 16 GT/s, 8 GT/s, 5 GT/s, and 2.5 GT/s Data Rates with Automatic Link Equalization
- Low-Latency Mode Enables Cache-Coherent Links
- 16 Lanes with Flexible Link Bifurcation Including 1x16, 2x8, 4x4, 8x2, and Others
- Extends Reach by >36 dB at 32 GT/s Enabling Low-Cost PCB Materials and Connectors
- Receiver and Transmitter Performance Exceeds PCIe® Base Specification Requirements
- No System Software Required
- BGA Package Footprint Optimized for Board Routing
- Integrated AC-Coupling Capacitors Reduce Solution Size and Improves Signal Integrity Performance
- Supports SRIS, SRNS, and Common Clock Systems
- Supports Hot Plug and Hot Un-Plug
- Supports Lane Margining at the Receiver for Both Timing and Voltage
- Supports Slave Loopback
- Supports Systems with Lane Reversal and Implements Automatic Polarity Correction
- HCSL Reference Clock Output Eliminates Clock Buffers to Drive Downstream PCIe Components
- Advanced In-Band and Out-of-Band Diagnostics for Fleet Management, Large-Scale Server Deployments
- Full-Featured C and Python SDKs for Rapid Integration of Advanced Diagnostics Features
- Device Configuration through SMBus or EEPROM
- IEEE 1149.6 AC-JTAG Boundary Scan
- Full Portfolio of Pin- and Register-Compatible Retimers Enables Easy Performance Scaling Between CXL and PCIe Gen-4 and Gen-5

2 Applications

- Server and High-Performance PC Motherboards
- PCIe Riser and Add-in Cards
- NVMe JBOFs, GPU/Deep-Learning Accelerators

Product Family Information – x16, x8

Part #	CXL/PCIe	Lanes	Body Size (Nom)
PT5161LR	PCIe 5.0	16	8.9 mm x 22.8 mm
PT5161LX	CXL / PCIe 5.0	16	8.9 mm x 22.8 mm
PT4161LR	PCIe 4.0	16	8.9 mm x 22.8 mm
PT5081LR	PCIe 5.0	8	8.5 mm x 13.4 mm
PT5081LX	CXL / PCIe 5.0	8	8.5 mm x 13.4 mm
PT4080LR	PCIe 4.0	8	8.5 mm x 13.4 mm

3 Description

The PT5161L is a 16-Lane PCI Express® (PCIe®) Gen-5 and Compute Express Link™ (CXL™) protocol-aware low-latency Retimer designed to integrate seamlessly between a Root Complex and End Point(s) extending the reach by 36 dB at 32 GT/s. Compliant to all PCIe 5.0 rates and Retimer functional requirements, the PT5161L enables more system topologies and lower total solution cost while minimizing implementation overhead and Bill of Materials (BoM).

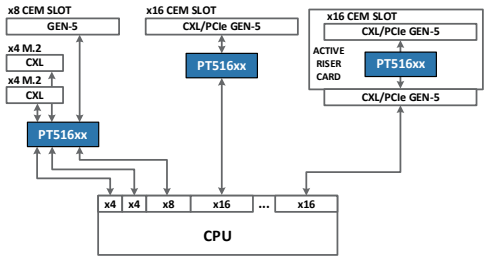
The innovative protocol-non-disruptive low-latency architecture of PT5161L significantly reduces latency through the Retimer while being transparent to system software and participating in Link Equalization with the Root Complex and End Point(s) to optimize Link performance. The PT5161L can autonomously adapt its latency to maximize performance during normal operational Link state (L0) while maintaining protocol interoperation.

To support a wide variety of End Points and port configurations, the PT5161L can bifurcate to one x16 Link, two x8 Links, four x4 Links, eight x2 Links, and more. Each Link operates independently, and per-Link diagnostics information such as Link state history and electrical margin are accessible through in-band (Receiver margining) and out-of-band (SMBus) methods.

The PT5161L uses a standard PCIe 100-MHz HCSL input clock and provides a 100-MHz HCSL output clock to drive other Retimer devices or PCIe components in the system.

The pinout is based on the Intel Retimer Supplemental Specification and uses an 8.9-mm x 22.8-mm Flip-Chip CSP package. The pinout allows for separate single-layer routing for all high-speed transmit and receive signals. Compact design, minimal supporting circuitry, and integrated AC-coupling capacitors greatly reduces overall solution size, making the PT5161L ideal for space-restricted applications like system boards and riser cards.

Typical Application Block Diagram



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4 Revision History

Revision	Date	Changes
-	March 2021	• Original Product Brief

5 Package, Mechanical, and Orderable Information

5.1 Package Outline Drawing

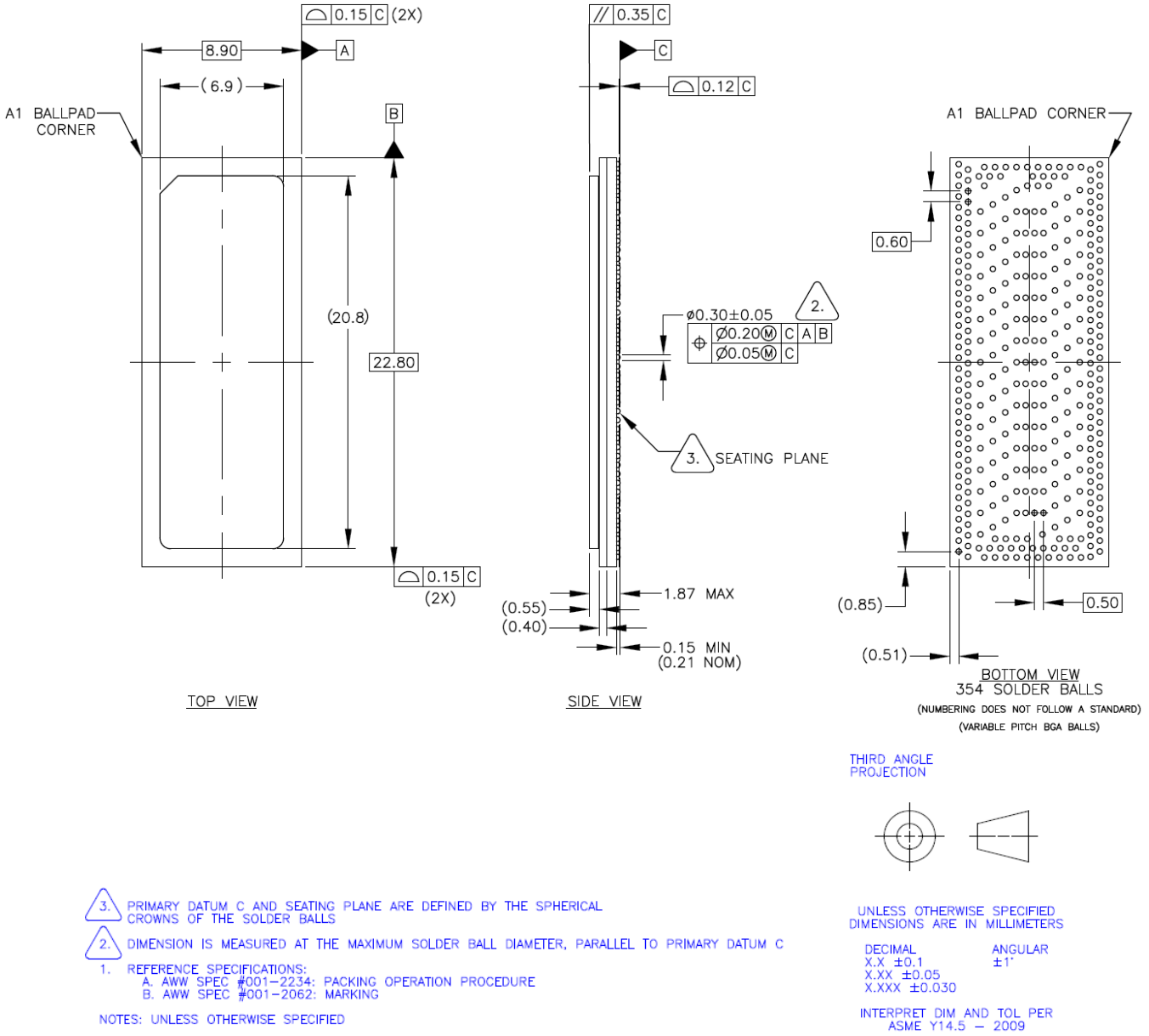

Figure 5-1: Package Outline Drawing

Table 5-1: Package Dimensions

Parameter	Conditions	Min	Typ	Max	Unit
Package width		8.85	8.90	8.95	mm
Package length		22.75	22.80	22.85	mm
Package thickness	Prior to BGA compression	1.55	1.71	1.87	mm

5.2 Package Land Pattern

Figure 5-2 shows the top view of the platform-side land pattern for the PT5161L.

NOTE: Refer to "Astera_Labs_PTx16xx_supplemental_info.xlsx" for detailed land pad coordinates, sizes, and rotation.

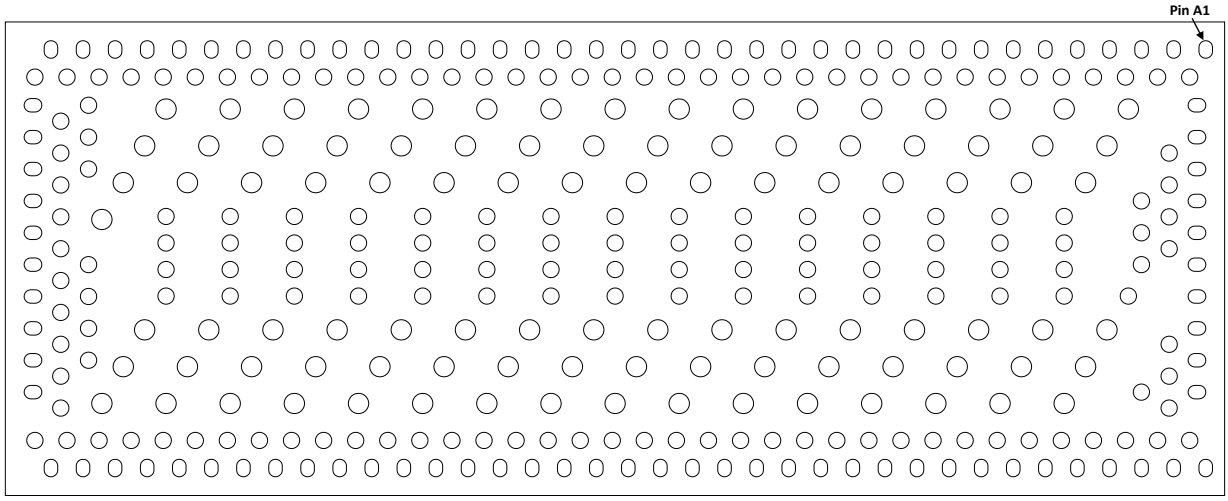

Figure 5-2: Package Land Pattern

5.3 Package Solder Mask Stencil

Astera Labs recommends keeping the solder paste aperture the same size as the land pads, shown in Figure 5-2 and using metal-defined (MD) pads rather than solder-mask-defined (SMD) pads.

5.4 Reflow Profile

Astera Labs recommends an assembly reflow profile consistent with lead-free assembly as outlined in the IPC/JEDEC J-STD-020E standard. Table 5-2 provides a rough guideline, however specific parameters such as peak temperature, peak temperature duration may need to be adjusted based on other system components.

Table 5-2: Guideline Lead-Free Assembly Reflow Parameters

Profile Feature	Lead-Free Assembly	Units
Ramp-up rate	1.5 to 3	°C / second
Preheat temperature	25 to 183	°C
Preheat time	150	seconds
Time maintained above T_L	70 to 80	seconds
T_L	221	°C
Peak temperature	250 to 255	°C
Time within 5 °C of peak temperature	20 to 30	seconds
Ramp-down rate (T_{peak} to T_L)	3	°C / second
Time from 25 °C to peak temperature	4	minutes

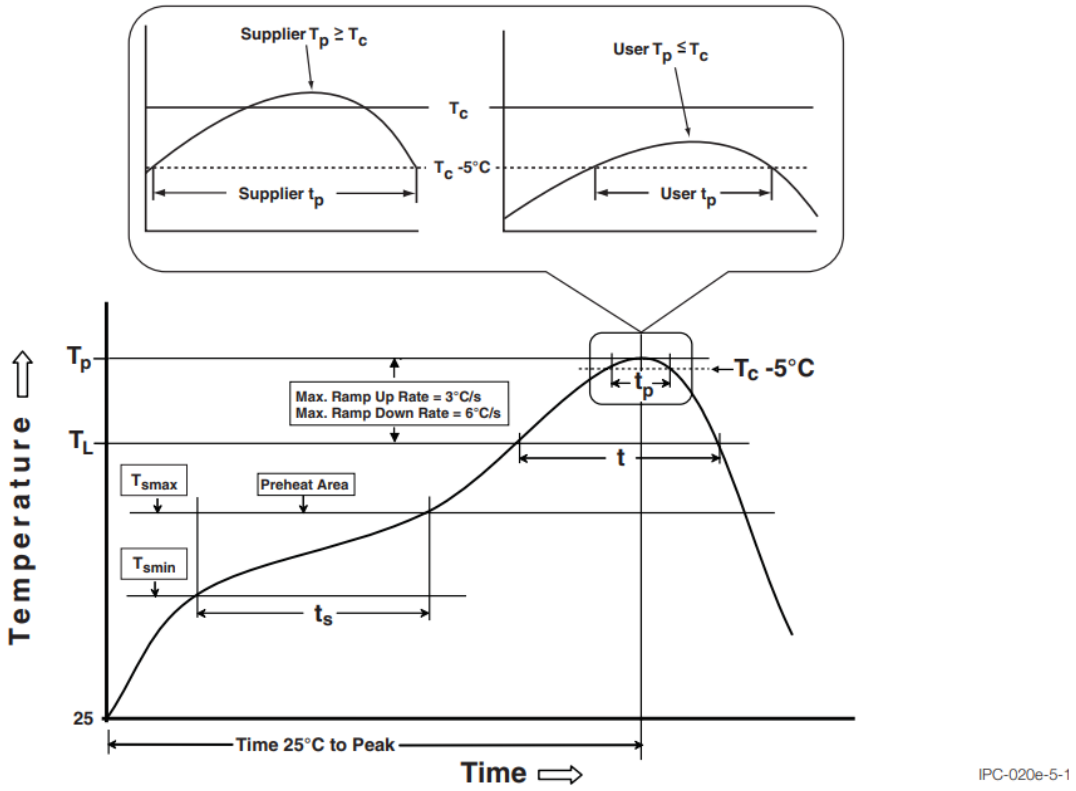

Figure 5-3: Reflow Profile from IPC/JEDEC J-STD-020E (Not to Scale)

5.5 Orderable Information

Table 5-3: Device Orderable Information

Base Part Number	Orderable Part Number	Package	Maximum PCIe Gen(1)	PCIe Lanes	Integrated AC Coupling Capacitors	Operating Junction Temperature	Pack Quantity	Top Marking(2)	Eco Status(3)	MSL Peak Temp(4)	Production Status
PT5161L	PT5161LC	354-pin FC-CSP	Gen-5, CXL	x16	Yes	-10 °C to 110 °C	N/A		EU-RoHS, Halogen-Free	Level-3-260C-168 HR	Pre-production(5)
	PT5161LRS	354-pin FC-CSP	Gen-5	x16	Yes	-10 °C to 110 °C	240		EU-RoHS, Halogen-Free	Level-3-260C-168 HR	(6)
	PT5161LRL	354-pin FC-CSP	Gen-5	x16	Yes	-10 °C to 110 °C	2400		EU-RoHS, Halogen-Free	Level-3-260C-168 HR	(6)
	PT5161LXS	354-pin FC-CSP	Gen-5, CXL	x16	Yes	-10 °C to 110 °C	240		EU-RoHS, Halogen-Free	Level-3-260C-168 HR	(6)
	PT5161LXL	354-pin FC-CSP	Gen-5, CXL	x16	Yes	-10 °C to 110 °C	2400		EU-RoHS, Halogen-Free	Level-3-260C-168 HR	(6)

(1) Astera Labs products support 100% backwards compatibility to earlier PCIe generations, unless otherwise noted.
(2) YYWW is a date code, ######### is a lot trace code. There may be additional marking, which relates to the logo or the lot trace code.
(3) Astera Labs defines “EU-RoHS” to mean products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. Astera Labs defines “Halogen-Free” to mean semiconductor products that are compliant with JS709B low-halogen requirements of ≤1000 ppm threshold.
(4) Moisture Sensitivity Level rating according to the JEDEC industry standard classifications and peak solder temperature.
(5) Astera Labs defines “Pre-production” as the final product revision which is undergoing full production qualification; and “Production” as the final product revision which has been qualified per applicable JEDEC standards.
(6) For availability, please contact info@AsteraLabs.com for more details.