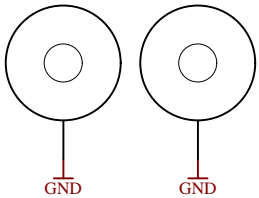
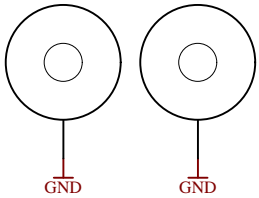


- FPGA-MISC
- FPGA-POWER
- B13
- B34
- B35
- MIO-BANKS
- MGT
- DDR-BANK
- B13.SchDoc
- B34.SchDoc
- B35.SchDoc
- MIO-BANKS.SchDoc
- MGT.SchDoc
- DDR-BANK.SchDoc
- FPGA-POWER.SchDoc
- DDR3-RAM
- B2B_Connector
- Clock
- ETH-PHY
- USB-PHY
- POWER
- POWER_2
- DDR3-RAM.SchDoc
- B2B_Connector.SchDoc
- Clock.SchDoc
- ETH-PHY.SchDoc
- USB-PHY.SchDoc
- POWER.SchDoc
- POWER_2.SchDoc

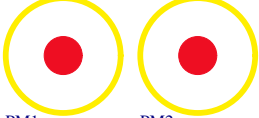
Mount.Hole 3.2mm Mount.Hole 3.2mm



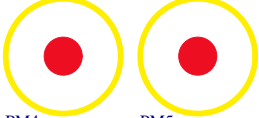
Mount.Hole 3.2mm Mount.Hole 3.2mm



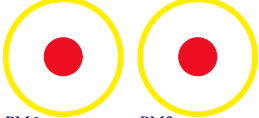
FIDU-DOT - small FIDU-DOT - small



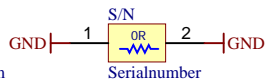
PM1 FIDU-DOT - small PM2 FIDU-DOT - small



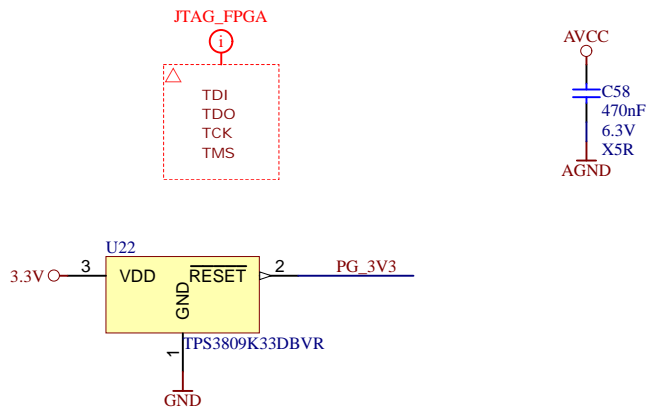
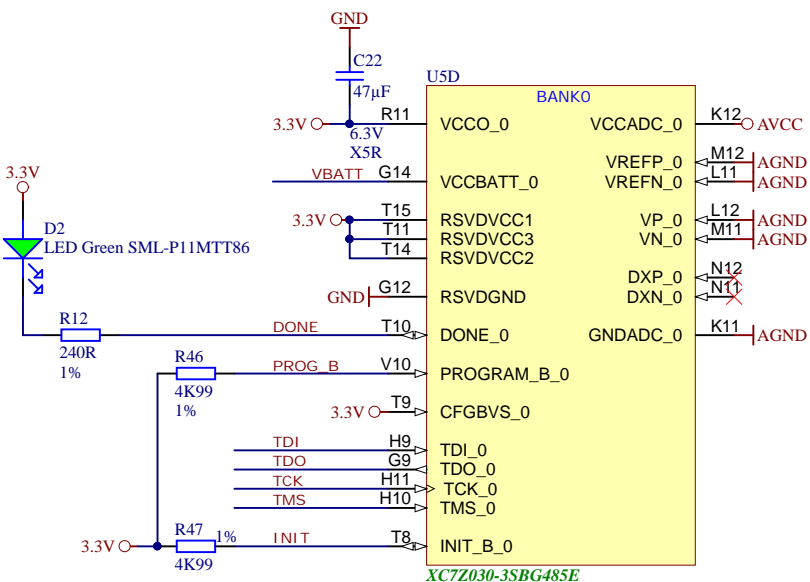
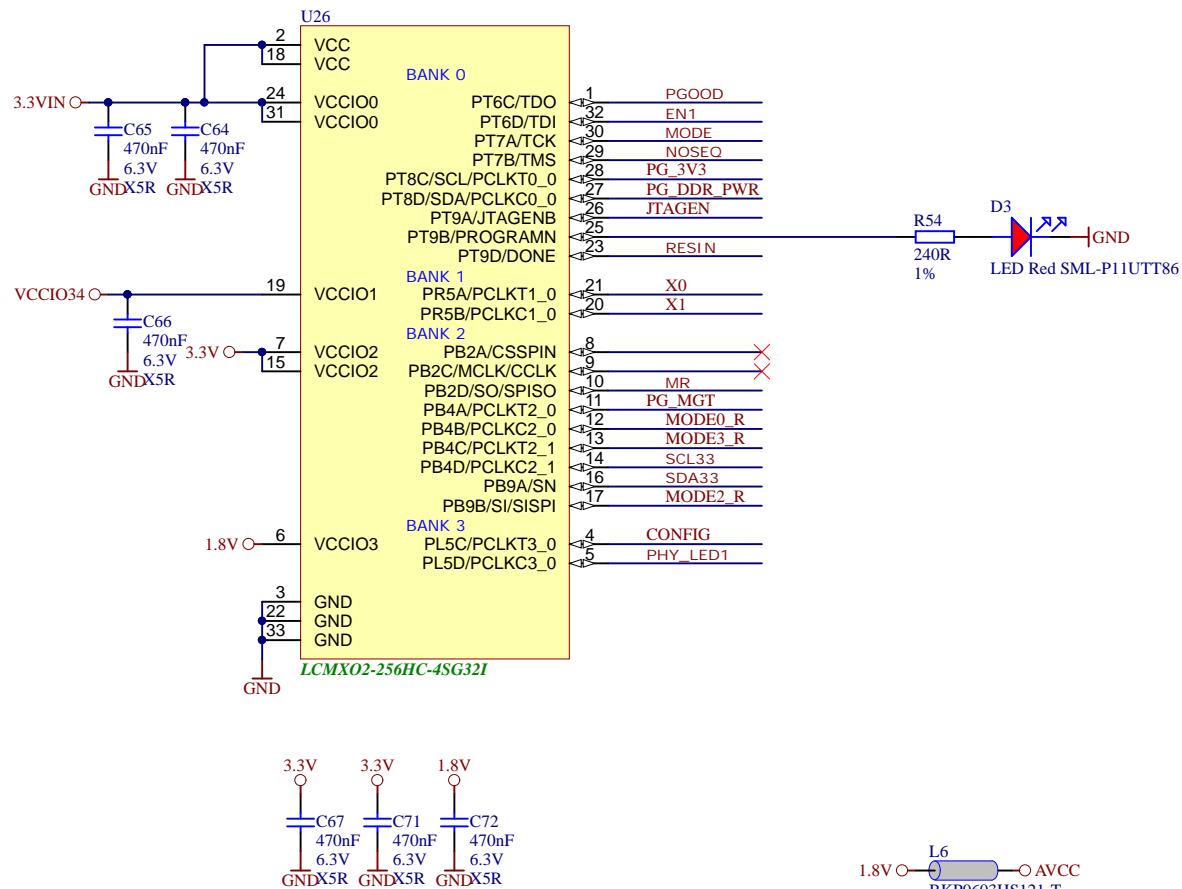
PM4 FIDU-DOT - small PM5 FIDU-DOT - small




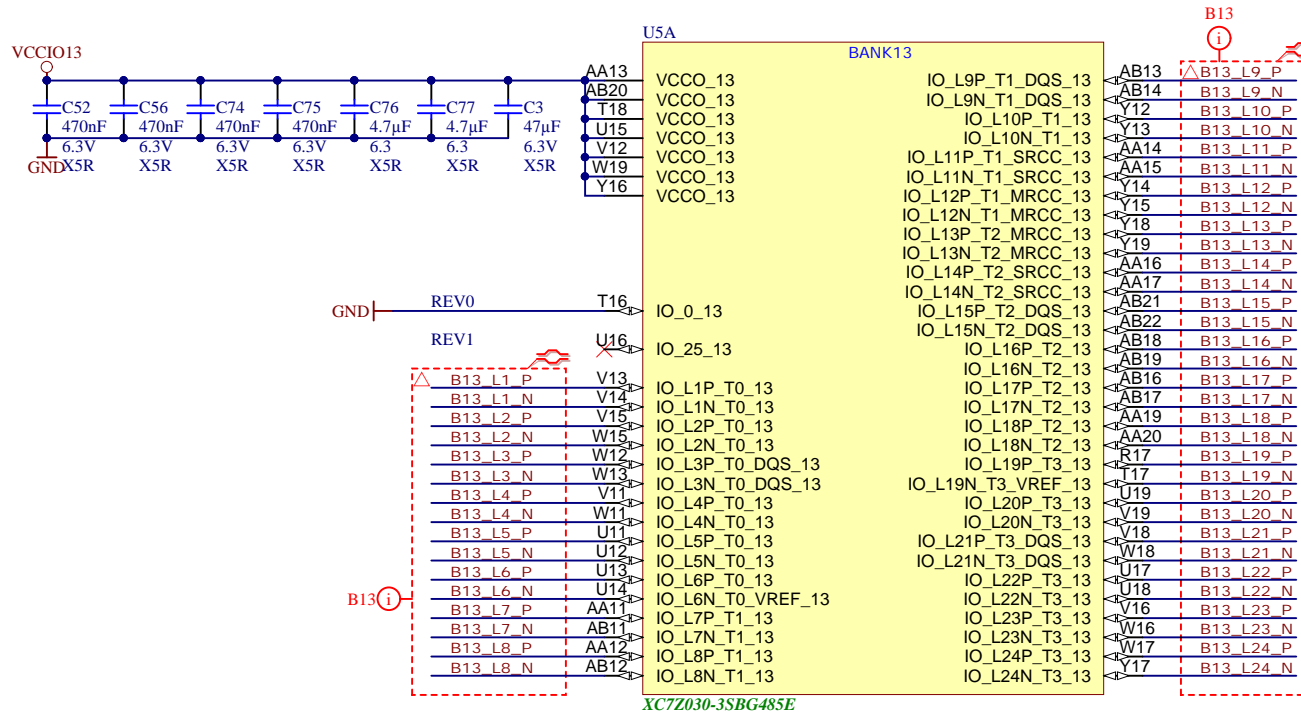
Serial
Serial
Serialnumber 6,3 x 6.3mm




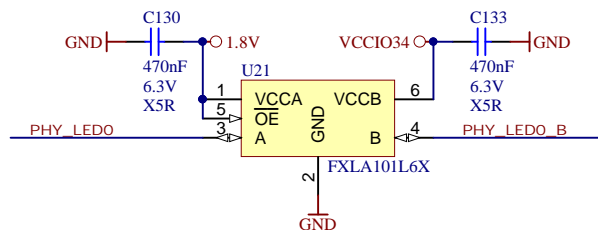
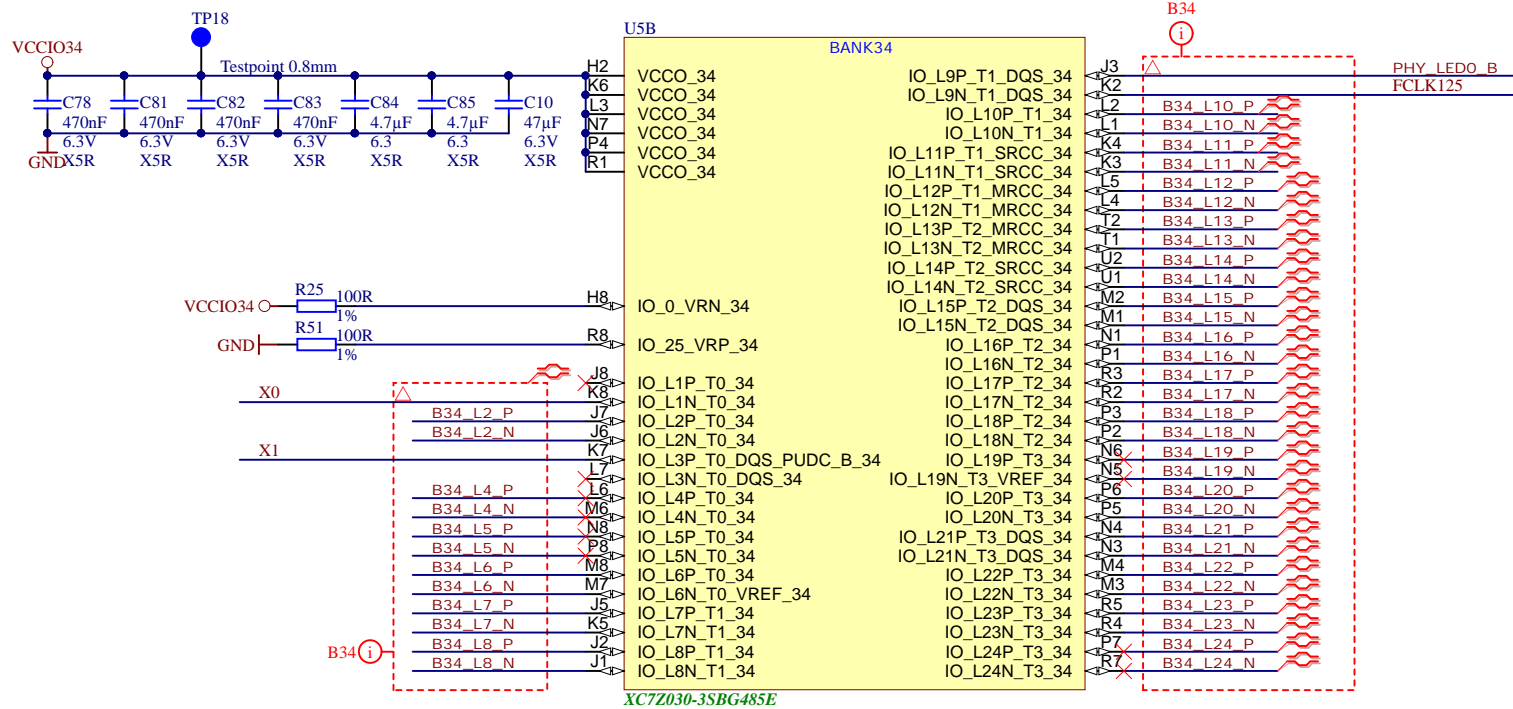
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| Title: TE0715 - Overview | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page1 of 15 |
| Filename: TE0715.SchDoc | | |



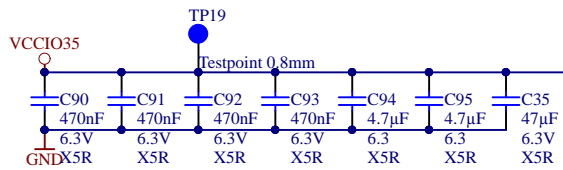
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| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 | | |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page2 | | of 15 |
| Filename: FPGA-MISC.SchDoc | | | | |



| | | | |
|---|--------------------------|---------------------------------------|-------------|
|  | Title: TE0715 - FPGA_B12 | | |
| | A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| | Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page3 of 15 |
| | Filename: B13.SchDoc | | |



| | | |
|--------------------------|---------------------------------------|-------------|
| Title: TE0715 - FPGA_B34 | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page4 of 15 |
| Filename: B34.SchDoc | | |

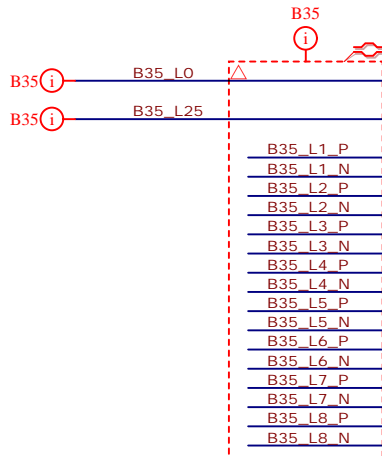


USC

BANK35

| | | | | |
|----|---------|-------------------------|----|-----------|
| A3 | VCCO_35 | IO_L9P_T1_DQS_AD3P_35 | A7 | B35_L9_P |
| C7 | VCCO_35 | IO_L9N_T1_DQS_AD3N_35 | A6 | B35_L9_N |
| D4 | VCCO_35 | IO_L10P_T1_AD11P_35 | A5 | B35_L10_P |
| E1 | VCCO_35 | IO_L10N_T1_AD11N_35 | A4 | B35_L10_N |
| F8 | VCCO_35 | IO_L11P_T1_SRCC_35 | C6 | B35_L11_P |
| G5 | VCCO_35 | IO_L11N_T1_SRCC_35 | C5 | B35_L11_N |
| | | IO_L12P_T1_MRCC_35 | D5 | B35_L12_P |
| | | IO_L12N_T1_MRCC_35 | C4 | B35_L12_N |
| | | IO_L13P_T2_MRCC_35 | B4 | B35_L13_P |
| | | IO_L13N_T2_MRCC_35 | B3 | B35_L13_N |
| | | IO_L14P_T2_AD4P_SRCC_35 | D3 | B35_L14_P |
| | | IO_L14N_T2_AD4N_SRCC_35 | C3 | B35_L14_N |
| | | IO_L15P_T2_DQS_AD12P_35 | A2 | B35_L15_P |
| | | IO_L15N_T2_DQS_AD12N_35 | A1 | B35_L15_N |
| | | IO_L16P_T2_35 | D1 | B35_L16_P |
| | | IO_L16N_T2_35 | C1 | B35_L16_N |
| | | IO_L17P_T2_AD5P_35 | E2 | B35_L17_P |
| | | IO_L17N_T2_AD5N_35 | D2 | B35_L17_N |
| | | IO_L18P_T2_AD13P_35 | B2 | B35_L18_P |
| | | IO_L18N_T2_AD13N_35 | B1 | B35_L18_N |
| | | IO_L19P_T3_35 | H4 | B35_L19_P |
| | | IO_L19N_T3_VREF_35 | H3 | B35_L19_N |
| | | IO_L20P_T3_AD6P_35 | G4 | B35_L20_P |
| | | IO_L20N_T3_AD6N_35 | F4 | B35_L20_N |
| | | IO_L21P_T3_DQS_AD14P_35 | F4 | B35_L21_P |
| | | IO_L21N_T3_DQS_AD14N_35 | E3 | B35_L21_N |
| | | IO_L22P_T3_AD7P_35 | G3 | B35_L22_P |
| | | IO_L22N_T3_AD7N_35 | G2 | B35_L22_N |
| | | IO_L23P_T3_35 | F2 | B35_L23_P |
| | | IO_L23N_T3_35 | F1 | B35_L23_N |
| | | IO_L24P_T3_AD15P_35 | H1 | B35_L24_P |
| | | IO_L24N_T3_AD15N_35 | G1 | B35_L24_N |

XC7Z030-3SBG485E

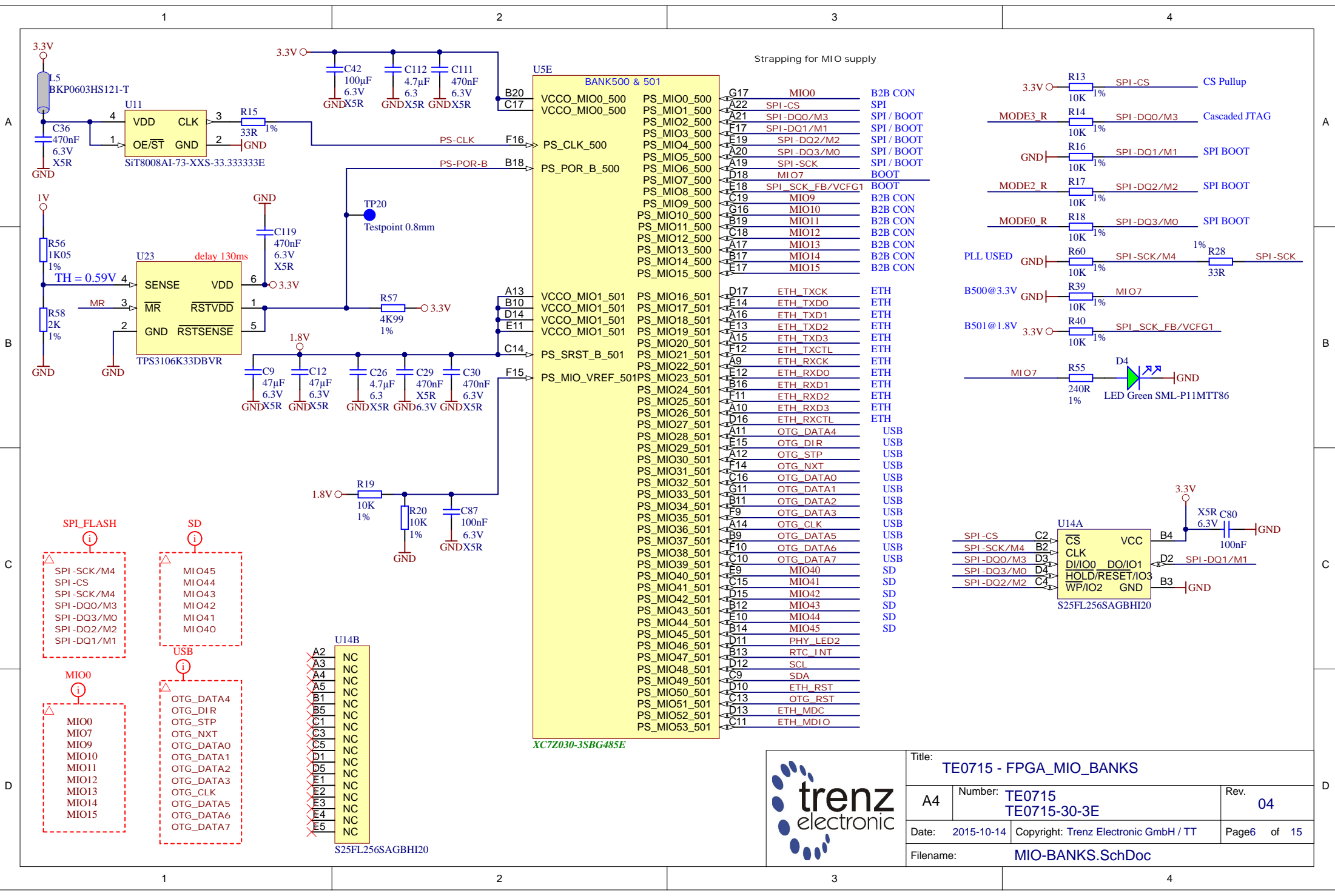


B35

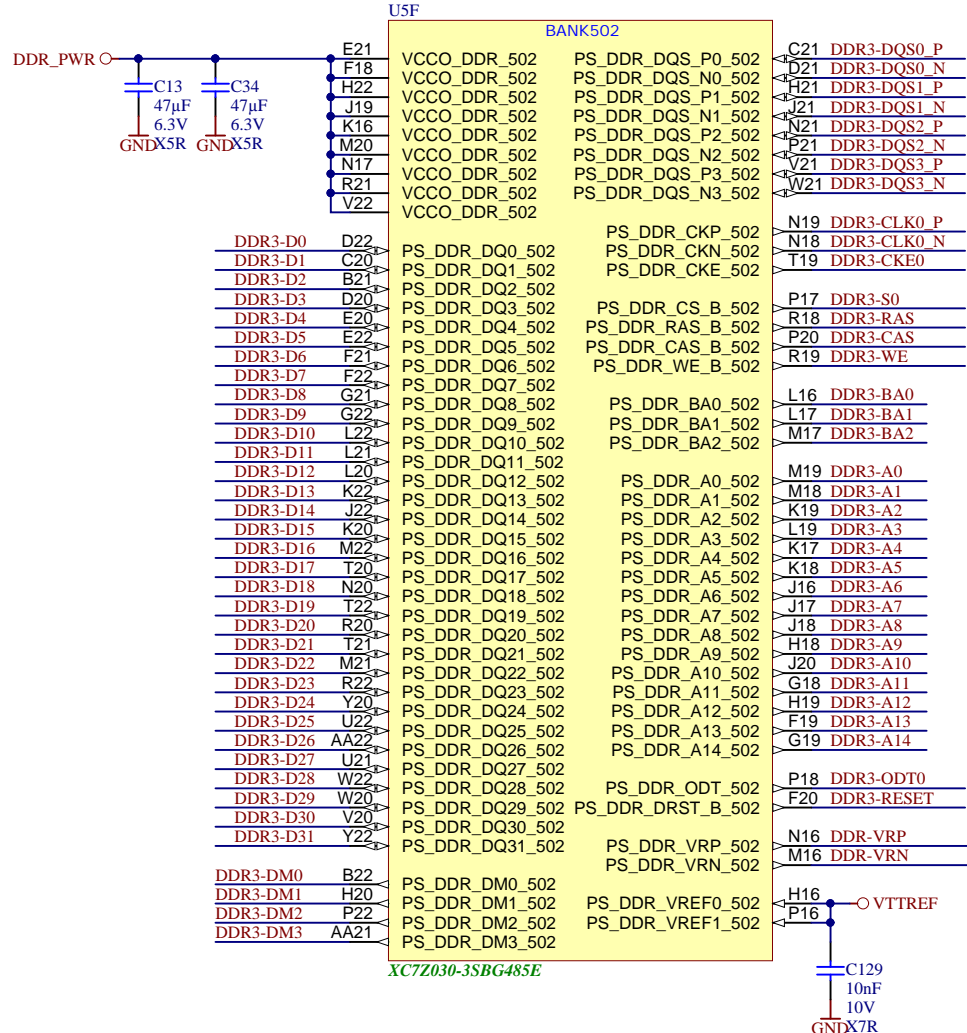

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|----|-----------|
| A7 | B35_L9_P |
| A6 | B35_L9_N |
| A5 | B35_L10_P |
| A4 | B35_L10_N |
| C6 | B35_L11_P |
| C5 | B35_L11_N |
| D5 | B35_L12_P |
| C4 | B35_L12_N |
| B4 | B35_L13_P |
| B3 | B35_L13_N |
| D3 | B35_L14_P |
| C3 | B35_L14_N |
| A2 | B35_L15_P |
| A1 | B35_L15_N |
| D1 | B35_L16_P |
| C1 | B35_L16_N |
| E2 | B35_L17_P |
| D2 | B35_L17_N |
| B2 | B35_L18_P |
| B1 | B35_L18_N |
| H4 | B35_L19_P |
| H3 | B35_L19_N |
| G4 | B35_L20_P |
| F4 | B35_L20_N |
| F4 | B35_L21_P |
| E3 | B35_L21_N |
| G3 | B35_L22_P |
| G2 | B35_L22_N |
| F2 | B35_L23_P |
| F1 | B35_L23_N |
| H1 | B35_L24_P |
| G1 | B35_L24_N |



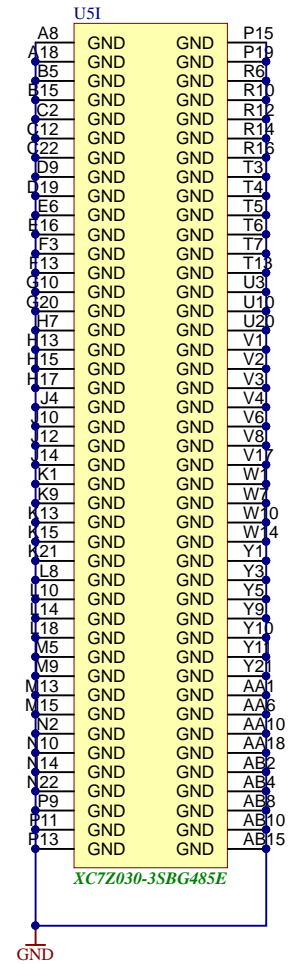
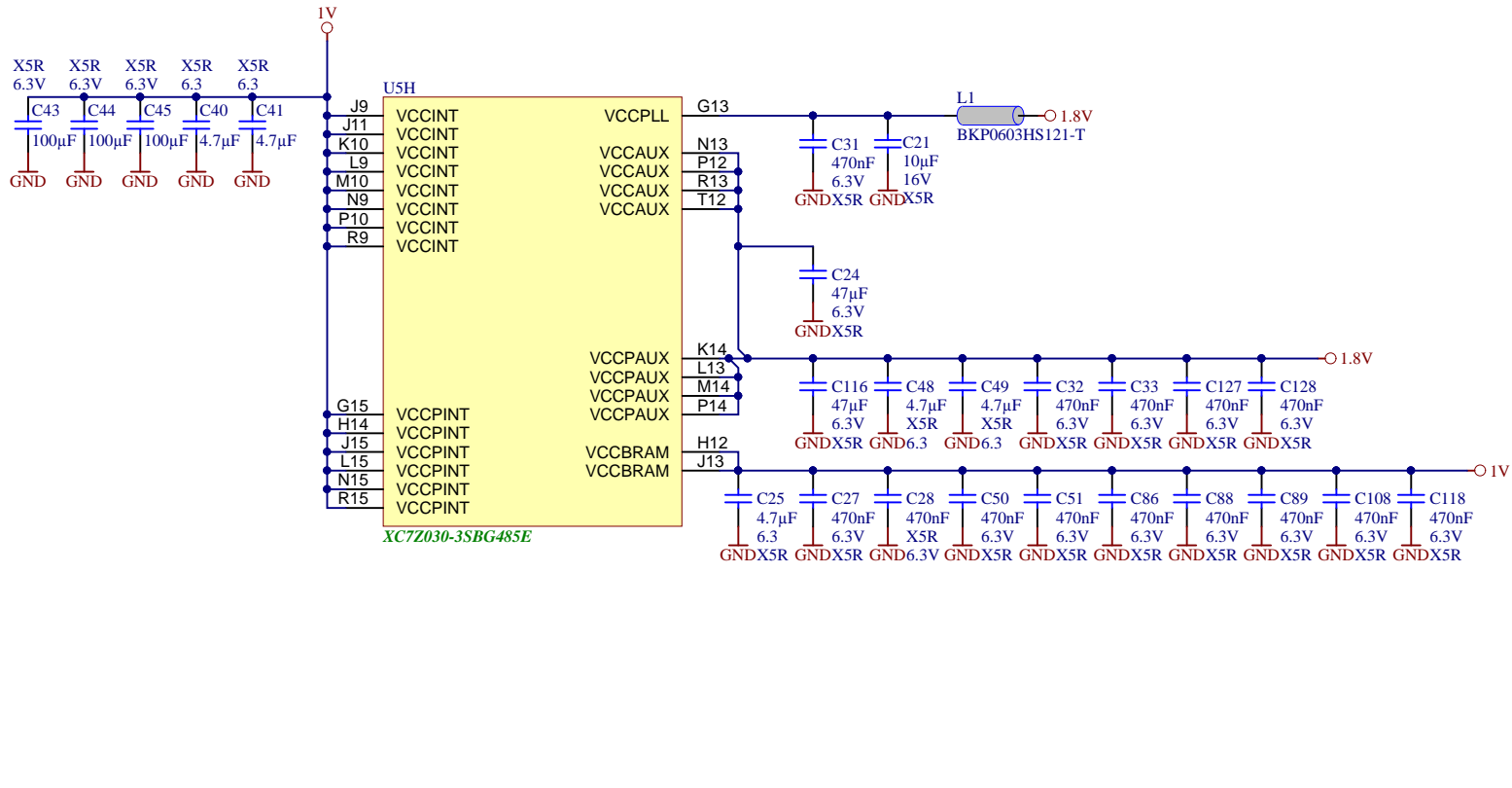
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| Title: TE0715 - FPGA_B35 | | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 | |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page5 | of 15 |
| Filename: B35.SchDoc | | | |



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|--------------------------------|---------------------------------------|--------------|
| Title: TE0715 - FPGA_MIO_BANKS | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page 6 of 15 |
| Filename: MIO-BANKS.SchDoc | | |

| | | |
|-----------------------------|---------------------------------------|--------------|
| Title: TE0715 - FPGA_PS-DDR | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page 7 of 15 |
| Filename: DDR-BANK.SchDoc | | |



| | | |
|-----------------------------|---------------------------------------|-------------|
| Title: TE0715 - FPGA_Power | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page8 of 15 |
| Filename: FGPA-POWER.SchDoc | | |

NOTE: B34 and B35 are HP Banks in 7030 Assembly with max 1.8V I/O Voltage

B13 48 IO, 24 LVDS Pairs
MIO0 8 IO, 3.3V
MIO1 6 IO 1.8V
ETH MDI Copper

B34 16 IO, 8 LVDS Pairs
USB OTG ETH SGMII
PLL CLK IN
GT CLK IN
GTP/GTX 4 Lanes

B34 18 IO, 9 LVDS Pairs
B35 48 IO, 24 LVDS Pairs
B35 2 IO

A

B

C

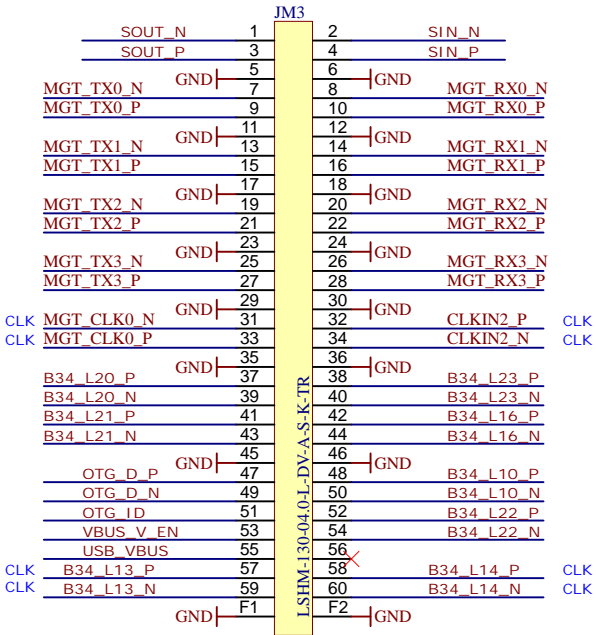
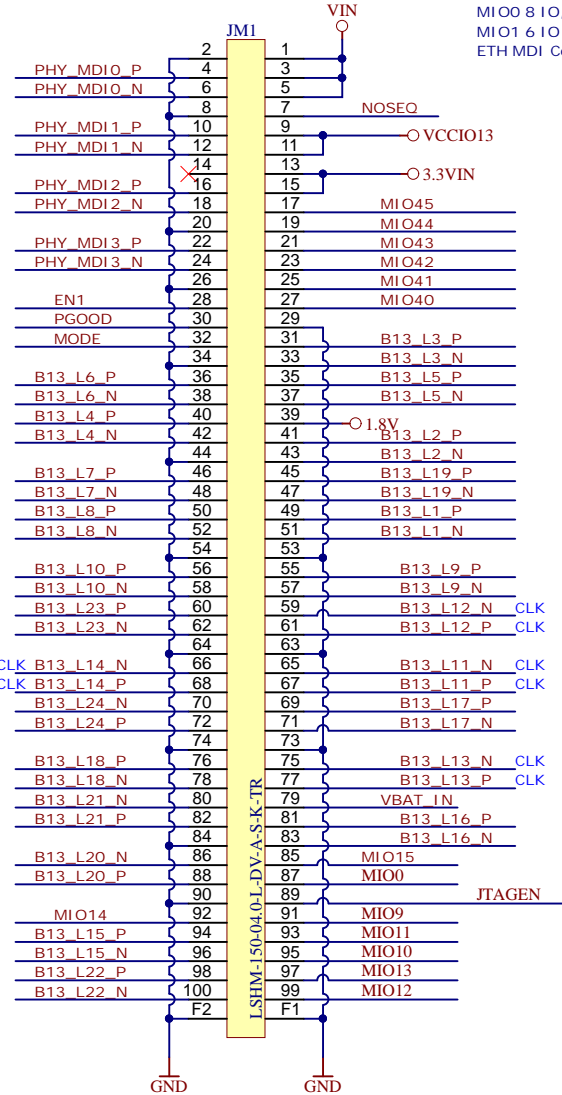
D

A

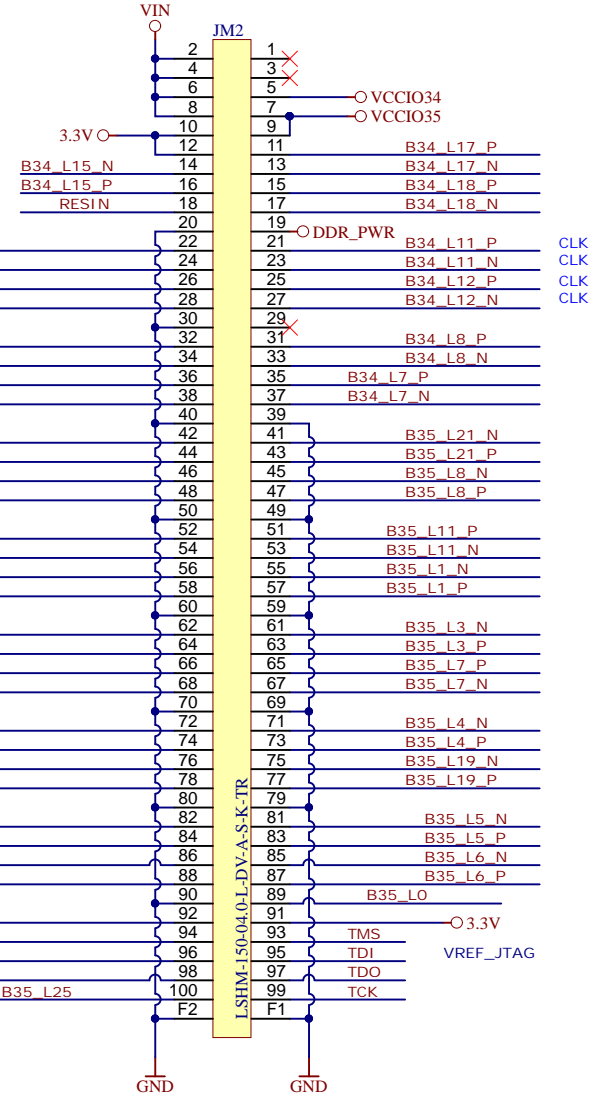
B

C

D



Top of Board



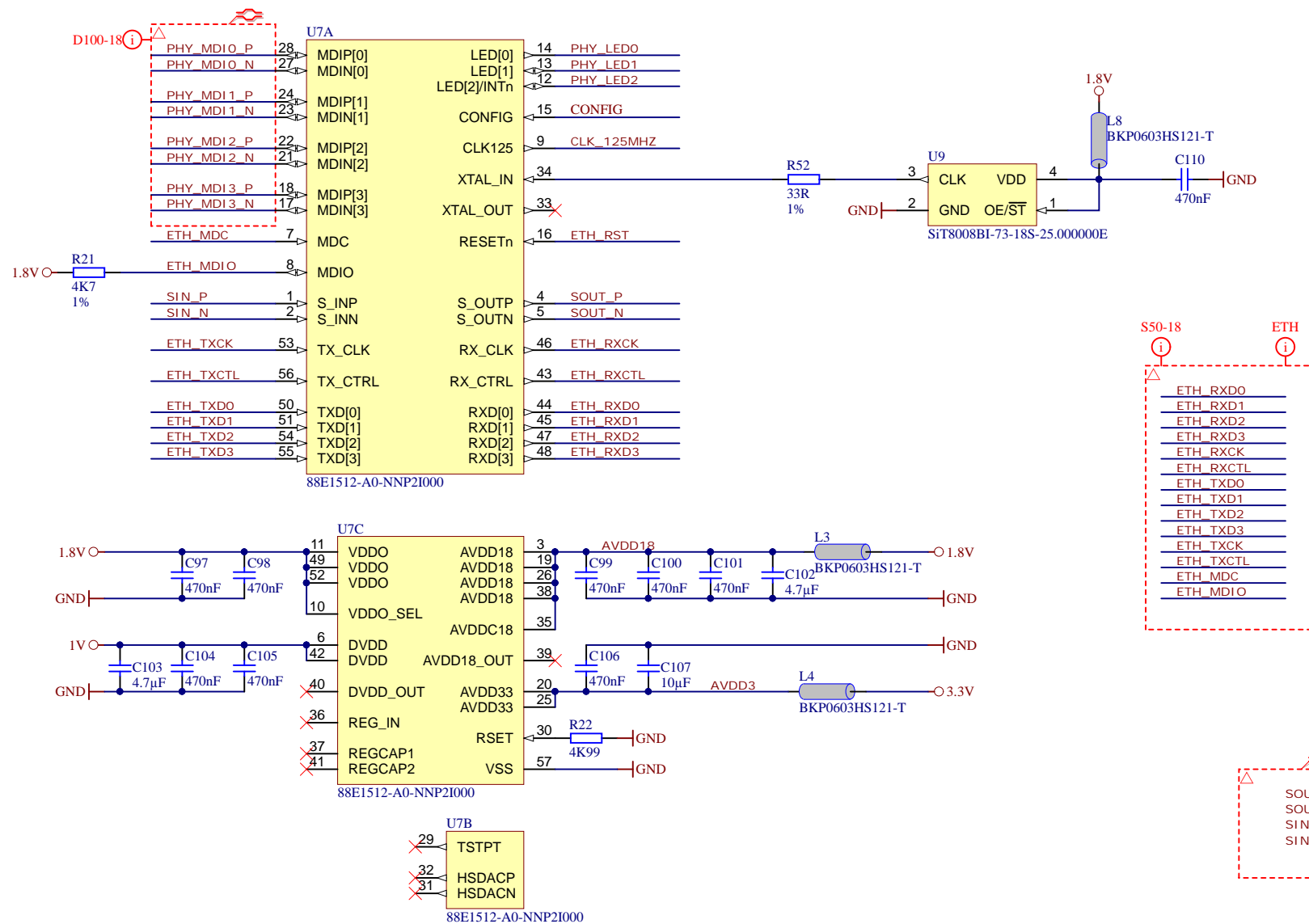
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| Title: TE0715 - B2B_Connectors | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page9 of 15 |
| Filename: B2B_Connector.SchDoc | | |

A

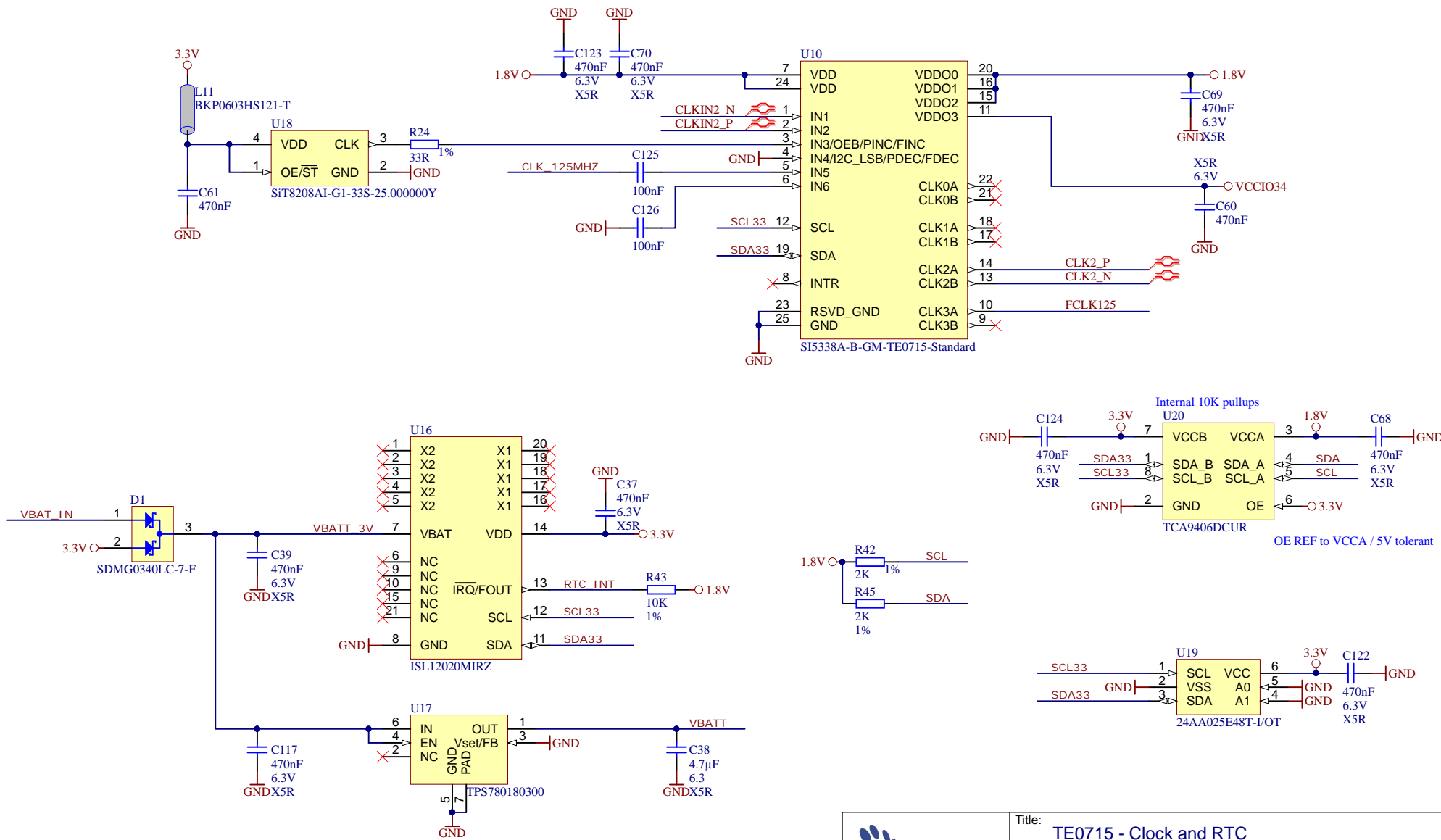
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C

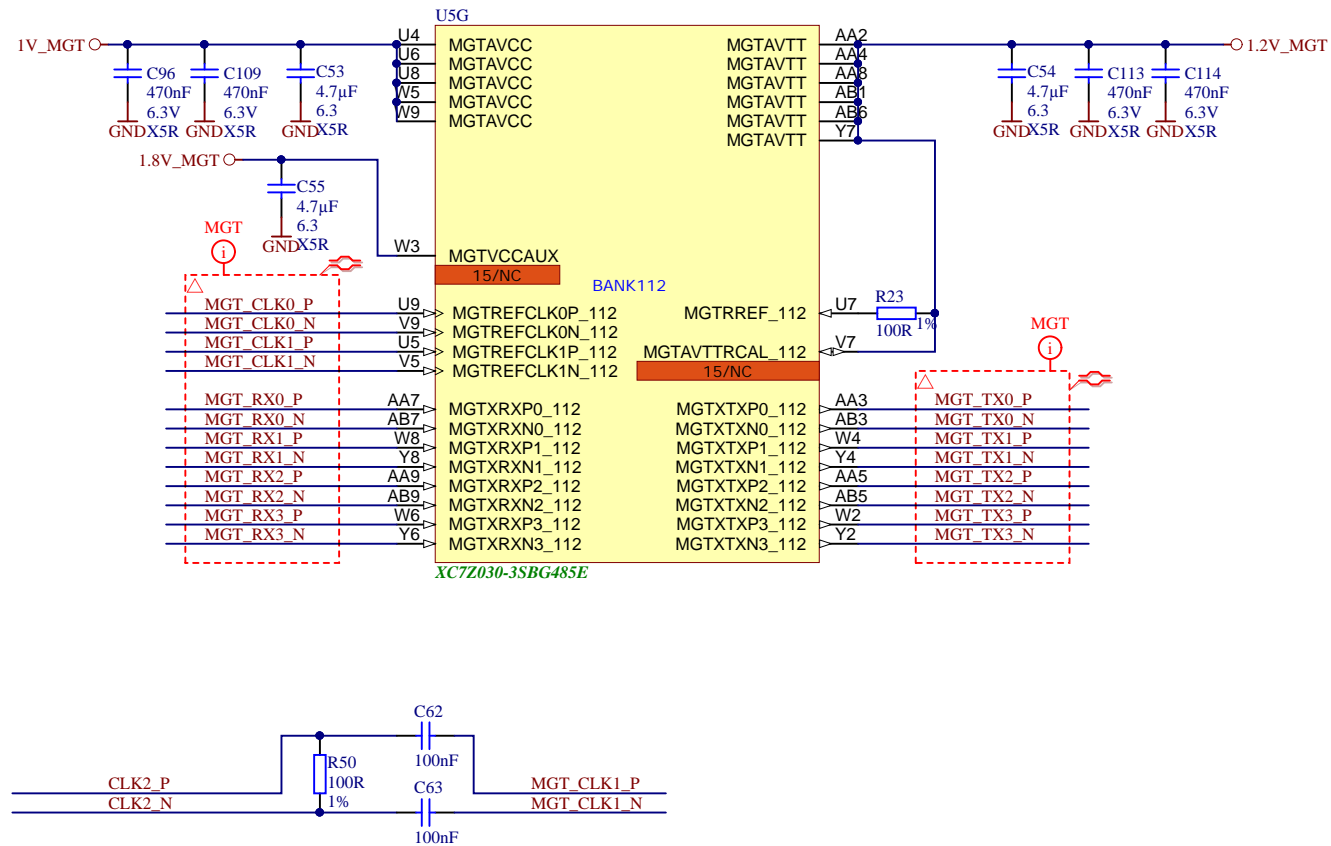
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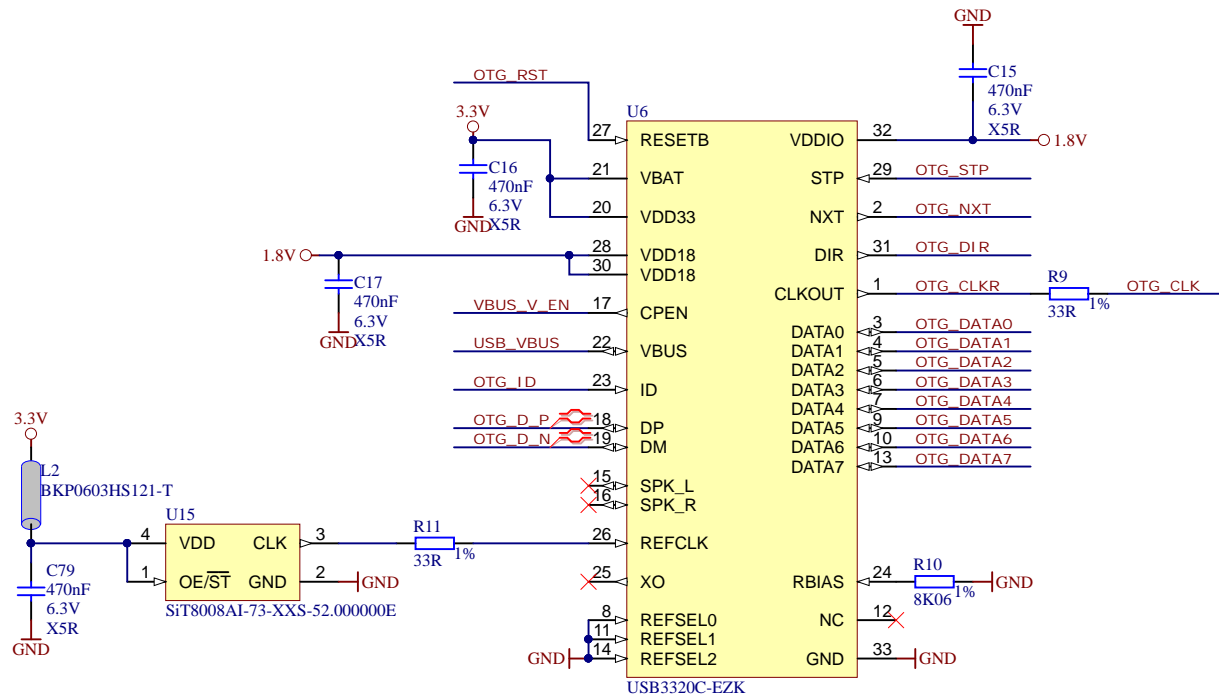
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| | Title: TE0715 - ETH_PHY | |
| | A4 | Number: TE0715 TE0715-30-3E |
| | Date: 2015-10-14 | Copyright: 2013 Trenz Electronic GmbH |
| | Rev. 04 | Page 10 of 15 |
| Filename: ETH-PHY.SchDoc | | |




| | | |
|-------------------------------|----------------------------------|---------------|
| Title: TE0715 - Clock and RTC | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: Trenz Electronic GmbH | Page 11 of 15 |
| Filename: Clock.SchDoc | | |



| | | | |
|--|--------------------------|---------------------------------------|---------------|
| | Title: TE0715 - FPGA_MGT | | |
| | A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| | Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page 12 of 15 |
| | Filename: MGT.SchDoc | | |



| | | | |
|---|--|---------------------------------------|--|
|  | | Title: TE0715 - USB_PHY | |
| | | A4 | Number: TE0715 TE0715-30-3E |
| Date: 2015-10-14 | | Copyright: 2013 Trenz Electronic GmbH | |
| Filename: USB-PHY.SchDoc | | Page 13 of 15 | |

A

B

C

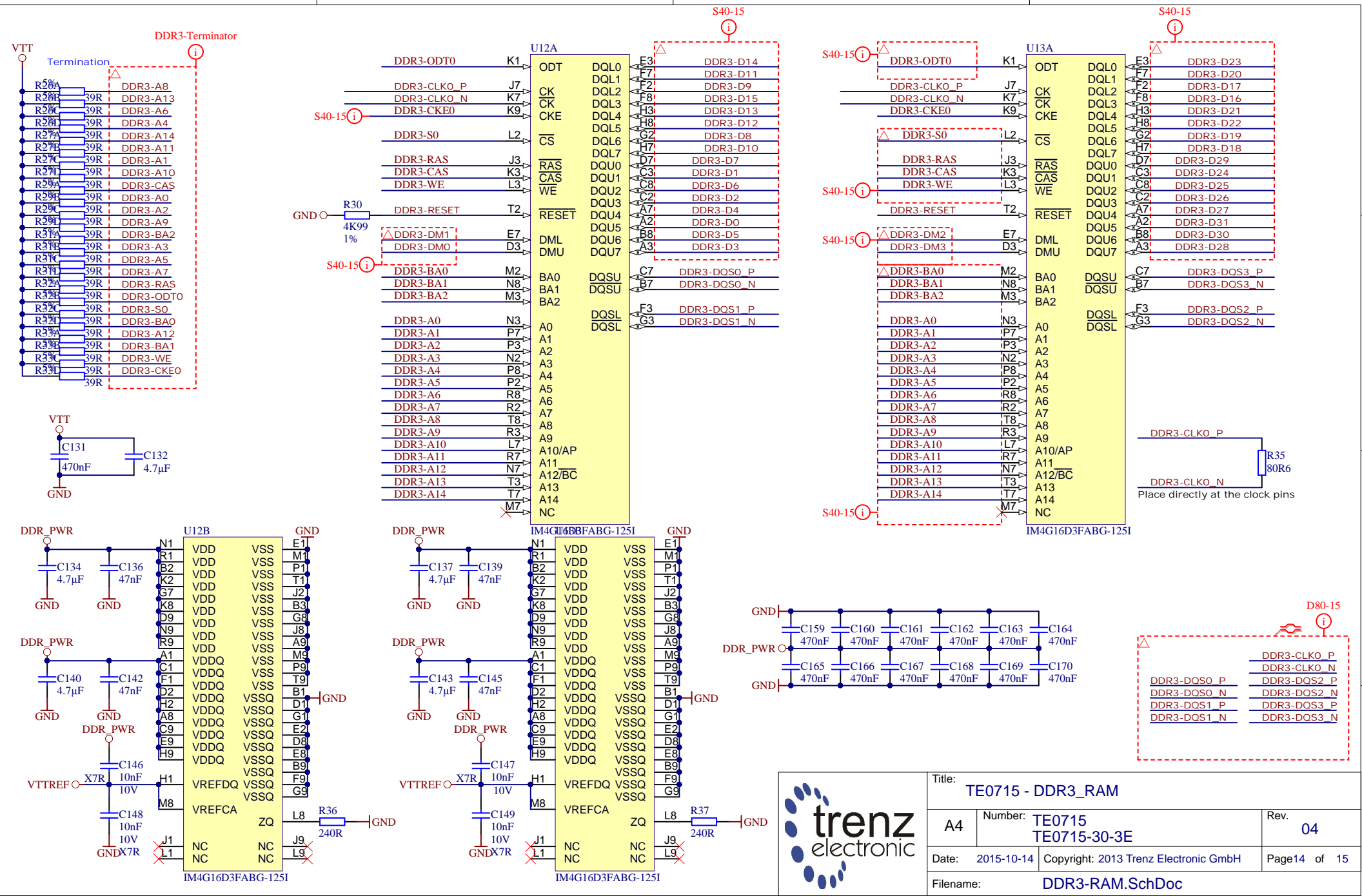
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A

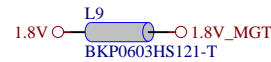
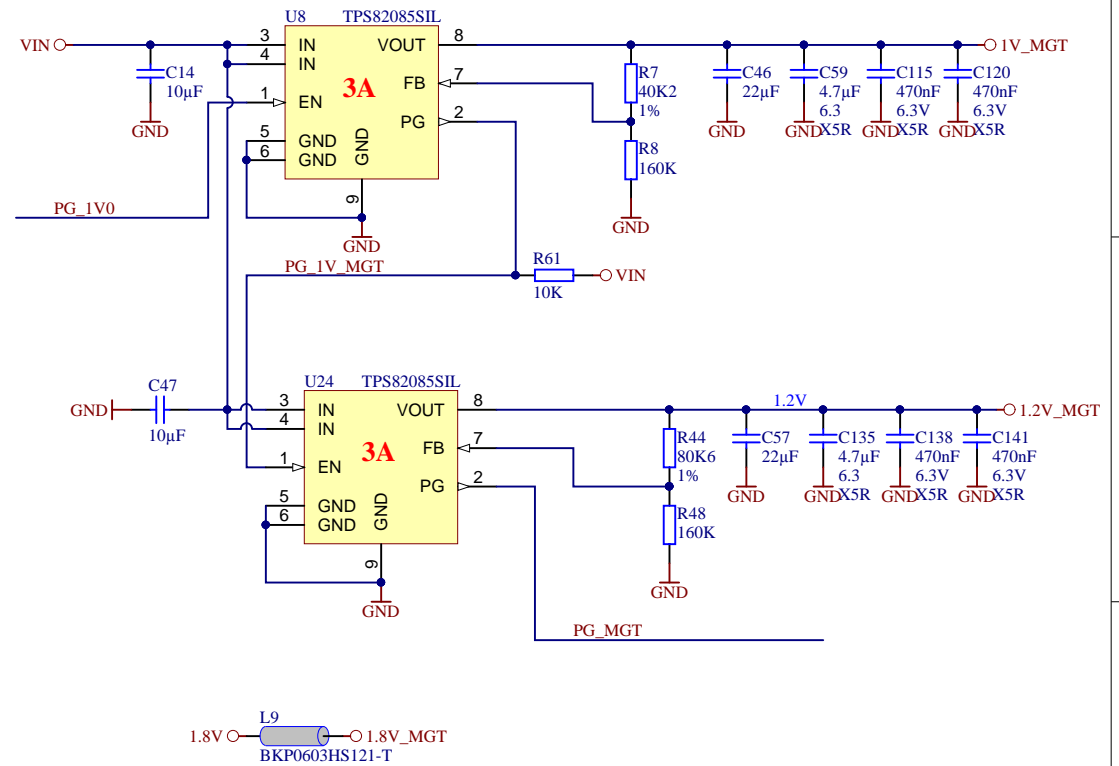
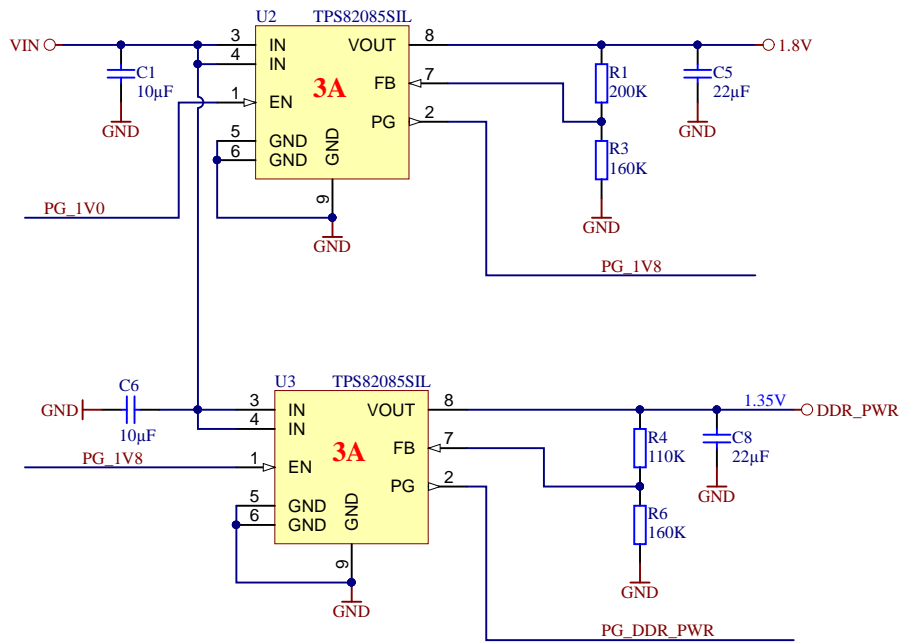
B

C

D



| | | |
|----------------------------------|--|----------------|
| Title: TE0715 - DDR3_RAM | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| Date: 2015-10-14 | Copyright: 2013 Trenz Electronic GmbH | Page 14 of 15 |
| Filename: DDR3-RAM.SchDoc | | |



| | | | |
|--|--------------------------|---------------------------------------|---------------|
| | Title: TE0715 - Power | | |
| | A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
| | Date: 2015-10-14 | Copyright: Trenz Electronic GmbH / TT | Page 15 of 15 |
| | Filename: POWER_2.SchDoc | | |

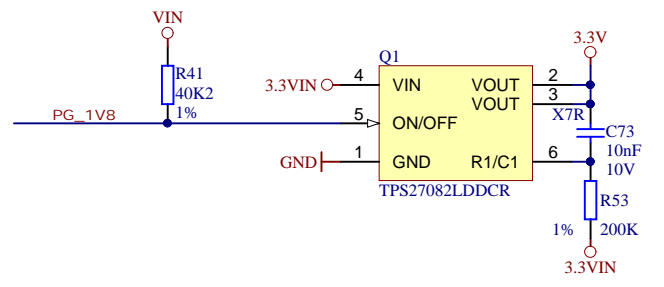
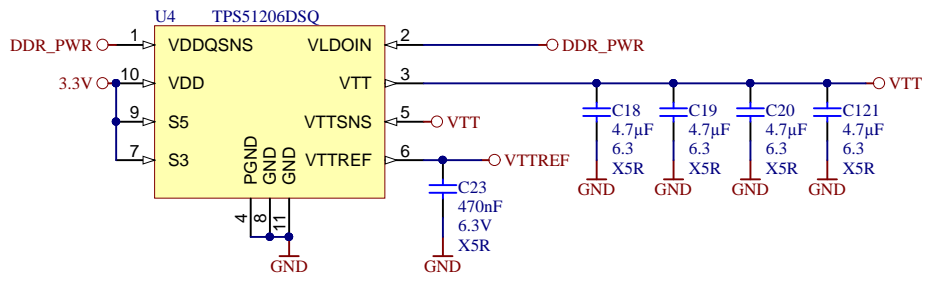
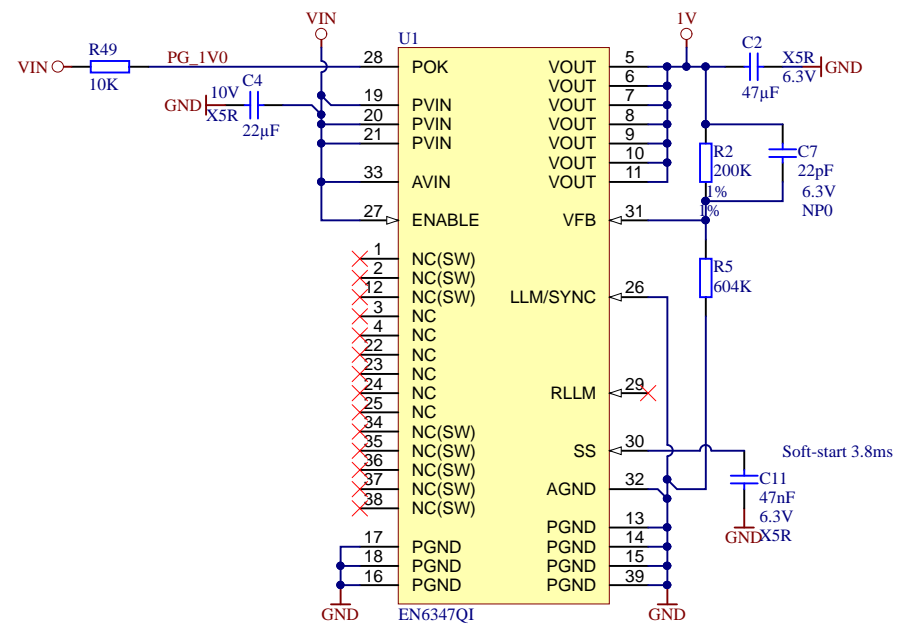
1

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3

4

- VIN ○ TP1 ● Testpoint 0.8mm
- DDR_PWR ○ TP2 ● Testpoint 0.8mm
- 1.8V ○ TP3 ● Testpoint 0.8mm
- 3.3V ○ TP4 ● Testpoint 0.8mm
- VTT ○ TP5 ● Testpoint 0.8mm
- VTTREF ○ TP6 ● Testpoint 0.8mm
- 3.3VIN ○ TP7 ● Testpoint 0.8mm
- 1.2V_MGT ○ TP8 ● Testpoint 0.8mm
- 1V ○ TP9 ● Testpoint 0.8mm
- GND | TP10 ● Testpoint 0.8mm
- GND | TP11 ● Testpoint 0.8mm
- GND | TP12 ● Testpoint 0.8mm
- GND | TP14 ● Testpoint 0.8mm
- GND | TP16 ● Testpoint 0.8mm
- GND | TP17 ● Testpoint 0.8mm



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|------------------------|---------------------------------------|---------------|
| Title: TE0715 - Power | | |
| A4 | Number: TE0715 TE0715-30-3E | Rev. 04 |
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| Filename: POWER.SchDoc | | |

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4